ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	FEATURES	SMBUS ADDRESS
EMC1043-1-ACZL-TR	8 pinMSOP package (Lead Free ROHS compliant)	Two external diodes with REC and Beta Compensation and Hottest Of Comparision	1001_100x
EMC1043-2-ACZL-TR			1001_101x
EMC1043-3-ACZL-TR			1001_000x
EMC1043-4-ACZL-TR			1001_001x
EMC1043-5-ACZL-TR		Two external diodes with REC. Beta Compensation on External Diode 1 only. Hottest of Comparision	1001_100x

Reel size is 4,000 pieces.

Evaluation Boards available upon request. (EVB-EMC1043, EVB-EMC1043C)

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Chapter 1 Pin Function

Figure 1.1 EMC1043 Pin Diagram

Table 1.1 EMC1043 Pin Description

PIN	PIN NO.	DESCRIPTION
DP1	1	External Diode 1 Positive (anode) Connection
DN1	2	External Diode 1 Negative (cathode) Connection
DP2	3	External Diode 2 Positive (anode) Connection
DN2	4	External Diode 2 Negative (cathode) Connection
GND	5	Ground
VDD	6	Supply Voltage
SMDATA	7	System Management Bus Data - bi-directional data, open drain output
SMCLK	8	System Management Bus Clock Input

Chapter 2 Electrical Specifications

2.1   Absolute Maximum Ratings

Table 2.1 Absolute Maximum Ratings

DESCRIPTION	RATING	UNIT
Supply Voltage V_{DD}	-0.3 to 5.0	V
Voltage on SMDATA and SMCLK pins	-0.3 to 5.5	V
Voltage on any other pin	-0.3 to VDD+0.3	V
Operating Temperature Range	-40 to 125	°C
Storage Temperature Range	-55 to 150	°C
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020	
Package Thermal Characteristics for MSOP-8		
Thermal Resistance T_{JA}(at 0 air flow)	135.9	°C/W
ESD Rating, All Pins Human Body Model	2000	V

Note: Stresses above those listed could cause damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

2.2   Electrical Specifications

Table 2.2 Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
V_{DD}=3.0V to 3.6V, T_A= -20°C to +85°C, Typical values at T_A = 27°C unless otherwise noted						
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Average Operating Current	I_{DD}		340	400	µA	4 conversions/s See Table 4.4.
	I_{STBY}		2	4	µA	Standby mode
Internal Temperature Monitor						
Temperature Accuracy			± 1	± 3	°C	-20°C≤ T_A ≤85°C
				± 1.5	°C	0°C < T_A ≤ 85°C
Temperature Resolution			0.125		°C	

Table 2.2 Electrical Characteristics (continued)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
V_{DD}=3.0V to 3.6V, T_A= -20°C to +85°C, Typical values at T_A = 27°C unless otherwise noted						
External Temperature Monitor						
Temperature Accuracy Remote Diode 40°C to 80°C Remote Diode -20°C to 125°C Remote Diode -64°C to 192°C				± 1 ± 3 ± 5	°C °C °C	15°C≤T_A≤70°C -20°C≤T_A≤85°C -20°C≤T_A≤85°C
Temperature Resolution			0.125		°C	
Filter Capacitor	C_{FILTER}			2.2	nF	Connected across external diode Note 2.2
Voltage Tolerance						
Voltage at pin (SMDATA,SMCLK)	V_{TOL}	-0.3		5.5	V	
SMBus Interface (SMDATA,SMCLK)						
Input High Level	V_{IH}	2.0			V	
Input Low Level	V_{IL}			0.8	V	
Input High/Low Current	I_{IH}/I_{IL}	-1		1	μA	
Hysteresis			500		mV	
Input Capacitance			5		pF	
Output Low Sink Current		6			mA	SMDATA = 0.6V
SMBus Timing						
Clock Frequency	F_{SMB}	10		400	kHz	
Spike Suppression				50	ns	
Bus free time Start to Stop	T_{BUF}	1.3			μS	
Hold time Start	$T_{HD:STA}$	0.6			μS	
Setup time Start	$T_{SU:STA}$	0.6			μS	
Setup time Stop	$T_{SU:STO}$	0.6			μS	
Data Hold Time	$T_{HD:DAT}$	0.3			μS	
Data Setup Time	$T_{SU:DAT}$	100			ns	
Clock Low Period	T_{LOW}	1.3			μS	
Clock High Period	T_{HIGH}	0.6			μS	
Clock/Data Fall Time	T_F	*		300	ns	*Min = 20+0.1C_b ns
Clock/Data Rise Time	T_R	*		300 Note 2.1	ns	*Min = 20+0.1C_b ns
Capacitive Load (each bus line)	C_b	0.6		400	pF	

Note 2.1 300nS rise time max is required for 400kHz bus operation. For lower clock frequencies, the maximum rise time is $(0.1/F_{SMB})+50nS$

Note 2.2 See SMSC Applications for Application Notes and Guidelines when measuring GPU processor diodes and CPU processor diodes.

2.3   System Management Bus Interface Protocol

A host controller, such as an SMSC I/O controller, communicates with the EMC1043 via the two wire serial interface named SMBus. The SMBus interface is used to read and write registers in the EMC1043, which is a slave-only device. A detailed timing diagram is shown in Figure 2.1.
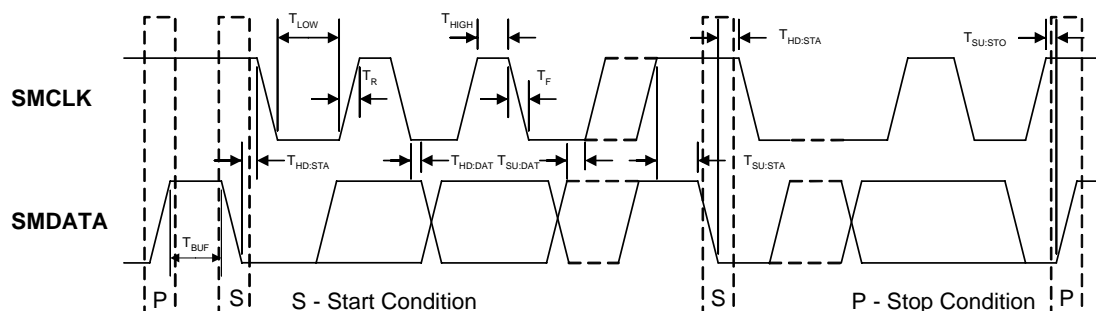
Figure 2.1 System Management Bus Timing Diagram

The EMC1043 implements a subset of the SMBus specification and supports Write Byte, Read Byte, Send Byte, and Receive Byte protocols as shown. In the tables that describe the protocol, the "gray" columns indicate that the slave is driving the bus.

All of the below protocols use the following convention:

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

2.3.1   Write Byte

The Write Byte is used to write one byte of data to the registers as shown in Table 2.3.

Table 2.3 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	STOP
1	7	1	1	8	1	8	1	1

2.3.2   Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 2.4.

Table 2.4 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	COMMAND	ACK	START	SLAVE ADDRESS	RD	ACK	DATA	NACK	STOP

Table 2.4 Read Byte Protocol

1	7	1	1	8	1	1	7	1	1	8	1	1

2.3.3   Send Byte

The Send Byte protocol is used to set the Internal Address Register to the correct Address as shown in Table 2.5. The Send Byte can be followed by the Receive Byte protocol described in Table 2.6 to read data from the register. The send byte protocol cannot be used to write data - if data is to be written to a register then the write byte protocol must be used as described in Section 2.3.1.

Table 2.5 Send Byte Protocol

START	SLAVE ADDR	WR	ACK	REG. ADDR	ACK	STOP
1	7	1	1	8	1	1

2.3.4   Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This can be used for consecutive reads of the same register as shown in Table 2.6.

Table 2.6 Receive Byte Protocol

START	SLAVE ADDR	RD	ACK	REG. DATA	NACK	STOP
1	7	1	1	8	1	1

2.3.5   SMBus Timing Diagram

The Timing for the SMBus is shown in Figure 2.1.

2.4   SMBus Addresses

The EMC1043 may be ordered with one of four slave addresses as shown in Ordering Information. Attempting to communicate with the EMC1043 SMBus interface with an invalid slave address or invalid protocol results in no response from the device and does not affect its register contents. The EMC1043 supports stretching of the SMCLK signal by other devices on the SMBus but will not perform this operation itself.

2.5   SMBus Timeout

The EMC1043 includes an SMBus time-out feature. Following a 25 ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface.

Chapter 3 Product Description

The EMC1043 is an SMBus sensor that monitors three temperature zones for use in a personal computer or embedded environment. The part may be used as a companion to one of SMSC's broad line of SIO host devices to perform fan control and thermal management.

The EMC1043-1, EMC1043-2, EMC1043-3 and EMC1043-4 are designed specifically to work with a CPU that implements the thermal diode as a PNP substrate transistor with the collector connected to GND. A new feature called beta compensation automatically compensates for measurement error caused by beta variation in CPU thermal diodes as described in Section 3.7.

Because the beta compensation circuit is designed to work with PNP substrate transistors, the EMC1043-1, EMC1043-2, EMC1043-3 and EMC1043-4 are not typically used with diode-connected transistors (such as the 2N3904) or CPUs that implement the thermal diode as a two-terminal diode (such as the AMD processor). However, the beta compensation feature may be disabled by configuring the appropriate register as described in Section 4.8. For applications that measure a two-terminal thermal diode, refer to the EMC1063.

A typical system is shown in Figure 3.1
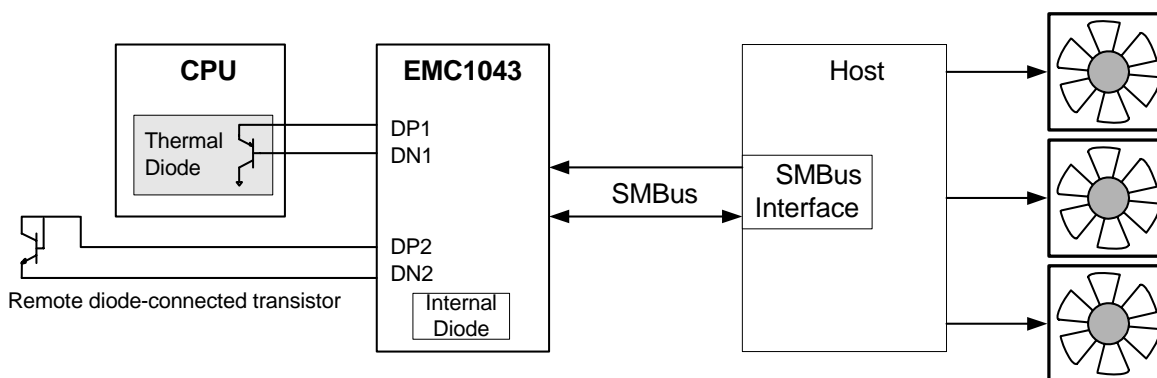
Figure 3.1 EMC1043 System Drawing

3.1   Power Modes

The EMC1043 has two power modes.

- Run Mode - In this mode, the temperature monitors are active and converting at the programmed conversion rate. The average power dissipation will depend on the conversion rate. When the EMC1043 is not actively converting a channel, it goes into a lower power wait state.

- Standby Mode (power-up default) - in this mode, the EMC1043 is put into a low power state. In the standby mode, temperature monitoring is disabled. The device will still respond to SMBus commands.

3.2   One Shot During Standby Mode

The EMC1043 supports a One-Shot command when it is in Standby Mode. Writing to the One-Shot register will cause the device to power up, perform 1 full set of temperature conversions, then return to Standby Mode.

3.3   Operation During Run Mode

When the device is active, there are two modes of operation available.

- Normal Mode (power-up default) - In this mode of operation, the EMC1043 continuously samples and updates all of its temperature channels.

- Hotter of Two Mode - In this mode, the EMC1043 continuously samples and then compares the two remote zones. The hotter of the two remote zones is loaded into the External Diode 2 Data Registers. In addition, the HOTTER bit in the Status register is set or cleared to indicate which external diode zone is hotter. If the two remote zones are exactly equal to each other, then the HOTTER bit is cleared (set to '0'), and the results of the two remote zones are stored in their respective registers.

3.3.1   Conversion Rates

The EMC1043 may be configured for different conversion rates based on the system requirements. The available rates are 1 full set of conversions per second to 16 full sets of conversions per second. The conversion rate is configured as described in Section 4.4. The available conversion rates are shown in Table 4.4.

3.3.2   Dynamic Averaging

The EMC1043 temperature channels support a new feature that measures the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled as described in Section 4.5 for increased power savings at the lower conversion rates. When Dynamic Averaging is enabled, the device will automatically adjust the sampling and measurement time for both external diode channels. This allows the device to average 2x or 4x longer than the normal 11 bit operation while still maintaining the selected conversion rate. The benefits of Dynamic Averaging are improved noise rejection due to the longer integration time as well as less random variation on the temperature measurement.

The Dynamic Averaging applies when a One-Shot command is issued. The device will perform the desired averaging during the one-shot operation according to the selected conversion rate.

The Dynamic Averaging will affect the average supply current based on the chosen conversion rate as shown in Table 3.1.

Table 3.1 Supply Current vs. Conversion Rate and ADC Averaging Factor

CONVERSION RATE	ADC AVERAGING FACTOR		
	4X (MAX_RES = 1) (DA_N = 0)	2X (MAX_RES = 0) (DA_N = 0)	1X (DA_N = 1)
1 / sec	190uA	132uA	105uA
2 / sec	315uA	205uA	150uA
4 / sec	580uA	350uA	235uA
8 / sec	N/A	640uA	405uA
16 / sec	N/A	N/A	750uA

3.4   Temperature Monitors

In general, thermal diode temperature measurements are based on the change in forward bias voltage of a diode when operated at two different currents. This ΔV_{BE} is then proportional to absolute temperature as shown in the following equation:

$$\Delta V_{BE} = V_{BE\_HIGH} - V_{BE\_LOW} = \frac{\eta kT}{q} \ln\left(\frac{I_{HIGH}}{I_{LOW}}\right)$$

where:

k = Boltzmann's constant

T = absolute temperature in Kelvin   **[1]**

q = electron charge

η = diode ideality factor
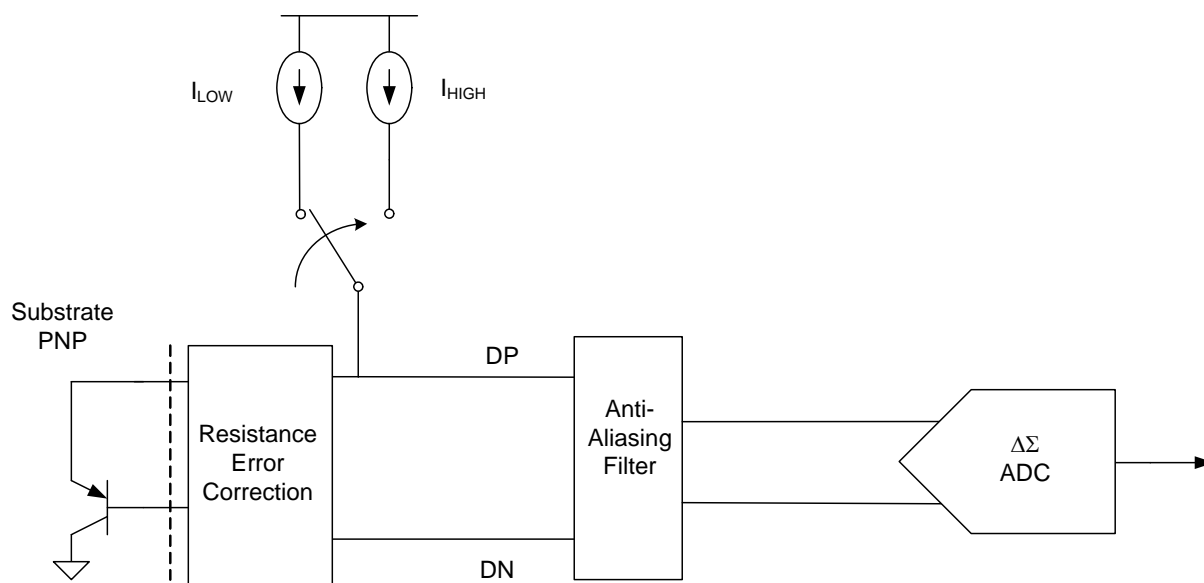
Figure 3.2 Block Diagram of Temperature Monitoring Circuit

Figure 3.2 shows a block diagram of the temperature measurement circuit. The negative terminal for the remote temperature diode, DN, is internally biased with a forward diode voltage referenced to ground.

The EMC1043-1, EMC1043-2, EMC1043-3 and EMC1043-4 are designed to work with the PNP substrate transistor in a CPU. The External Diode 2 channel in the EMC1043-5 has beta compensation disabled by default.

The external diodes in all versions of the EMC1043 are compatible with a broad range of thermal diodes that may be connected as shown in Figure 3.3 (see Section 4.8 for programming details when using diode-connected transistors as the external diodes).

Typical
substrate
i.e. CPU substrate
PNP

Typical
remote
discrete PNP transistor
i.e.
2N3906

Typical
remote
discrete NPN transistor
i.e.
2N3904
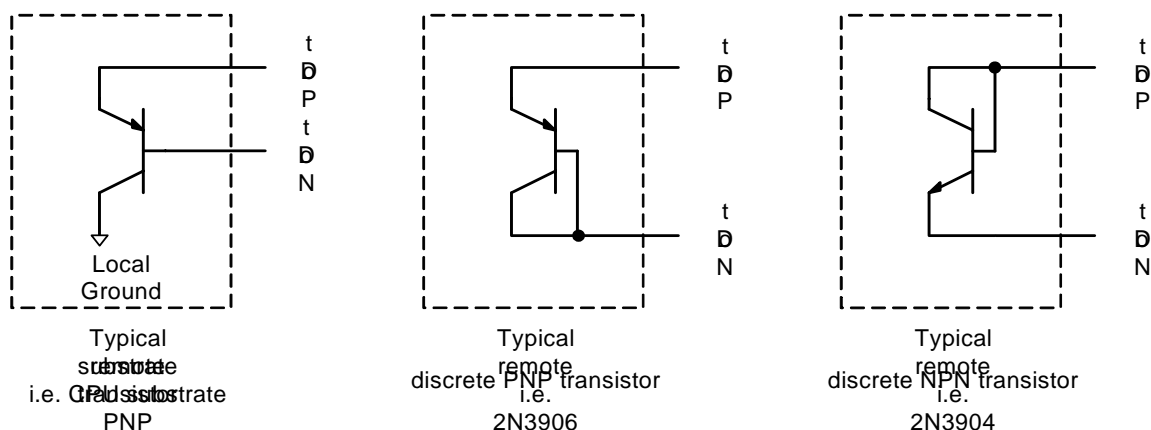
Figure 3.3 External Diode Configurations

3.5   Temperature Measurement Results and Data

Each temperature result for each zone is available in two byte wide data registers. As shown in Section 4.1, the 11-bit format has the 8 most significant bits stored in the high byte register and the 3 least significant bits stored in the three MSB positions of the low byte register. The delta-sigma ADC may be operated with more than 11 bits of resolution for improved averaging as described in Section 4.5, but the temperature result is reported at 11-bit resolution.

The temperature results for the two remote zones are also stored in extended format with a range from -64°C to +191°C. The data format is a 2's complement number offset by 64°C as shown in Section 4.2. The data for each of the remote zones in both legacy and extended format is stored in separate data registers so that both data formats are always available. Table 3.2 shows the default and extended range formats.

Table 3.2 EMC1043 Temperature Data Format

	RANGE -64°C TO 127°C	RANGE -64°C TO 191°C
TEMPERATURE (°C)	BINARY	OFFSET BINARY
Diode Fault	100 0000 0000	100 0000 0000
<= -64	110 0000 0000	100 0000 0000
-63.875	110 0000 0001	100 0000 0001
-63	110 0000 1000	100 0000 1000
-1	111 1111 1000	101 1111 1000
0	000 0000 0000	110 0000 0000
0.125	000 0000 0001	110 0000 0001
1	000 0000 1000	110 0000 1000
64	010 0000 0000	000 0000 0000
65	010 0000 1000	000 0000 1000
127	011 1111 1000	001 1111 1000
127.875	011 1111 1111	001 1111 1111
128	011 1111 1111	010 0000 0000
191	011 1111 1111	011 1111 1000
>= 191.875	011 1111 1111	011 1111 1111

3.6   Resistance Error Correction (REC)

Resistance error correction is an automatic feature that eliminates the need to characterize and compensate for series resistance in the external diode lines. The EMC1043 corrects for as much as 100 ohms of series resistance.

When using a temperature sensor that does not include resistance error correction, voltage developed across the parasitic resistance in the external diode path produces an error in the reported temperature. The error introduced by this resistance is approximately +0.7°C per ohm. Sources of series resistance are PCB trace resistance, on die (i.e. on the processor) metal resistance, bulk resistance in the base and emitter of the temperature transistor.

When monitoring the thermal diode of an AMD K8 processor, the Resistance Error Correction must be disabled for accurate temperature measurements. This is accomplished by clearing the REC bit in the configuration 2 register (see Section 4.5). Please see Application note "13.16 - Using the EMC1043 with AMD Processors" for more details.

3.7   Beta Compensation

The Beta Compensation function automatically eliminates temperature errors caused by beta variation in modern, low beta transistors used for monitoring processor temperatures.   Changes in beta as differing currents are applied to temperature transistors can cause significant temperature errors in monitoring devices. As modern processor geometries shrink the trend is for transistor betas to decrease, which exacerbates temperature errors.

Discrete transistors, with collector connected to base to form a diode, are generally immune to these temperature errors because of high (>100) betas. A beta variation of 10% from low current to high current, when beta equals 100, induces approximately 0.12° error at 100°C. However for a low beta (1.0) substrate transistor used for processor temperature measurement, a beta variation of 10% from low to high current induces approximately 6.12° error at 100°C.

Because the Beta Compensation function is designed to be used with substrate PNP transistors only, this function should be disabled when using a diode-connected transistor (such as the 2N3904) or CPUs that implement the thermal diode as a two-terminal device. The Beta Compensation function is disabled by writing 07h to the Beta Configuration register

When measuring an AMD K8 processor, the Beta Compensation circuitry must be disabled. See Section 4.8. Please see SMSC Application note "13.16 - Using the EMC1043 with AMD Processors" for more details.

3.8 Programmable Ideality Factor

The EMC1043 default is for a diode ideality factor of 1.008 which is common for a 2N3904 diode and for many processor transistors. When a diode or transistor is used that has a different ideality factor value than 1.008 a temperature error is induced that is a linear function of temperature. Previous solutions for this mismatch in ideality factor has been to supply a programmable offset to the temperature reading which corrects the error at a single temperature but causes a residual error at all other temperatures. The EMC1043 ideality factor register corrects this mismatch error at all temperatures (see Section 4.7).

APPLICATION NOTE: When monitoring a substrate transistor or CPU diode and beta compensation is enabled, the Ideality Factor should not be adjusted. Beta Compensation automatically corrects for most ideality errors.

3.9 Diode Faults

The EMC1043 detects a fault if the DP pin is left floating or is shorted to VDD. In the case of a diode fault, the corresponding status bit will be set and the output data will be set at 400h.

Chapter 4 Register Set and Description

The following registers are accessible through the SMBus Interface.

Table 4.1 EMC1043 Register Set

REGISTER ADDRESS READ	WRITE	R/W	REGISTER NAME	SYMBOL	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT VALUE
00h	N/A	R	Internal Temperature High Byte - Legacy Format	INTHBL	Sign	64	32	16	8	4	2	1	00h
23h	N/A	R	Internal Temperature Low Byte - Legacy Format	INTLBL	0.5	0.25	0.125						00h
01h	N/A	R	External Diode 1 High Byte - Legacy Format	ET1HBL	Sign	64	32	16	8	4	2	1	00h
10h	N/A	R	External Diode 1 Low Byte - Legacy Format	ET1LBL	0.5	0.25	0.125						00h
F8h	N/A	R	External Diode 2 High Byte - Legacy Format	ET2HBL	Sign	64	32	16	8	4	2	1	00h
F9h	N/A	R	External Diode 2 Low Byte - Legacy Format	ET2LBL	0.5	0.25	0.125						00h
FAh	N/A	R	External Diode 1 High Byte - Extended Format	ET1HBE	128	64	32	16	8	4	2	1	00h
FBh	N/A	R	External Diode 1 Low Byte - Extended Format	ET1LBE	0.5	0.25	0.125						00h
FCh	N/A	R	External Diode 2 HIgh Byte - Extended Format	ET2HBE	128	64	32	16	8	4	2	1	00h

Table 4.1 EMC1043 Register Set (continued)

REGISTER ADDRESS READ	REGISTER ADDRESS WRITE	R/W	REGISTER NAME	SYMBOL	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT VALUE
FDh	N/A	R	External Diode 2 Low Byte - Extended Format	ET2LBE	0.5	0.25	0.125						00h
							Status and Control						
02h	N/A	R	Status	STS	Busy	-	-	HOTTER	-	-	D2	D1	00h
03h	09h	R/W	Configuration	CFG	-	ADC_STOP	-	-	-	CR<2:0>			45h
04h	04h	R/W	Configuration 2	CFG2	-	-	-	-	MAX_RES	DA_n	COMP	REC	09h
							One Shot						
N/A	0Fh	W	One Shot Conversion	Shot	The data written to this register is irrelevant and will not be stored								00h
							Ideality						
27h	27h	R/W	External Diode 1 Ideality Correction Factor	IDCF1	-	-	B5	B4	B3	B2	B1	B0	12h (1.008)
28h	28h	R/W	External Diode 2 Ideality Correction Factor	IDCF2	-	-	B5	B4	B3	B2	B1	B0	12h (1.008)
29h	29h	R/W	External Diode 1 Beta Configuration	BCF1	-	-	-	-	-	BETA<2:0>			03h

Table 4.1 EMC1043 Register Set (continued)

REGISTER ADDRESS READ	WRITE	R/W	REGISTER NAME	SYMBOL	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT VALUE
2Ah	2Ah	R/W	External Diode 2 Beta Configuration	BCF2	-	-	-	-	-	BETA<2:0>			03h (07h for EMC1043-5)
EDh	EDh	R	Product ID	PID	0	0	0	0	1	1	0	0	0Ch (-1)
					0	0	0	0	1	1	0	1	0Dh (-2)
					0	0	0	0	1	1	1	0	0Eh (-3)
					0	0	0	0	1	1	1	1	0Fh (-4)
					0	0	1	0	1	1	0	0	2Ch (-5)
FEh	FEh	R	Manufacturer ID	SMSC	0	1	0	1	1	1	0	1	5Dh
FFh	FFh	R	Revision Register	REV	-	-	-	-	0	0	0	1	01h

During Power on Reset (POR), the default values are stored in the registers. A POR is initiated when power is first applied to the part and the voltage on the VDD supply surpasses the POR level as specified in the electrical characteristics. Any reads to undefined registers will return 00h. Writes to undefined registers will not have an effect.

The EMC1043 uses an interlock mechanism that will update the Low byte of a particular monitor when the High Byte is read. This prevents changes in register content when the ADC updates between successive reads.

4.1 Legacy Temperature Data Registers (00h, 23h, 01h, 10h, F8h, F9h)

As shown in Table 4.1, each temperature monitor has two data registers. The 11 bit temperature data is stored aligned to the left resulting in the High Byte containing temperature in 1°C steps and the Low Byte containing fractions of a degree.

4.2 Extended Format Temperature Registers (FAh-FDh)

The Extended Format Temperature Registers store only the external diode temperatures in the extended data format. This is because, due to the operating range limitations of the EMC1043, the internal temperature could not benefit from the extended temperature range. Like the Legacy data formatting, the data is stored in two registers per temperature channel.

4.3   Status Register - 02h

Table 4.2 Status Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
02h	Status	Busy	-	-	HOTTER	-	-	D2	D1	00h

The Status Register is a read only register and returns the operational status of the part. External diode faults are indicated by bits 1 and 0. If either bit is set to '1', then a diode fault has occurred. When a diode fault occurs, the D1 or D2 status bit is set, but otherwise the data remains unchanged.

Bit 7 - Busy - indicates that the ADC is currently converting a temperature.

Bit 4 - HOTTER - during Hotter of Two mode, this bit indicates which of the external diode channels is hotter. If this bit is '0', then External Diode 1 is hotter or equal to External Diode 2. If this bit is '1', then External Diode 2 is hotter than External Diode 1. During normal operation, this bit will always read a '0'.

Bit 1 - D2 - indicates that a diode fault has occurred on External Diode 2.

Bit 0 - D1 - indicates that a diode fault has occurred on External Diode 1.

4.4   Configuration Register (03h Read, 09h Write)

Table 4.3 Configuration Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
03h Read, 09h Write	Config	-	STANDBY	-	-	-	CR<2:0>			45h

The Configuration Register controls the basic functionality of the EMC1043. The bits are described below:

Bit 6 - STANDBY- controls the ADC conversions and power modes of the part.

- '0' - The device is in the run operating mode. The ADC is converting at the user-programmed conversion rate.
- '1' - (default) The device is in the standby operating mode (see Section 3.1).

Bit 2-0 - CR<2:0> - determines the conversion rate for the temperature monitoring per Table 4.4.

Table 4.4 Conversion Rate

CR<2:0>			CONVERSIONS / SECOND (CONVERSION TIME)
2	**1**	**0**	
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	1 Conversion / sec
1	0	0	2 Conversions / sec
1	0	1	4 Conversions / sec (default)
1	1	0	8 Conversions / sec
1	1	1	16 Conversions / sec

4.5   Configuration 2 Register - (04h)

Table 4.5 Configuration 2 Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
04h	CFG2	-	-	-	-	MAX_RES	DA_n	COMP	REC	09h

The Configuration 2 Register controls the basic functionality of the EMC1043 that is NOT compatible with the EMC1023.

Bit 3 - MAX_RES - controls the external diode conversion time during dynamic averaging. Although the dynamic averaging may be used to increase the ADC resolution, only 11 bits of data are available in the temperature registers.

- '0' - the dynamic averaging will set the ADC averaging factor at 1x when the conversion rate is set at 16 conversions per second and 2x at conversion rates lower than 16 per second.

- '1' (default) - the dynamic averaging will set the ADC averaging factor at 1x when the conversion rate is set at 16 conversions per second, 2x at 8 conversions / second and 4x at conversion rates lower than 8 per second.

Bit 2 - DA_n - controls the dynamic digital averaging circuitry. See Section 3.3.2.

- '0' (default) - dynamic averaging is enabled. Depending on the selected conversion rate, the ADC averaging factor is increased for the external diodes.

- '1' - dynamic averaging is disabled. The ADC averaging factor will remain fixed at 1x for all conversion rates and will allow increased power savings at the slower conversion rates.

Bit 1 - COMP - configures the device to perform a comparison for the Hotter of Two mode (see Section 3.3, "Operation During Run Mode," on page 12.)

- '0' (default) - the device is in normal mode

- '1' - the device is in Hotter of Two mode. In this mode, the two external diode channels are measured and compared against each other. The hotter of the two channels has its data loaded into the External Diode 2 Data Registers. The Internal Diode and External Diode 1 Data Registers remain unaffected.

Bit 0 - REC - controls the Resistance Error Correction circuitry

- ■ '0' - The Resistance Error Correction circuitry is disabled.

- ■ '1' (default) - The Resistance Error Correction circuitry is active and will automatically correct for up to 100 ohms of series resistance in the diode lines for both External Diode 1 and External Diode 2 channels.

4.6   One Shot Register - (0Fh)

Table 4.6 One Shot Registers

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Fh	One Shot Conversion	Writing to this register address initiates the one-shot. The data is not important and is not stored								00h

The One Shot Register is an address place holder for the one-shot command. Writing to the address initiates the command. The data written is not important and is not stored. Reading from the one-shot registers will always return 00h.

4.7   Ideality Configuration Registers (27h - 28h)

Table 4.7 Ideality Configuration Registers

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
27h	Diode 1 Ideality Correction Factor	-	-	B5	B4	B3	B2	B1	B0	12h (1.008)
28h	Diode 2 Ideality Correction Factor	-	-	B5	B4	B3	B2	B1	B0	12h (1.008)

The Ideality Configuration Registers store the ideality correction factor that is applied to each external diode.

The table below shows the ideality factor settings for the Ideality Configuration registers. Shading indicates power-up default. All codes that are not listed are reserved and should not be used.

Beta Compensation and Resistance Error Correction automatically correct for most diode ideality errors, therefore it is not recommended that these settings be updated without consulting SMSC.

Table 4.8 Ideality Factor Look Up Table

SETTING	FACTOR		SETTING	FACTOR		SETTING	FACTOR
001000	0.9951		011000	1.0159		101000	1.0377
001001	0.9964		011001	1.0173		101001	1.0391
001010	0.9976		011010	1.0186		101010	1.0404
001011	0.9989		011011	1.0199		101011	1.0418
001100	1.0002		011100	1.0213		101100	1.0432
001101	1.0015		011101	1.0226		101101	1.0446
001110	1.0028		011110	1.0240		101110	1.0460
001111	1.0041		011111	1.0253		101111	1.0475
010000	1.0054		100000	1.0267		110000	1.0489
010001	1.0067		100001	1.0280		110001	1.0503
010010	1.0080		100010	1.0294			
010011	1.0093		100011	1.0308			
010100	1.0106		100100	1.0321			
010101	1.0119		100101	1.0335			
010110	1.0133		100110	1.0349			
010111	1.0146		100111	1.0363			

For CPU substrate transistors that require the BJT transistor model, the ideality factor behaves slightly differently than for discrete diode-connected transistors. Refer to Table 4.9 when using a CPU substrate transistor.

Table 4.9 Substrate Diode Ideality Factor Look-Up Table (BJT Model)

SETTING	FACTOR		SETTING	FACTOR		SETTING	FACTOR
001000	0.9869		011000	1.0079		101000	1.0291
001001	0.9882		011001	1.0092		101001	1.0304
001010	0.9895		011010	1.0105		101010	1.0317
001011	0.9908		011011	1.0120		101011	1.0330
001100	0.9921		011100	1.0132		101100	1.0343
001101	0.9934		011101	1.0146		101101	1.0356
001110	0.9947		011110	1.0159		101110	1.0369
001111	0.9960		011111	1.0173		101111	1.0382
010000	0.9973		100000	1.0187		110000	1.0395

Table 4.9 Substrate Diode Ideality Factor Look-Up Table (BJT Model) (continued)

SETTING	FACTOR	SETTING	FACTOR	SETTING	FACTOR
010001	0.9986	100001	1.0200	110001	1.0408
010010	1.0000	100010	1.0213		
010011	1.0013	100011	1.0226		
010100	1.0026	100100	1.0239		
010101	1.0039	100101	1.0252		
010110	1.0053	100110	1.0265		
010111	1.0066	100111	1.0278		

APPLICATION NOTE: When measuring a 65nm Intel CPUs, the Ideality Setting should be the default 12h. When measuring 45nm Intel CPUs, the Ideality Setting should be 15h.

4.8 Beta Configuration Registers (29h - 2Ah)

Table 4.10 Beta Configuration Registers

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
29h	Diode 1 Beta Configuration	-	-	-	-	-	BETA<2:0>			03h
2Ah	Diode 2 Beta Configuration	-	-	-	-	-	BETA<2:0>			03h (07h for EMC1043-5)

The Beta Configuration Registers have a factory programmed power-on default based on the beta of the PNP substrate transistor that is being monitored as the external diode. The default value of the Diode 2 Beta Configuration Register of EMC1043-5 is 07h (disabled).

The beta compensation circuit is able to compensate for beta variation within a given range. The beta configuration register is configured to the proper range to match the CPU to be monitored. The beta values should be set so that the minimum expected beta is not below the threshold indicated in Table 4.11. Beta compensation is activated if the BETA<2:0> bits are set to any value other than 07h.

When using diode-connected transistors (such as the 2N3904) or CPUs that implement the thermal diode as a two-terminal diode, the Beta Configuration Register should be set to 07h.

Table 4.11 Beta Configuration Look Up Table

BETA<2:0>			MINIMUM BETA
2	1	0	
0	0	0	0.11
0	0	1	0.18
0	1	0	0.25

Table 4.11 Beta Configuration Look Up Table (continued)

BETA<2:0>			
2	**1**	**0**	**MINIMUM BETA**
0	1	1	0.33 (default)
1	0	0	0.43
1	0	1	1.00
1	1	0	2.33
1	1	1	Disabled

4.9   Product ID Register (EDh)

Table 4.12 Product ID Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
EDh	PID	0	0	X	0	1	1	X	X	0Ch (-1) 0Dh (-2) 0Eh (-3) 0Fh (-4) 2Ch (-5)

The Product ID Register holds the unique product ID for identifying SMSC EMC products. See Table 4.1 for a list of the product ID number for each version of the EMC1043.

4.10   Manufacturer ID Register (FEh)

Table 4.13 Manufacturer ID Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FEh	SMSC	0	1	0	1	1	1	0	1	5Dh

The Manufacturer ID register contains an 8 bit word that identifies the manufacturer of the EMC1043 (SMSC = 5Dh).
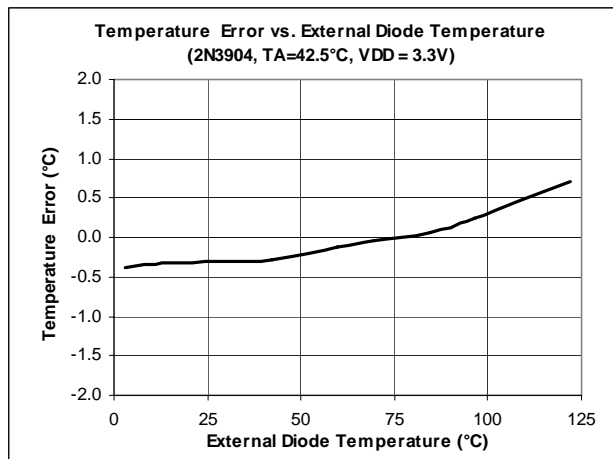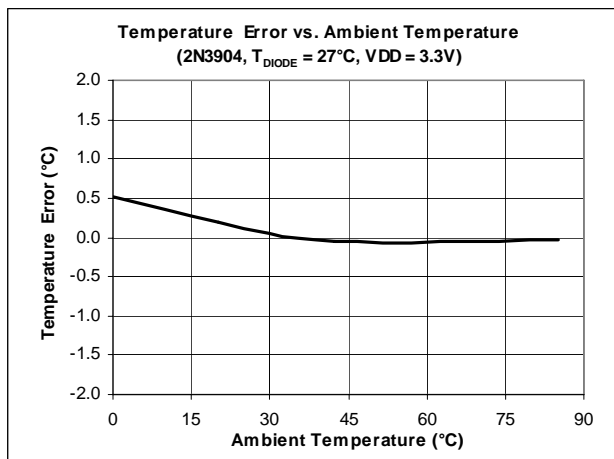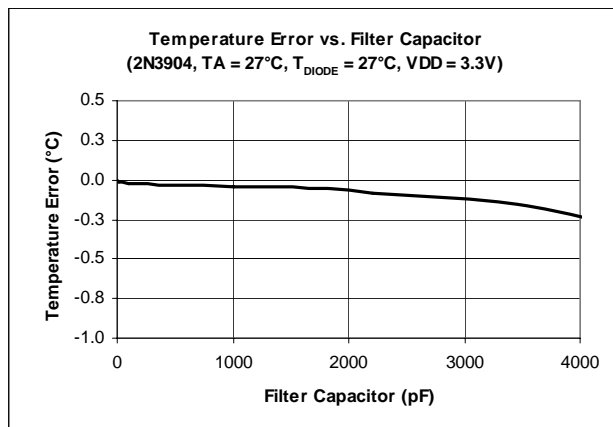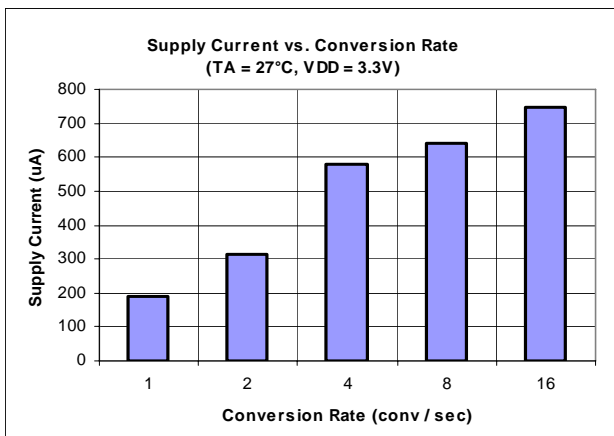
4.11   Revision Register (FFh)

Table 4.14 Revision Register

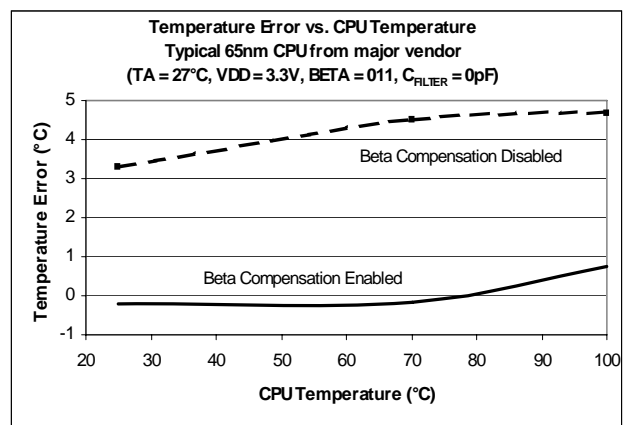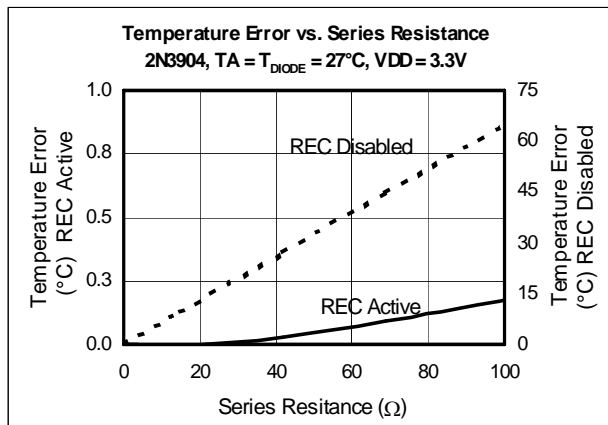| ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FFh	REV	-	-	-	-	0	0	0	1	01h

The Revision register contains a 4 bit word that identifies the die revision.

Chapter 5 Typical Operating Curves

Supply Current vs. Conversion Rate
(TA = 27°C, VDD = 3.3V)

Temperature Error vs. Filter Capacitor
(2N3904, TA = 27°C, T_{DIODE} = 27°C, VDD = 3.3V)

Temperature Error vs. Ambient Temperature
(2N3904, T_{DIODE} = 27°C, VDD = 3.3V)

Temperature Error vs. External Diode Temperature
(2N3904, TA=42.5°C, VDD = 3.3V)

Temperature Error vs. Leakage Resistance
(2N3904, TA = T_DIODE = 27°C, VDD = 3.3V)

Standby Current vs. Supply Voltage
(TA = 27°C)

Temperature Error vs. Series Resistance
2N3904, TA = T_DIODE = 27°C, VDD = 3.3V

Temperature Error vs. CPU Temperature
Typical 65nm CPU from major vendor
(TA = 27°C, VDD = 3.3V, BETA = 011, C_FILTER = 0pF)

Chapter 6 Package Outline
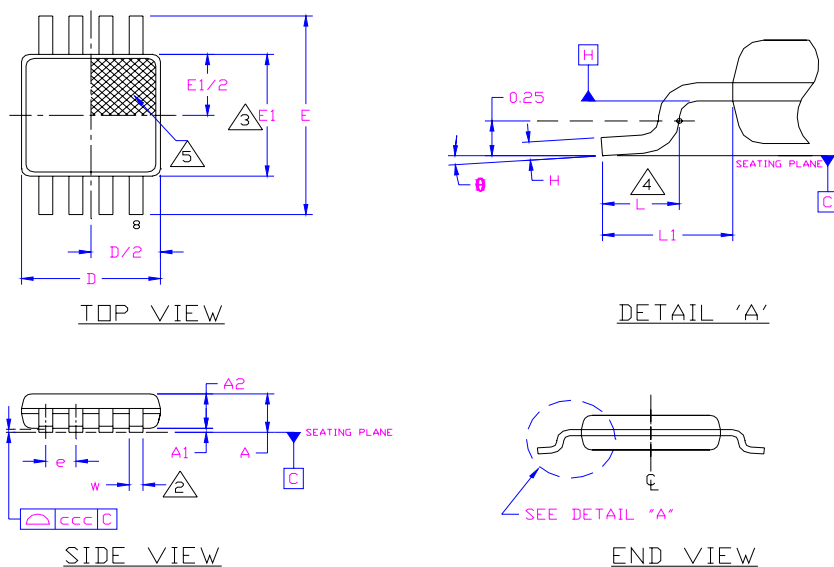
Figure 6.1 8-Pin MSOP Package Outline - 3x3mm Body 0.65mm Pitch

Table 6.1 8-Pin MSOP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	0.80	~	1.10	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	0.75	0.85	0.95	Body Thickness
D	2.80	3.00	3.20	X Body Size
E	4.65	4.90	5.15	Y Span
E1	2.80	~	3.20	Y body Size
H	0.08	~	0.23	Lead Foot Thickness
L	0.40	~	0.80	Lead Foot Length
L1	0.95 REF			Lead Length
e	0.65 BSC			Lead Pitch
θ	0°	~	8°	Lead Foot Angle
W	0.22	~	0.38	Lead Width
ccc	~	~	0.10	Coplanarity

Notes:

1. Controlling Unit: millimeters.

2. Tolerance on the true position of the leads is ± 0.065 mm maximum.

3. Package body dimensions D and E1 do not include mold protrusion or flash. Dimensions D and E1 to be determined at datum plane H. Maximum mold protrusion or flash is 0.15mm (0.006 inches) per end, and 0.15mm (0.006 inches) per side.

4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.

5. Details of pin 1 identifier are optional but must be located within the zone indicated.

6.1   Package Markings

All devices will be marked on the first line of the top side with "1043". On the second line, they will be marked with the appropriate -X number (-1, -2, etc), the Functional Revision "B" and Country Code (CC) .