CY7C65219

Dock Management Controller (DMC)

General Description

The CY7C65219-40LQXI Dock Management Controller (DMC) is a USB Billboard controller that is designed for managing USB dock and monitor solutions. The DMC provides USB full-speed capability to support USB Billboard device class v1.21. It supports signed and unsigned firmware download over USB to programmable dock components (such as USB PD Controller and Hub controller) connected to the DMC. DMC uses Cypress' proprietary M0S8 technology with a 32-bit, 48-MHz Arm® Cortex® -M0 processor with 128-KB flash, 8-KB SRAM, 20 GPIOs, full-speed USB device controller, and a Crypto engine for authentication. DMC provides system-level ESD protection. DMC is available in a 40-QFN package.

Features

Dock Management Controller

- USB-IF Certified USB 2.0 FS Silicon, TID#1534
- USB Billboard device class v1.21 support
- Firmware update support and status reporting for DMC and all programmable dock components

32-bit MCU Subsystem

- 48-MHz Arm Cortex-M0 CPU
- 128-KB Flash
- 8-KB SRAM

Integrated Digital Blocks

- Hardware Crypto block enables Authentication
- Full-Speed USB Device Controller supporting Billboard Device Class
- Integrated timers and counters
- Four run-time reconfigurable serial communication blocks (SCBs) with reconfigurable I^2C, SPI, or UART functionality

Clocks and Oscillators

- Integrated oscillator eliminating the need for external clock

Power

- 2.7 V to 5.5 V operation
- Independent supply voltage pin for GPIO that allows 1.71 V to 5.5 V signaling on the I/Os
- Reset: 30 µA, Deep Sleep: 30 µA, Sleep: 3.5 mA

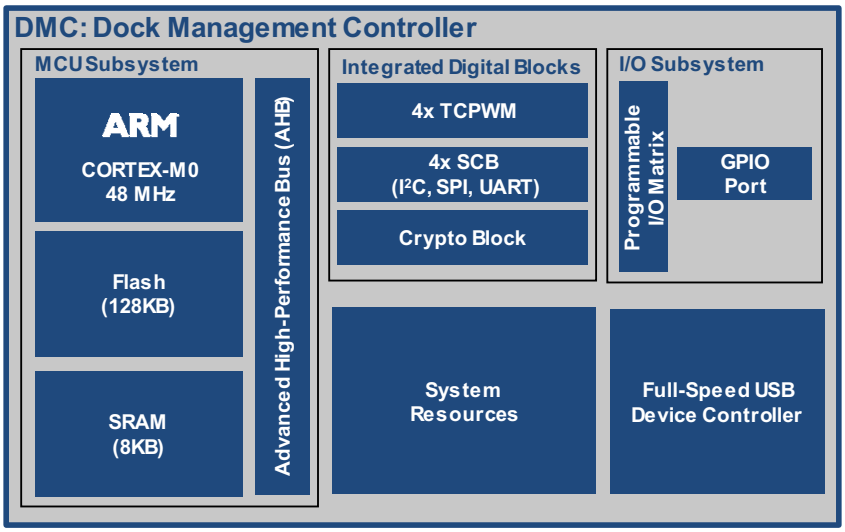
System-Level ESD Protection

- On DPLUS and DMINUS pins
- ±8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C

Packages

- 40-pin QFN for Docks/monitors
- Supports industrial temperature range (–40 °C to +85 °C)

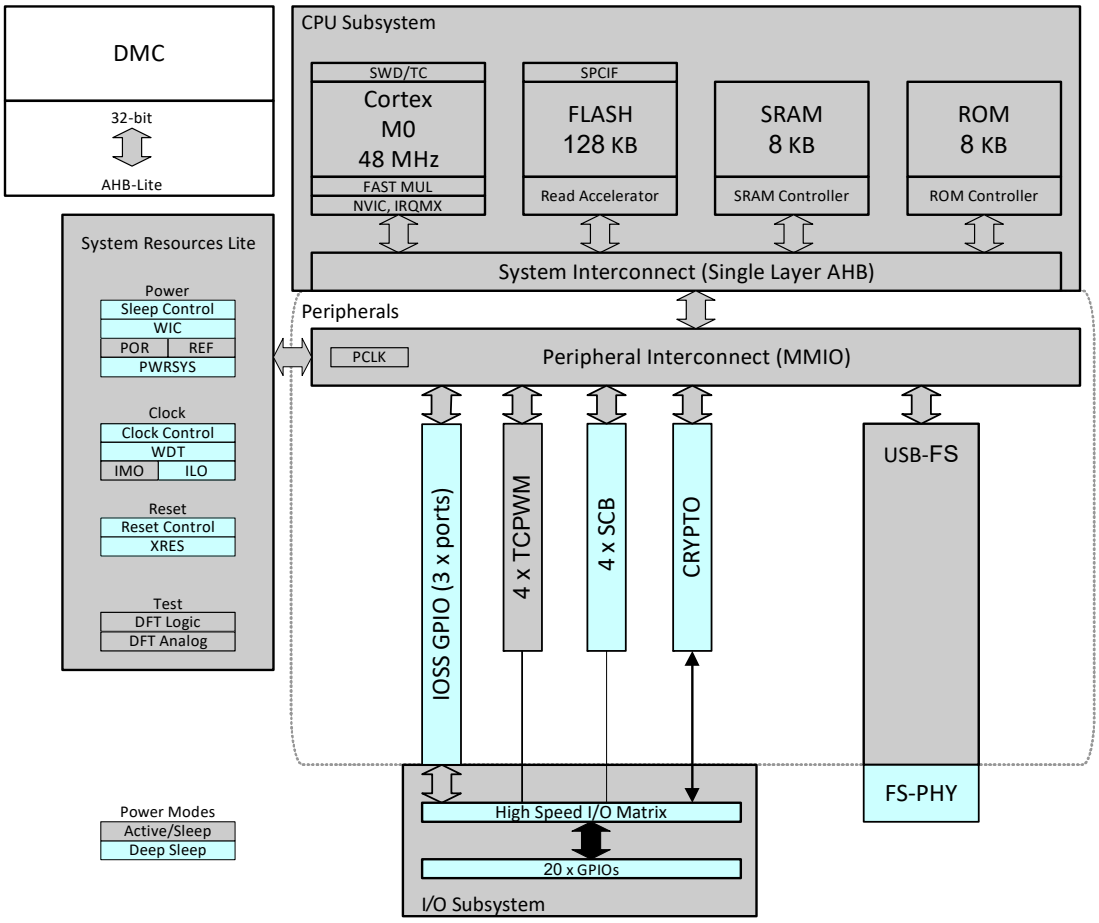
Logic Block Diagram



Contents

DMC Block Diagram

Figure 1. DMC Block Diagram[1]



Note
1. See Acronyms section for more details.

Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in DMC is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for DMC has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The DMC device has a flash module with two banks of 64 KB flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

Crypto Block

DMC integrates a crypto block for hardware assisted authentication of firmware images. The DMC Crypto block provides cryptography functionality. It includes hardware acceleration blocks for Advanced Encryption Standard (AES) block cipher, Secure Hash Algorithm (SHA-1 and SHA-2), Cyclic Redundancy Check (CRC), and pseudo random number generation.

Full-Speed USB Subsystem

The FSUSB subsystem contains a full-speed USB device controller as described in the Integrated Billboard Device section.

- USB2.0 Full-Speed (FS) PHY with integrated 5.0 V to 3.3 V regulator
- 8-kV IEC ESD Protection on the following pins: DP, DM

Integrated Billboard Device

DMC integrates a complete full-speed USB 2.0 device controller capable of functioning as a Billboard class device. The USB 2.0 device controller can also support other device classes.

Firmware Update Support

DMC has the capability to do firmware update to itself and other dock components such as USB PD Controller and Hub Controller. It implements the firmware update functionality and status reporting on a vendor interface using a full-speed USB 2.0 device controller. DMC gets the firmware update request and firmware content through the USB interface from the host. DMC communicates with dock components using SCB.

Unsigned Firmware Update

The firmware update procedure expects the host to send the metadata of the programmable component's FW information. This metadata includes SHA-256 of the individual firmware image. DMC notifies the host to send the individual component's firmware image one by one and update to the dock component connected to DMC through SCB. DMC verifies the firmware validity by comparing the received SHA-256 with the calculated SHA-256 of the firmware received.

Signed Firmware Update

The signed firmware update follows the same procedure as the unsigned firmware update but it uses RSA-2048/SHA-256 for signing.

Contact Cypress customer support for more information on the signed firmware update.

Refer to the EZ-PD™ Dock Reference Design Guide for more details.

Peripherals

Serial Communication Blocks (SCB)

DMC has four SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I^2C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^2C that creates a mailbox address range in the memory of DMC and effectively reduce I^2C communication to reading from and writing to an array in memory. In addition, the blocks support 128-deep FIFOs for receive and transmit which, by increasing the time given for the

CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripherals are compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204).

The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on SCB 1-3 blocks of DMC are not completely compliant with the I^2C specification in the following aspects:

- The GPIO cells for SCB 1's I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

DMC has four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality.

GPIO

DMC has up to 20 GPIOs (these GPIOs can be configured for GPIOs and SCB) and SWD pins, which can also be used as GPIOs. The I^2C pins from SCB 0 are overvoltage-tolerant.

The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Table 1. DMC Power Modes

Mode	Description
RESET	Power is Valid and XRES is not asserted. An internal reset source is asserted or SleepController is sequencing the system out of reset.
ACTIVE	Power is Valid and CPU is executing instructions.
SLEEP	Power is Valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most hard-IPs are shut off. Deep Sleep regulator powers logic, but only low-frequency clock is available.

Pinouts

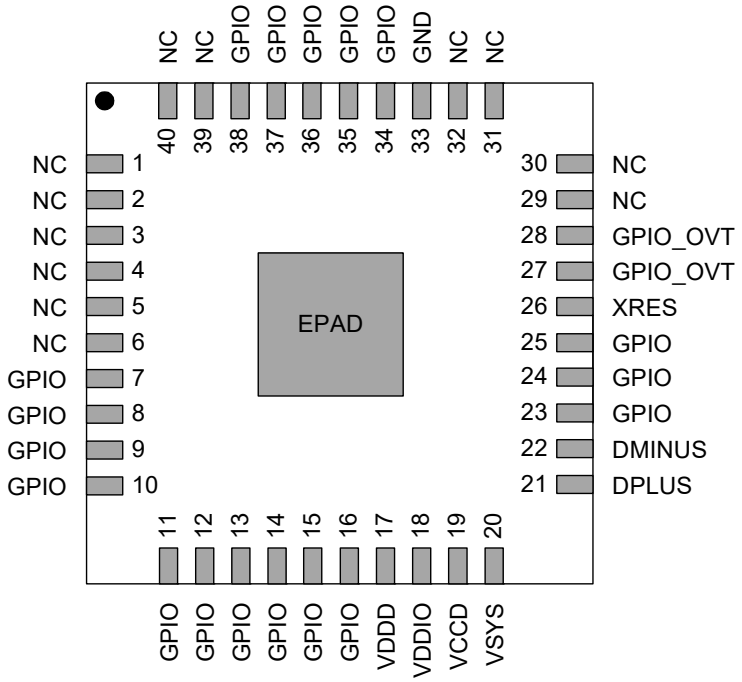
Table 2. DMC Pin Description for 40-QFN Device

Pin Map 40-QFN	Name	Description
1	NC	NC
2	NC	NC
3	NC	NC
4	NC	NC
5	NC	NC
6	NC	NC
7	P1.0	GPIO/UART_2_TX / SPI_2_MISO
8	P1.1	GPIO/UART_2_RX / SPI_2_SEL
9	P1.2	GPIO/UART_0_RX/ UART_3_CTS/ SPI_3_MOSI/ I2C_3_SCL
10	P1.3	GPIO/UART_0_TX/ UART_3_RTS/ SPI_3_CLK/ I2C_3_SDA
11	P1.6	GPIO / UART_1_TX / SPI_1_MISO
12	P1.4	GPIO / UART_3_TX/ SPI_3_MISO/ SWD_1_CLK
13	P1.5	GPIO / UART_3_RX/ SPI_3_SEL/ SWD_1_DAT
14	P1.7	GPIO / UART_1_RX / SPI_1_SEL
15	P2.0	GPIO / UART_1_CTS / SPI_1_CLK/ I2C_1_SCL / SWD_0_DAT
16	P2.1	GPIO / UART_1_RTS / SPI_1_MOSI/ I2C_1_SDA / SWD_0_CLK
17	VDDD	VDDD supply Input / Output (2.7 V–5.5 V)
18	VDDIO	1.71 V–5.5 V supply for I/Os. This supply also powers the global analog multiplex buses.
19	VCCD	1.8-V regulator output for filter capacitor
20	VSYS	System power supply (2.7 V–5.5 V)
21	DPLUS	USB 2.0 DP
22	DMINUS	USB 2.0 DM
23	P2.4	GPIO
24	P2.5	GPIO / UART_0_TX/ SPI_0_MOSI
25	P2.6	GPIO / UART_0_RX/ SPI_0_CLK
26	XRES	External Reset Input. Internally pulled-up to VDDIO.
27	P0.0	I2C_0_SDA / GPIO_OVT / UART_0_CTS / SPI_0_SEL/ TCPWM0
28	P0.1	I2C_0_SCL / GPIO_OVT / UART_0_RTS / SPI_0_MISO/ TCPWM1
29	NC	NC
30	NC	NC
31	NC	NC
32	NC	NC
33	VSS	Ground Supply (GND)
34	P3.2	GPIO / TCPWM0
35	P3.3	GPIO / TCPWM1
36	P3.4	GPIO / UART_2_CTS / SPI_2_MOSI/ I2C_2_SDA / TCPWM2
37	P3.5	GPIO / UART_2_RTS / SPI_2_CLK/ I2C_2_SCL / TCPWM3
38	P3.6	GPIO

Table 2. DMC Pin Description for 40-QFN Device *(continued)*

Pin Map 40-QFN	Name	Description
39	NC	NC
40	NC	NC

Figure 2. Pinout of 40-QFN Package (Top View)



Available Firmware and Software Tools

EZ-PD Dock DMC Configuration Generation Tool

The EZ-PD Dock DMC Configuration Generation Tool can be used to update DMC images with the modified configuration. It allows configuring the dock topology to manage and do firmware update to programmable dock components connected to DMC.

EZ-PD Dock Image Creation Tool

The EZ-PD Dock Image Creation Tool is used to create a single combined firmware image file, referred to as the composite dock image from firmware files of components present in the dock. This composite image is used for firmware update to be used by EZ-PD Dock Firmware Update Tool.

EZ-PD Dock Firmware Update Tool

The EZ-PD Dock Firmware Update Tool is a WinUSB-based application that runs on Windows systems. This tool updates firmware for devices in the dock and reports the final consolidated status. It takes the files generated using the EZ-PD Dock Image Creation Tool as the input and initiates a firmware update.

You can download the EZ-PD Dock DMC Configuration Generation Tool, EZ-PD Dock Image Creation Tool, EZ-PD Dock Firmware Update Tool and its associated documentation at the following link:

http://www.cypress.com/documentation/reference-designs/ez-pd-ccg4-usb-type-c-monitordock-solution

DMC Programming

There are two ways to program application firmware into a DMC device:

1. Programming the device flash over SWD Interface
2. Application firmware update over an USB interface

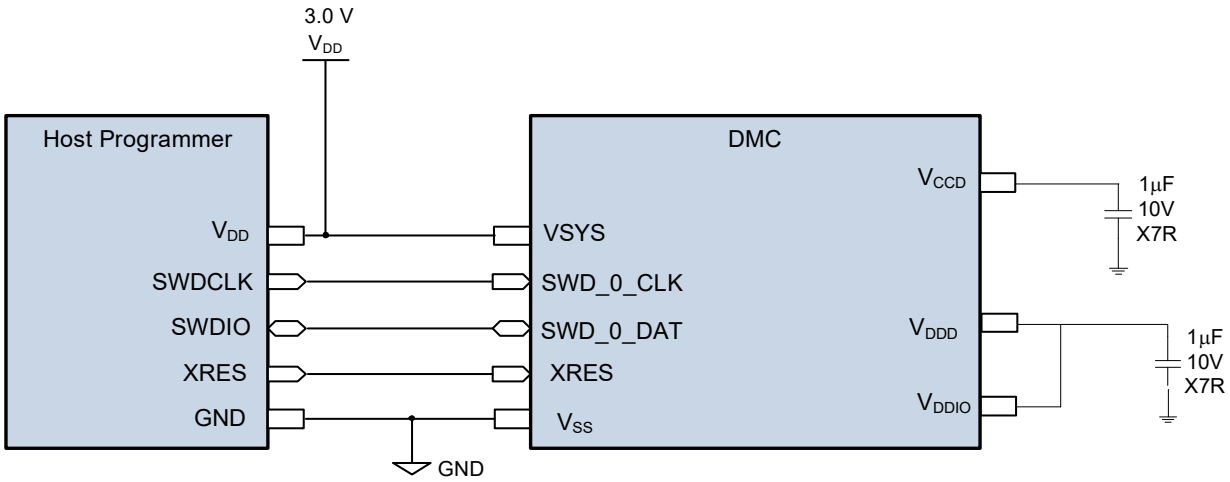
Generally, the DMC device is programmed over the SWD interface only during development or during the manufacturing process of the end product. Once the end product is manufactured, the DMC device's application firmware can be updated via the USB interface running on the alternate application image.

Programming the Device Flash over SWD Interface

The DMC device can be programmed using the SWD interface. Cypress provides a programming kit (CY8CKIT-002 MiniProg3 Kit) called MiniProg3, which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file. This hex file is a binary file generated as an output of building the firmware project in PSoC Creator Software. Click here for more information on how to use the MiniProg3 programmer. There are many third-party programmers that support mass programming in a manufacturing environment.

As shown in the block diagram in Figure 3, the SWD_0_DAT and SWD_0_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the device can be powered by the host programmer by connecting its VTARG (power supply to the target device) to VSYS pin of the DMC device. If the DMC device is powered using an on-board power supply, it can be programmed using the “Reset Programming” option.

Figure 3. Connecting the Programmer to DMC Device

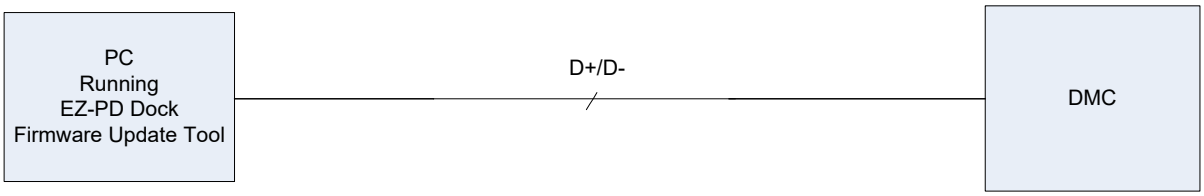


Application Firmware Update over USB Interface

The application firmware provided by Cypress for all DMC applications have dual images. Application firmware can only be updated using other copy of application firmware over the USB vendor interface that binds to the Microsoft WinUSB driver. This allows fail-safe update of the alternate image while executing from the current image. For more information, refer to the EZ-PD Dock Reference Design Guide.

In this application, the firmware update can be performed over the D+/D- lines (USB2.0) as shown in Figure 4.

Figure 4. Application Firmware Update



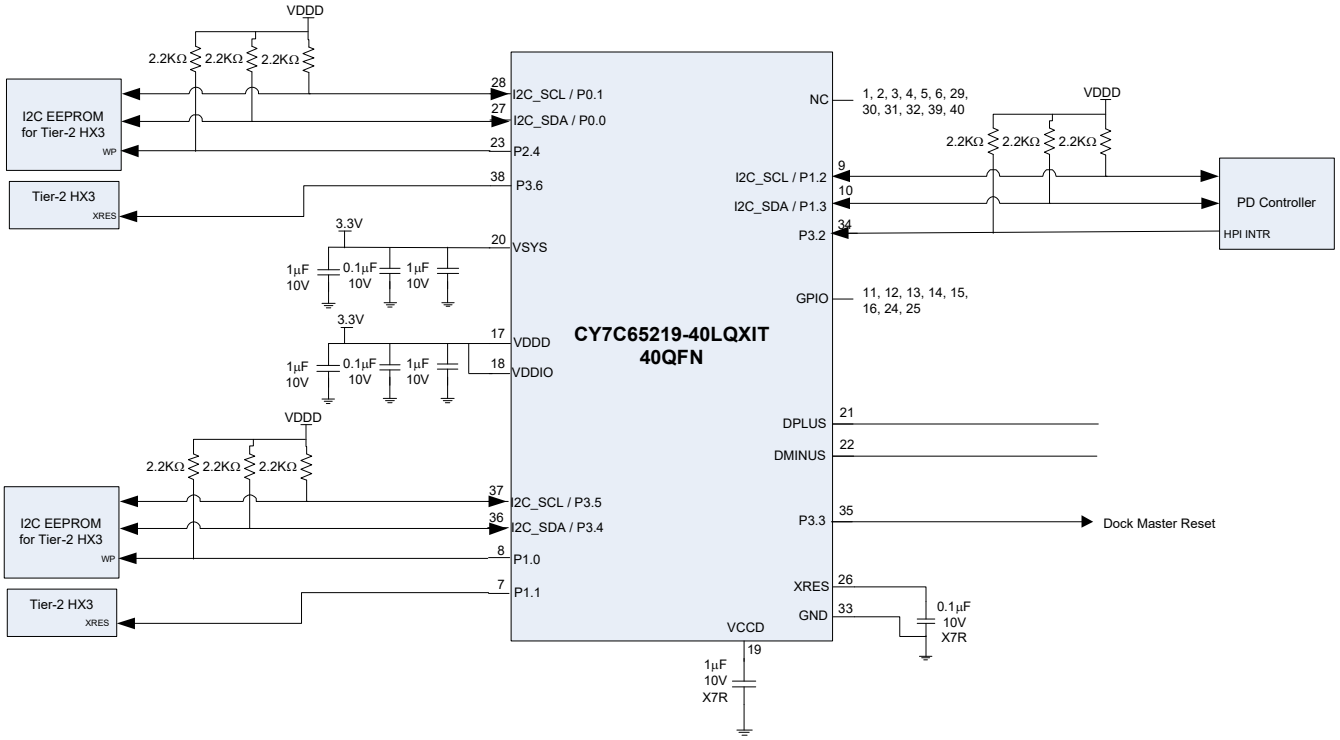
Applications

Figure 5 illustrates the application diagram of a dock/monitor using a DMC device. In this application, DMC is used as Billboard and Firmware Update device for all programmable dock components.

A typical dock/monitor application also includes a PD controller for Type-C ports and Hub for port expansion. DMC is connected to the PD controller and Hub controller through SCB (in this case I^2C interface) and GPIOs. DMC communicates with the PD controller and Hub controller and provides their status. It also enables firmware update over the SCB interface.

More details including the schematic of the EZ-PD Dock Reference Design can be found here.

Figure 5. Dock/Monitor Application Diagram (40-QFN Device)



Electrical Specifications

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{SYS_MAX}	Digital supply relative to V_{SS}	–0.5	–	6	V	Absolute max
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDIO} + 0.5	V	
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage	–0.5	–	6	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
$I_{GPIO\_INJECTION}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–100	–	100	mA	Tested at 125 °C
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on DPLUS, DMINUS pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for DPLUS, DMINUS pins

Device-Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted.

Table 4. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PWR#1	V_{SYS}	–	2.7	–	5.5	V	
SID.PWR#13	V_{DDIO}	I/O supply voltage	1.71	–	5.5[2]	V	2.7 V < V_{DDD} < 5.5 V
SID.PWR24	V_{CCD}	Output voltage for core Logic	–	1.8	–	V	–
SID.PWR#4	I_{DD}	Supply current	–	25	–	mA	From V_{SYS} T_A = 25 °C / V_{SYS} = 5 V, T_A = 25 °C FS USB, no I/O sourcing current, 2 SCBs at 1 Mbps, CPU at 24 MHz.
SID.PWR#1_B	V_{SYS}	Power supply for USB operation	4.5	–	5.5	V	USB configured, USB Regulator enabled
SID.PWR#1_C	V_{SYS}	Power supply for USB operation	3.15	–	3.45	V	USB configured, USB Regulator disabled
SID.PWR#15	C_{efc}	External regulator voltage bypass for V_{CCD}	1	1.3	1.6	µF	X5R ceramic or better
SID.PWR#16	C_{exc}	Power supply decoupling capacitor for V_{SYS}	0.8	1	–	µF	X5R ceramic or better
Sleep Mode. VSYS = 2.7 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V and TA = 25 °C.							
SID25A	I_{DD20A}	WDT wakeup on. IMO at 48 MHz.	–	3.5	–	mA	V_{SYS} = 3.3 V, T_A = 25 °C, All blocks except CPU are on, USB in Suspend Mode, no I/O sourcing current
Deep Sleep Mode							
SID_DS	I_{DD_DS}	V_{SYS} = 3.0 to 3.6 V. CC Attach, I^2C, WDT Wakeup on.	–	30	–	µA	Power Source = V_{SYS}, I^2C and WDT enabled for Wakeup.
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted. This does not include current drawn due to the XRES internal pull-up resistor.	–	30	–	µA	Power Source = V_{SYS} = 3.3 V, T_A = 25 °C

Table 5. AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#4	F_{CPU}	CPU input frequency	DC	–	48	MHz	All V_{DDD}
SID.PWR#20	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	–
SID.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	All V_{DDIO}

Note
2. If V_{DDIO} > V_{DDD}, GPIO P2.4 cannot be used. It must be left unconnected. See Table 2 for pin numbers.

I/O

Table 6. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.GIO#39	$V_{IH\_VDDIO2.7-}$	LVTTL input, V_{DDIO} < 2.7 V	0.7× V_{DDIO}	–	–	V	–
SID.GIO#40	$V_{IL\_VDDIO2.7-}$	LVTTL input, V_{DDIO} < 2.7 V	–	–	0.3 × V_{DDIO}	V	–
SID.GIO#41	$V_{IH\_VDDIO2.7+}$	LVTTL input, $V_{DDIO} \geq$ 2.7 V	2.0	–	–	V	–
SID.GIO#42	$V_{IL\_VDDIO2.7+}$	LVTTL input, $V_{DDIO} \geq$ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH_3V}	Output voltage HIGH level	V_{DDIO}–0.6	–	–	V	I_{OH} = 4 mA at 3-V V_{DDIO}
SID.GIO#34	$V_{OH\_1.8V}$	Output voltage HIGH level	V_{DDIO}–0.5	–	–	V	I_{OH} = 1 mA at 1.8-V V_{DDIO}
SID.GIO#35	$V_{OL\_1.8V}$	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DDIO}
SID.GIO#36	V_{OL_3V}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 3-V V_{DDIO} for SBU and AUX pins
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all V_{DDIO}
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all V_{DDIO}
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T_A, all V_{DDIO}. Guaranteed by characterization.
SID.GIO#17	C_{PIN}	Max pin capacitance	–	3.0	7	pF	All V_{DDIO}, all packages, all I/Os. Guaranteed by characterization.
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL VDDIO > 2.7 V	15	40	–	mV	Guaranteed by characterization
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × VDDIO	–	–	mV	V_{DDIO} < 4.5 V. Guaranteed by characterization.
SID69	I_{DIODE}	Current through protection diode to VDDIO/Vss	–	–	100	µA	Guaranteed by characterization
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	Guaranteed by characterization
OVT							
SID.GIO#46	I_{IHS}	Input current when Pad > VDDIO for OVT inputs	–	–	10.00	µA	Per I^2C specification

Table 7. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3 V V_{DDIO}, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3 V V_{DDIO}, C_{load} = 25 pF

XRES

Table 8. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.XRES#1	V_{IH_XRES}	Input voltage HIGH threshold on XRES pin	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.XRES#2	V_{IL_XRES}	Input voltage LOW threshold on XRES pin	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.XRES#3	C_{IN_XRES}	Input capacitance on XRES pin	–	–	7	pF	Guaranteed by characterization
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin	–	0.05 × V_{DDIO}	–	mV	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 9. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature-phase inputs

I²C

Table 10. Fixed I²C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	60	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	185	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
SID152	I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 11. Fixed I²C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

Table 12. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	125	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312	µA	–

Table 13. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 14. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mbps	–	–	560	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mbps	–	–	600	µA	–

Table 15. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F_{SPI}	SPI Operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 16. Fixed SPI Master Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO Valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to slave capturing edge

Table 17. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID170	T_{DMI}	MOSI Valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO Valid after Sclock driving edge	–	–	$42 + 3 \times T_{CPU}$	ns	$T_{CPU} = 1/F_{CPU}$
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	–

System Resources

Power-on-Reset (POR) with Brown Out SWD Interface

Table 18. Imprecise Power On Reset (PRES) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Power-on Reset (POR) rising trip voltage	0.80	–	1.50	V	–
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4	V	–

Table 19. Precise Power On Reset (POR) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	Brown-out Detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	–

Table 20. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SWD#1	F_SWDCLK1	$3.3\ V \le V_{DDIO} \le 5.5\ V$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	$1.8\ V \le V_{DDIO} \le 3.3\ V$	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T	ns	Guaranteed by characterization
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 21. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–

Table 22. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	–25 °C ≤ T_A ≤ 85 °C, all V_{DDD}
SID226	$T_{STARTIMO}$	IMO start-up time	–	–	7	µs	Guaranteed by characterization
SID229	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	Guaranteed by characterization
SID.CLK#1	F_{IMO}	IMO frequency	24	–	48	MHz	All V_{DDD}

Internal Low-Speed Oscillator

Table 23. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	I_{LO} operating current	–	0.3	1.05	µA	–
SID233	$I_{ILOLEAK}$	I_{LO} leakage current	–	2	15	nA	–

Table 24. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	I_{LO} start-up time	–	–	2	ms	Guaranteed by characterization
SID238	$T_{ILODUTY}$	I_{LO} duty cycle	40	50	60	%	Guaranteed by characterization
SID.CLK#5	F_{ILO}	I_{LO} frequency	20	40	80	kHz	–

Table 25. VSYS Switch Specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.vddsw.1	Res_sw	Resistance from V_{SYS} supply input to the output supply V_{DDD}	–	–	1.5	Ω	Measured with a load current of 5 mA–10 mA on V_{DDD}.

Memory

Table 26. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.MEM#3	FLASH_ERASE	Row erase time	–	–	15.5	ms	–
SID.MEM#4	FLASH_WRITE	Row (Block) write time (erase and program)	–	–	20	ms	–
SID.MEM#8	FLASH_ROW_PGM	Row program time after erase	–	–	7	ms	–
SID178	$T_{BULKERASE}$	Bulk erase time (64 KB)	–	–	35	ms	–
SID180	$T_{DEVPROG}$	Total device program time	–	–	7.5	s	Guaranteed by characterization
SID182	F_{RET1}	Flash retention, $T_A \le 55$ °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A	F_{RET2}	Flash retention, $T_A \le 85$ °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	F_{RET3}	Flash retention, $T_A \le 105$ °C, 10 K P/E cycles	3	–	–	years	Guaranteed by characterization

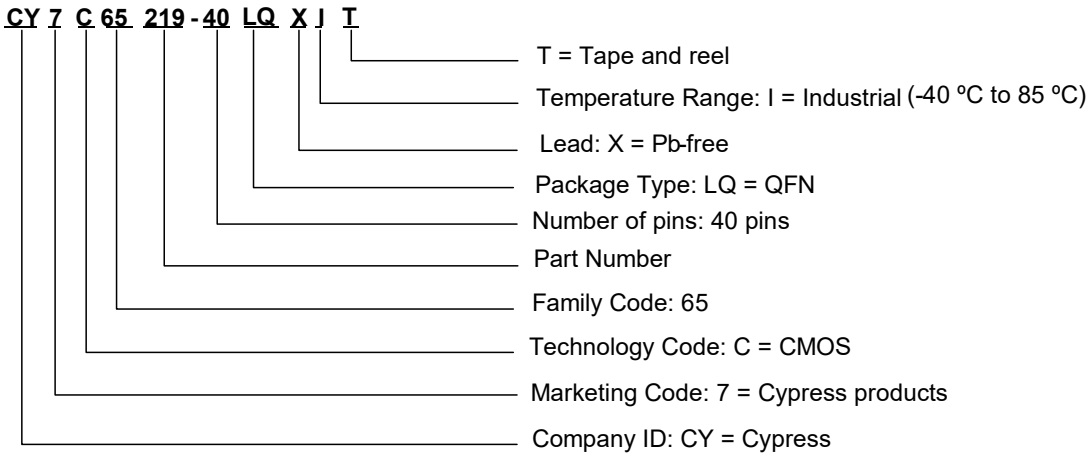
Ordering Information

Table 27 lists the DMC part numbers and features.

Table 27. DMC Ordering Information

Part Number	Application	Default FW	Package	Si ID
CY7C65219-40LQXIT	Docks/Monitors	Application launcher and 2 copies of application FW that can update DMC as unsigned firmware update	40-QFN	1D0A
CY7C65219-40LQXI				

Ordering Code Definitions



Packaging

Table 28. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	Industrial	–40	25	85	°C
T_J	Operating junction temperature	Industrial	–40	25	100	°C
T_{JA}	Package θ_{JA} (40-pin QFN)	–	–	–	17	°C/W
T_{JC}	Package θ_{JC} (40-pin QFN)	–	–	–	2	°C/W

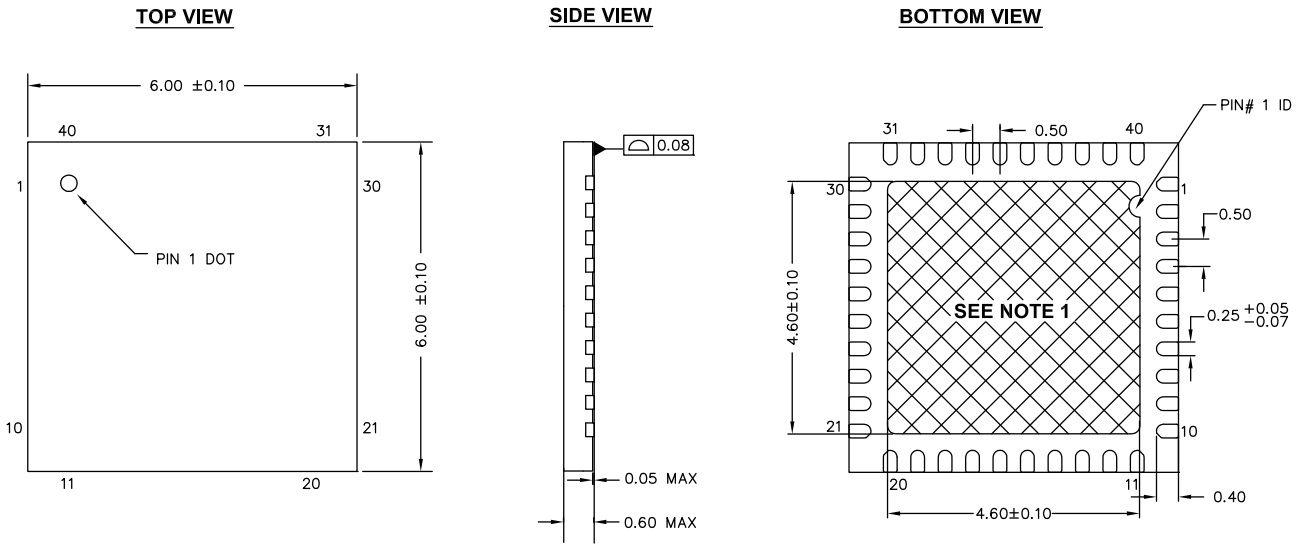
Table 29. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
40-pin QFN	260 °C	30 seconds

Table 30. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
40-pin QFN	MSL 3

Figure 6. 40-pin QFN Package Outline, 001-80659



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

Acronyms

Table 31. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
AES	advanced encryption standard
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
ESD	electrostatic discharge
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
IOSS	input/output subsystem
I/O	input/output, see also GPIO
LDO	low-dropout regulator
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
MMIO	memory mapped input/output
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
opamp	operational amplifier
PCB	printed circuit board

Table 31. Acronyms Used in this Document *(continued)*

Acronym	Description
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCB	serial communication block
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SHA	secure hash algorithm
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TCPWM	timer/counter pulse-width modulator
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USB PD	USB Power Delivery
USB-FS	USB Full-Speed
USBIO	USB input/output, CCG2 pins used to connect to a USB port
VDM	vendor defined messages
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 32. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

References and Links to Applications Collaterals

Knowledge Base Articles

- Key Differences Among EZ-PD™ CCG1, CCG2, CCG3 and CCG4 - KBA210740
- Programming EZ-PD™ CCG2, EZ-PD™ CCG3 and EZ-PD™ CCG4 Using PSoC® Programmer and MiniProg3 - KBA96477
- CCGX Frequently Asked Questions (FAQs) - KBA97244
- Handling Precautions for CY4501 CCG1 DVK - KBA210560
- Cypress EZ-PD™ CCGx Hardware - KBA204102
- Difference between USB Type-C and USB-PD - KBA204033
- CCGx Programming Methods - KBA97271
- Getting started with Cypress USB Type-C Products - KBA04071
- Type-C to DisplayPort Cable Electrical Requirements
- Dead Battery Charging Implementation in USB Type-C Solutions - KBA97273
- Termination Resistors Required for the USB Type-C Connector – KBA97180
- VBUS Bypass Capacitor Recommendation for Type-C Cable and Type-C to Legacy Cable/Adapter Assemblies – KBA97270
- Need for Regulator and Auxiliary Switch in Type-C to DisplayPort (DP) Cable Solution - KBA97274
- Need for a USB Billboard Device in Type-C Solutions – KBA97146
- CCG1 Devices in Type-C to Legacy Cable/Adapter Assemblies – KBA97145
- Cypress USB Type-C Controller Supported Solutions – KBA97179
- Termination Resistors for Type-C to Legacy Ports – KBA97272
- Handling Instructions for CY4502 CCG2 Development Kit – KBA97916
- Thunderbolt™ Cable Application Using CCG3 Devices - KBA210976
- Power Adapter Application Using CCG3 Devices - KBA210975
- Methods to Upgrade Firmware on CCG3 Devices - KBA210974
- Device Flash Memory Size and Advantages - KBA210973
- Applications of EZ-PD™ CCG4 - KBA210739

Application Notes

- AN96527 - Designing USB Type-C Products Using Cypress's CCG1 Controllers
- AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2
- AN95599 - Hardware Design Guidelines for EZ-PD™ CCG2
- AN210403 - Hardware Design Guidelines for Dual Role Port Applications Using EZ-PD™ USB Type-C Controllers
- AN210771 - Getting Started with EZ-PD™ CCG4

Reference Designs

- EZ-PD™ CCG2 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- EZ-PD™ CCG2 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to HDMI/DVI/VGA Adapter Solution
- EZ-PD™ CCG2 USB Type-C to HDMI Adapter Solution
- CCG1 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- CCG1 USB Type-C to Legacy USB Device Cable Paddle Card Reference Schematics
- EZ-USB GX3 USB Type-C to Gigabit Ethernet Dongle
- EZ-PD™ CCG2 USB Type-C Monitor/Dock Solution
- CCG2 20W Power Adapter Reference Design
- CCG2 18W Power Adapter Reference Design
- EZ-USB GX3 USB Type-A to Gigabit Ethernet Reference Design Kit
- EZ-PD Dock Reference Design

Kits

- CY4501 CCG1 Development Kit
- CY4502 EZ-PD™ CCG2 Development Kit
- CY4531 EZ-PD CCG3 Evaluation Kit
- CY4541 EZ-PD™ CCG4 Evaluation Kit

Datasheets

- CCG1 Datasheet: USB Type-C Port Controller with Power Delivery
- CYPD1120 Datasheet: USB Power Delivery Alternate Mode Controller on Type-C
- CCG2: USB Type-C Port Controller Datasheet
- CCG4: Two-Port USB Type-C Controller Datasheet

Document History Page

Document Title: CY7C65219, Dock Management Controller (DMC) Document Number: 002-20954				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*A	6002250	MUTH	12/21/2017	Initial release. Changed datasheet status to Final.
*B	6592100	MUTH	06/10/2019	Added “USB-IF Certified USB 2.0 FS Silicon, TID#1534” in Features. Updated Copyright information.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

IMPORTANT NOTE REGARDING PROTECTED FIRMWARE DOWNLOAD: Cypress has implemented protections in the product to prevent unauthorized firmware updates from being applied to the product. However, no computing device or system can be absolutely secure. Therefore, the parties agree that Cypress shall not have any liability arising out of any failure of the product's security features, such as the inability to load firmware or a breach allowing the loading of unauthorized firmware.

Notice regarding compliance with Universal Serial Bus specification. Cypress offers firmware and hardware solutions that are certified to comply with the Universal Serial Bus specification, USB Type-C™ Cable and Connector Specification, and other specifications of USB Implementers Forum, Inc (USB-IF). You may use Cypress or third party software tools, including sample code, to modify the firmware for Cypress USB products. Modification of such firmware could cause the firmware/hardware combination to no longer comply with the relevant USB-IF specification. You are solely responsible ensuring the compliance of any modifications you make, and you must follow the compliance requirements of USB-IF before using any USB-IF trademarks or logos in connection with any modifications you make. In addition, if Cypress modifies firmware based on your specifications, then you are responsible for ensuring compliance with any desired standard or specifications as if you had made the modification. CYPRESS IS NOT RESPONSIBLE IN THE EVENT THAT YOU MODIFY OR HAVE MODIFIED A CERTIFIED CYPRESS PRODUCT AND SUCH MODIFIED PRODUCT NO LONGER COMPLIES WITH THE RELEVANT USB-IF SPECIFICATIONS.