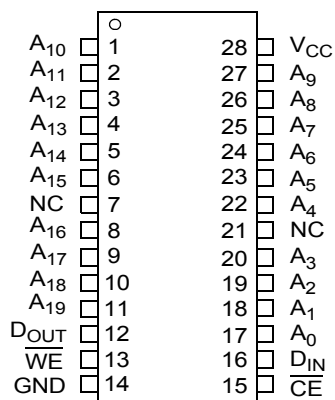


## Contents

<b>Pin Configuration .....</b>	<b>3</b>	<b>Ordering Information .....</b>	<b>10</b>
<b>Selection Guide .....</b>	<b>3</b>	Ordering Code Definitions .....	10
<b>Maximum Ratings .....</b>	<b>4</b>	<b>Package Diagrams .....</b>	<b>11</b>
<b>Operating Range .....</b>	<b>4</b>	<b>Acronyms .....</b>	<b>13</b>
<b>Electrical Characteristics .....</b>	<b>4</b>	<b>Document Conventions .....</b>	<b>13</b>
<b>Capacitance .....</b>	<b>5</b>	Units of Measure .....	13
<b>Thermal Resistance .....</b>	<b>5</b>	<b>Document History Page .....</b>	<b>14</b>
<b>AC Test Loads and Waveforms .....</b>	<b>5</b>	<b>Sales, Solutions, and Legal Information .....</b>	<b>15</b>
<b>Data Retention Characteristics .....</b>	<b>6</b>	Worldwide Sales and Design Support .....	15
<b>Data Retention Waveform .....</b>	<b>6</b>	Products .....	15
<b>Switching Characteristics .....</b>	<b>7</b>	PSoC® Solutions .....	15
<b>Switching Waveforms .....</b>	<b>8</b>	Cypress Developer Community .....	15
<b>Truth Table .....</b>	<b>10</b>	Technical Support .....	15

## Pin Configuration

Figure 1. 28-pin SOJ pinout (Top View) <sup>[2]</sup>



## Selection Guide

Description	CY7C107D-10 CY7C1007D-10	Unit
Maximum access time	10	ns
Maximum operating current	80	mA
Maximum CMOS standby current, I <sub>SB2</sub>	3	mA

### Note

- NC pins are not connected on the die.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  relative to GND <sup>[3]</sup> ..... -0.5 V to +6.0 V

DC voltage applied to outputs in High-Z state <sup>[3]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage <sup>[3]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$	Speed
Industrial	-40 °C to +85 °C	5 V $\pm$ 0.5 V	10 ns

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		7C107D-10 7C1007D-10		Unit
				Min	Max	
V <sub>OH</sub>	Output HIGH voltage	I <sub>OH</sub> = −4.0 mA		2.4	–	V
		I <sub>OH</sub> = −0.1 mA		–	3.4 <sup>[4]</sup>	
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 8.0 mA		–	0.4	V
V <sub>IH</sub>	Input HIGH voltage			2.2	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW voltage <sup>[3]</sup>			−0.5	0.8	V
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		−1	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , output disabled		−1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>max</sub> = 1/t <sub>RC</sub>	100 MHz	–	80	mA
			83 MHz	–	72	mA
			66 MHz	–	58	mA
			40 MHz	–	37	mA
I <sub>SB1</sub>	Automatic $\overline{\text{CE}}$ Power-down current – TTL Inputs	Max V <sub>CC</sub> , $\overline{\text{CE}} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>max</sub>		–	10	mA
I <sub>SB2</sub>	Automatic $\overline{\text{CE}}$ Power-down current – CMOS Inputs	Max V <sub>CC</sub> , $\overline{\text{CE}} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0		–	3	mA

### Note

3.  $V_{IL}$  (min) = -2.0 V and  $V_{IH}$  (max) =  $V_{CC} + 1$  V for pulse durations of less than 5 ns.

4. Please note that the maximum  $V_{OH}$  limit does not exceed minimum CMOS  $V_{IH}$  of 3.5V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum  $V_{IH}$  of 3.5 V, please refer to Application Note [AN6081](#) for technical details and options you may consider.

## Capacitance

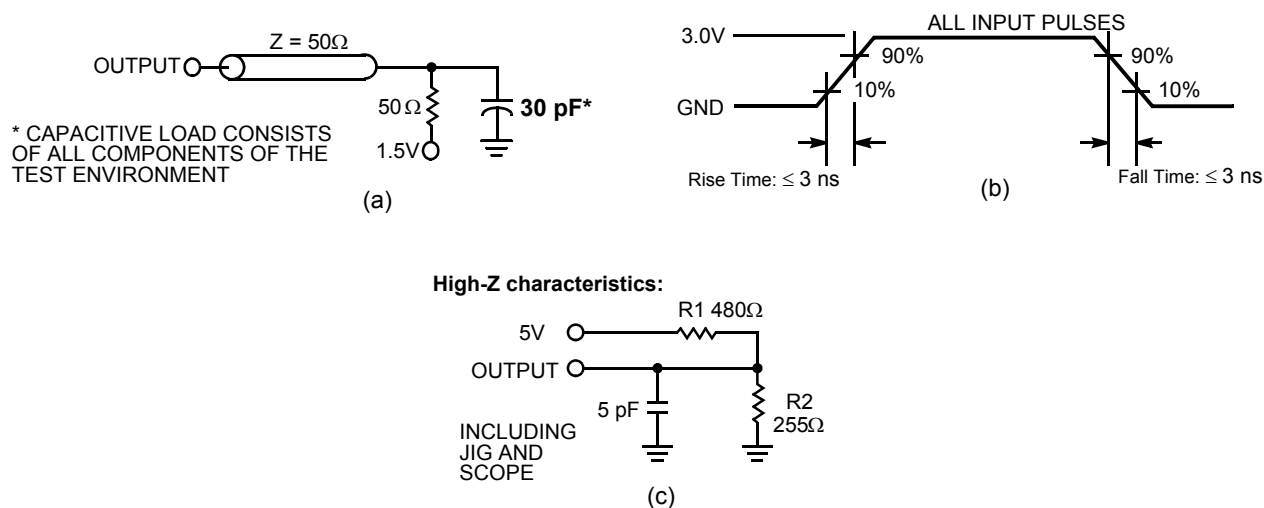
Parameter <sup>[5]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub> : Addresses	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 5.0 V	7	pF
C <sub>IN</sub> : Controls			10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

## Thermal Resistance

Parameter <sup>[5]</sup>	Description	Test Conditions	300-Mil Wide SOJ	400-Mil Wide SOJ	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.16	58.76	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		40.84	40.54	°C/W

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms <sup>[6]</sup>



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High-Z) are tested using the load conditions shown in Figure 2 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

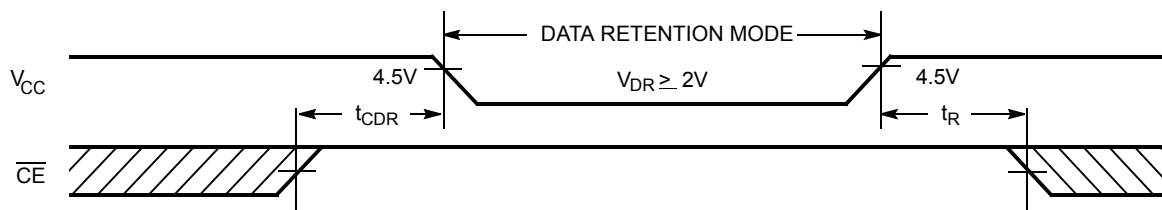
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		2.0	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	3	mA
$t_{CDR}^{[7]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[8]}$	Operation recovery time		$t_{RC}$	–	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

- AC characteristics (except High-Z) are tested using the load conditions shown in Figure 2 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).
- Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 50\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 50\text{ }\mu\text{s}$ .

## Switching Characteristics

Over the Operating Range

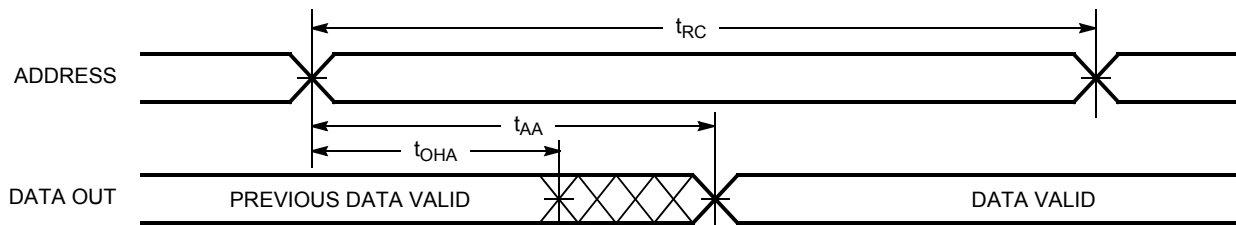
Parameter <sup>[9]</sup>	Description	7C107D-10 7C1007D-10		Unit
		Min	Max	
Read Cycle				
t <sub>power</sub> <sup>[10]</sup>	V <sub>CC</sub> (typical) to the first access	100	–	μs
t <sub>RC</sub>	Read cycle time	10	–	ns
t <sub>AA</sub>	Address to data valid	–	10	ns
t <sub>OHA</sub>	Data hold from address change	3		ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to data valid	–	10	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to Low Z <sup>[11]</sup>	3	–	ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to High Z <sup>[11, 12]</sup>	–	5	ns
t <sub>PU</sub> <sup>[13]</sup>	$\overline{\text{CE}}$ LOW to power-up	0	–	ns
t <sub>PD</sub> <sup>[13]</sup>	$\overline{\text{CE}}$ HIGH to power-down	–	10	ns
Write Cycle <sup>[14]</sup>				
t <sub>WC</sub>	Write cycle time	10	–	ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to write end	7	–	ns
t <sub>AW</sub>	Address set-up to write end	7	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address set-up to write start	0	–	ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ pulse width	7	–	ns
t <sub>SD</sub>	Data set-up to write end	6	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to Low Z <sup>[11]</sup>	3	–	ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to High Z <sup>[11, 12]</sup>	–	6	ns

### Notes

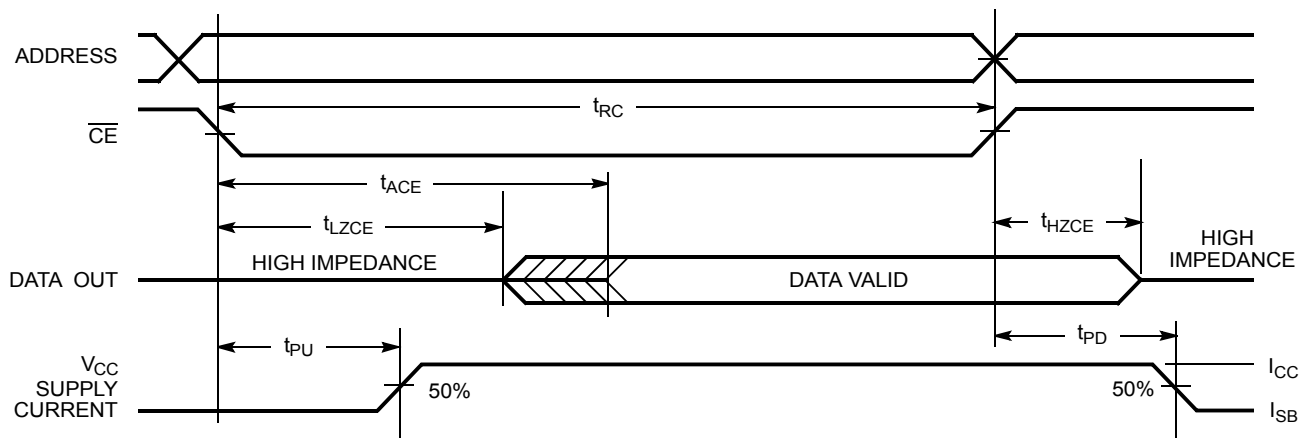
9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{\text{OL}}/I_{\text{OH}}$  and 30-pF load capacitance.
10.  $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at typical  $V_{\text{CC}}$  values until the first memory access can be performed.
11. At any given temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$  and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any given device.
12.  $t_{\text{HZCE}}$  and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (c) of [Figure 2 on page 5](#). Transition is measured when the outputs enter a high impedance state.
13. This parameter is guaranteed by design and is not tested.
14. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

## Switching Waveforms

**Figure 4. Read Cycle No. 1 (Address Transition Controlled)** <sup>[15, 16]</sup>



**Figure 5. Read Cycle No. 2** <sup>[16, 17]</sup>



### Notes

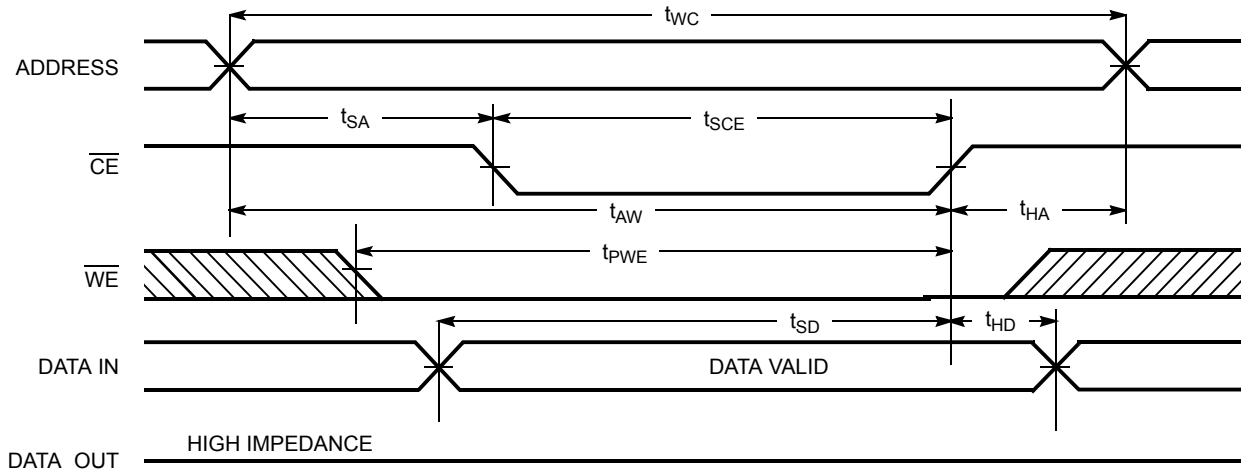
15. Device is continuously selected,  $\overline{CE} = V_{IL}$ .

16.  $\overline{WE}$  is HIGH for read cycle.

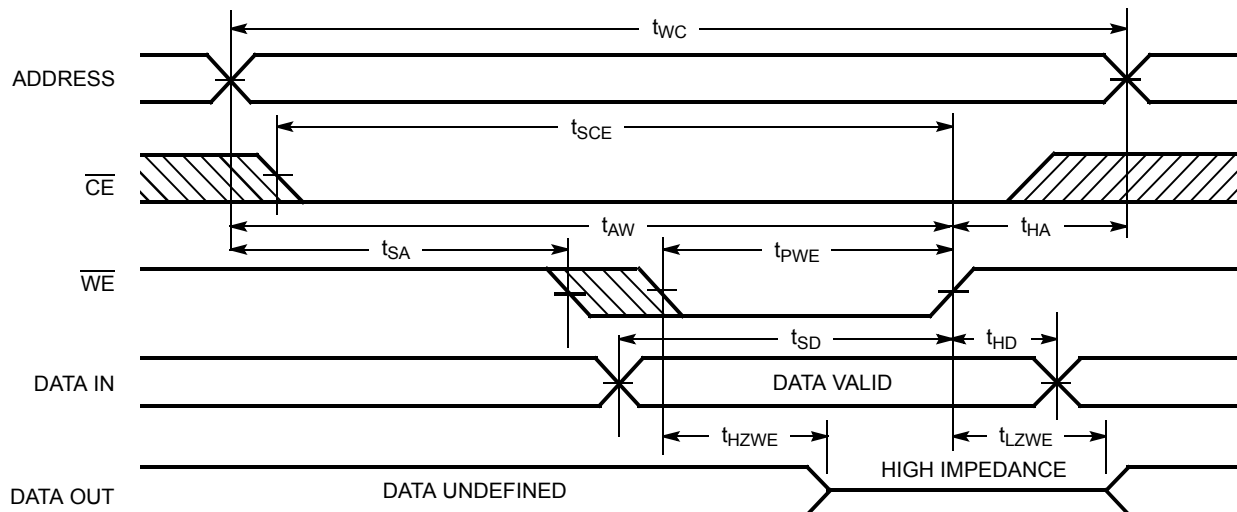
17. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

## Switching Waveforms(continued)

**Figure 6. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [18]**



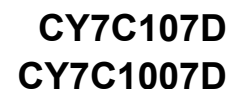
**Figure 7. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled) [18]**



### Note

18. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.





$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\text{D}_{\text{OUT}}$	Mode	Power
H	X	High Z	Power-down	Standby ( $\text{I}_{\text{SB}}$ )
L	H	Data out	Read	Active ( $\text{I}_{\text{CC}}$ )
L	L	High Z	Write	Active ( $\text{I}_{\text{CC}}$ )

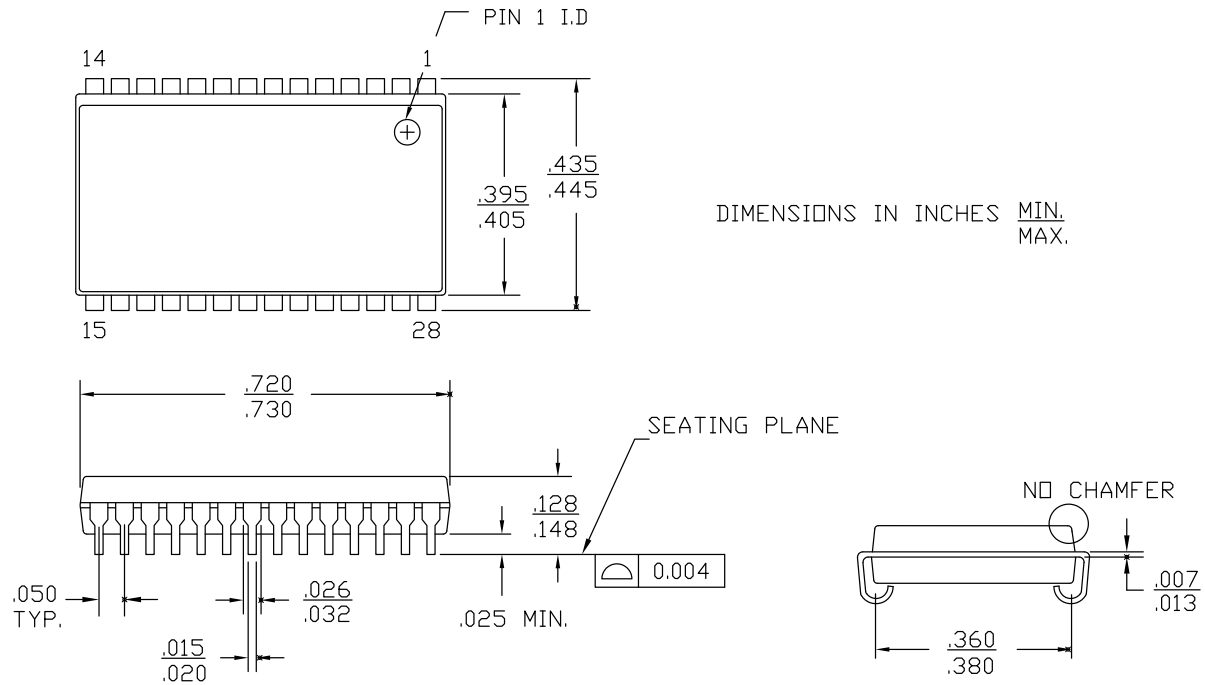
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C107D-10VXI	51-85032	28-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1007D-10VXI	51-85031	28-pin (300-Mil) Molded SOJ (Pb-free)	

Diagram illustrating the pinout of the CY7C017VX-I, showing the connection of each pin to its respective function:

- Temperature Range: I = Industrial
- Pb-free
- Package Type: V = 28-pin Molded SOJ
- Speed: 10 ns
- Process Technology: D = C9, 90 nm Technology
- xx7 = 07 or 007 = (400-Mil / 300-Mil) 1-Mbit density
- Family Code: 1 = Fast Asynchronous SRAM family
- Technology Code: C = CMOS
- Marketing Code: 7 = SRAM
- Company ID: CY = Cypress

## Package Diagrams

**Figure 8. 28-pin SOJ (400 Mils) V28.4 (Molded SOJ V28) Package Outline, 51-85032**



### NOTES :

1. PACKAGE WEIGHT : 1.24g
2. JEDEC REFERENCE : MS-027

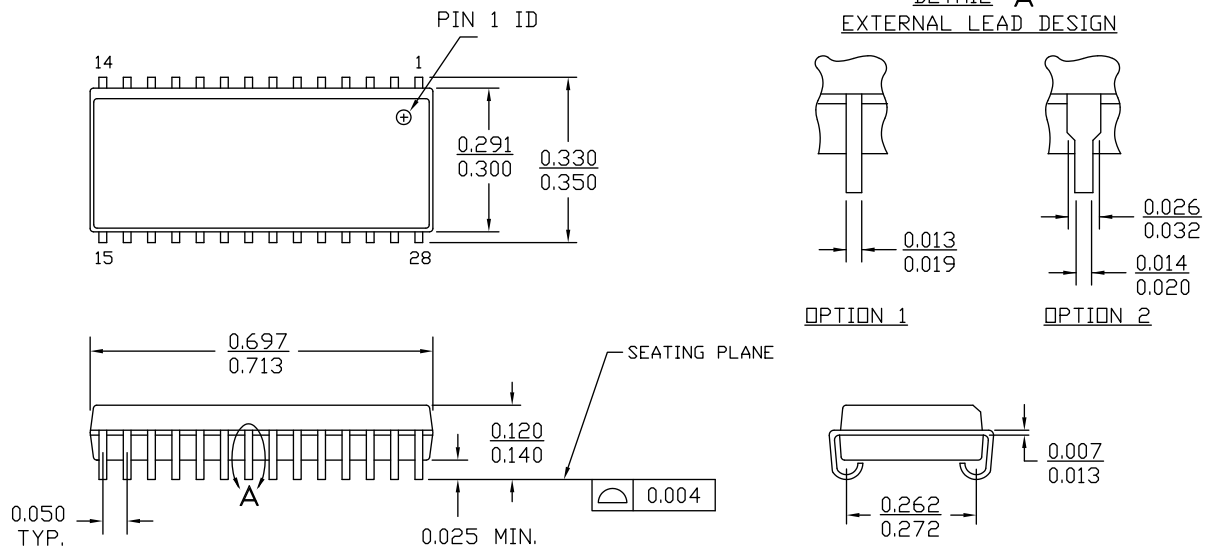
51-85032 \*F

## Package Diagrams(continued)

**Figure 9. 28-pin SOJ (300 Mils) V28.3 (Molded SOJ V21) Package Outline, 51-85031**

NOTE :

1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN.  
MAX.



51-85031 \*E

## Acronyms

Acronym	Description
BGA	Ball Grid Array
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Very Fine-Pitch Ball Grid Array
I/O	Input/Output
JTAG	Joint Test Action Group
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C107D/CY7C1007D, 1-Mbit (1 M × 1) Static RAM Document Number: 38-05469				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233722	See ECN	RKF	DC parameters modified as per EROS (Spec # 01-02165) Pb-free offering in Ordering Information
*B	263769	See ECN	RKF	Added Data Retention Characteristics table Added T <sub>power</sub> Spec in Switching Characteristics Table Shaded Ordering Information
*C	307601	See ECN	RKF	Reduced Speed bins to –10 and –12 ns
*D	560995	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 12 ns speed bin Added I <sub>CC</sub> values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V <sub>CC</sub> +2V to V <sub>CC</sub> +1V in footnote #3
*E	802877	See ECN	VKN	Changed I <sub>CC</sub> specs from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz
*F	2898399	03/24/2010	AJU	Updated Package Diagrams
*G	3104943	12/08/2010	AJU	Added <a href="#">Ordering Code Definitions</a> .
*H	3218989	04/07/2011	PRAS	Added TOC Added Acronyms and Units of Measure table. Updated Package diagrams from *C to *D (51-85032)
*I	4040950	06/26/2013	MEMJ	Updated <a href="#">Functional Description</a> . Updated <a href="#">Electrical Characteristics</a> Added one more Test Condition “I <sub>OH</sub> = –0.1mA” for V <sub>OH</sub> parameter and added maximum value corresponding to that Test Condition. Added Note 4 and referred the same note in maximum value for V <sub>OH</sub> parameter corresponding to Test Condition “I <sub>OH</sub> = –0.1mA”. Updated <a href="#">Package Diagrams</a> : spec 51-85031 – Changed revision from *D to *E. Updated in new template.
*J	4385003	05/23/2014	MEMJ	Updated <a href="#">Package Diagrams</a> : spec 51-85032 – Changed revision from *E to *F. Completing Sunset Review.
*K	4578500	11/24/2014	MEMJ	Added related documentation hyperlink in page 1.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

#### Products

<a href="#">Automotive</a>	<a href="#">cypress.com/go/automotive</a>
<a href="#">Clocks &amp; Buffers</a>	<a href="#">cypress.com/go/clocks</a>
<a href="#">Interface</a>	<a href="#">cypress.com/go/interface</a>
<a href="#">Lighting &amp; Power Control</a>	<a href="#">cypress.com/go/powerpsoc</a>
	<a href="#">cypress.com/go/plc</a>
<a href="#">Memory</a>	<a href="#">cypress.com/go/memory</a>
<a href="#">PSoC</a>	<a href="#">cypress.com/go/psoc</a>
<a href="#">Touch Sensing</a>	<a href="#">cypress.com/go/touch</a>
<a href="#">USB Controllers</a>	<a href="#">cypress.com/go/USB</a>
<a href="#">Wireless/RF</a>	<a href="#">cypress.com/go/wireless</a>

#### PSoC® Solutions

[psoc.cypress.com/solutions](#)  
[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

#### Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

#### Technical Support

[cypress.com/go/support](#)

© Cypress Semiconductor Corporation, 2007-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.