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## Selection Guide

Description <sup>[1]</sup>	-15	Unit
Maximum Access Time	15	ns
Maximum Operating Current	80	mA
Maximum CMOS Standby Current	10	mA

## Pin Configurations

Figure 1. 44-pin SOJ/TSOP II pinout <sup>[2]</sup>

A <sub>4</sub>	1	44	A <sub>5</sub>
A <sub>3</sub>	2	43	A <sub>6</sub>
A <sub>2</sub>	3	42	A <sub>7</sub>
A <sub>1</sub>	4	41	$\overline{\text{OE}}$
A <sub>0</sub>	5	40	$\overline{\text{BHE}}$
$\overline{\text{CE}}$	6	39	$\overline{\text{BLE}}$
I/O <sub>0</sub>	7	38	I/O <sub>15</sub>
I/O <sub>1</sub>	8	37	I/O <sub>14</sub>
I/O <sub>2</sub>	9	36	I/O <sub>13</sub>
I/O <sub>3</sub>	10	35	I/O <sub>12</sub>
V <sub>CC</sub>	11	34	V <sub>SS</sub>
V <sub>SS</sub>	12	33	V <sub>CC</sub>
I/O <sub>4</sub>	13	32	I/O <sub>11</sub>
I/O <sub>5</sub>	14	31	I/O <sub>10</sub>
I/O <sub>6</sub>	15	30	I/O <sub>9</sub>
I/O <sub>7</sub>	16	29	I/O <sub>8</sub>
$\overline{\text{WE}}$	17	28	NC
A <sub>15</sub>	18	27	A <sub>8</sub>
A <sub>14</sub>	19	26	A <sub>9</sub>
A <sub>13</sub>	20	25	A <sub>10</sub>
A <sub>12</sub>	21	24	A <sub>11</sub>
NC	22	23	NC

Figure 2. 48-ball FBGA pinout <sup>[2]</sup>

1	2	3	4	5	6	
$\overline{\text{BLE}}$	$\overline{\text{OE}}$	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	NC	A
I/O <sub>8</sub>	$\overline{\text{BHE}}$	A <sub>3</sub>	A <sub>4</sub>	$\overline{\text{CE}}$	I/O <sub>0</sub>	B
I/O <sub>9</sub>	I/O <sub>10</sub>	A <sub>5</sub>	A <sub>6</sub>	I/O <sub>2</sub>	I/O <sub>1</sub>	C
V <sub>SS</sub>	I/O <sub>11</sub>	NC	A <sub>7</sub>	I/O <sub>3</sub>	V <sub>CC</sub>	D
V <sub>CC</sub>	I/O <sub>12</sub>	NC	NC	I/O <sub>4</sub>	V <sub>SS</sub>	E
I/O <sub>14</sub>	I/O <sub>13</sub>	A <sub>14</sub>	A <sub>15</sub>	I/O <sub>5</sub>	I/O <sub>6</sub>	F
I/O <sub>15</sub>	NC	A <sub>12</sub>	A <sub>13</sub>	$\overline{\text{WE}}$	I/O <sub>7</sub>	G
NC	A <sub>8</sub>	A <sub>9</sub>	A <sub>10</sub>	A <sub>11</sub>	NC	H

### Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25 °C.
- NC pins are not connected on the die.

## Pin Definitions

Pin Name	Pin Number	I/O Type	Description
A <sub>0</sub> –A <sub>15</sub>	1–5, 18–21, 24–27, 42–44	Input	<b>Address Inputs used to select one of the address locations.</b>
I/O <sub>0</sub> –I/O <sub>15</sub>	7–10, 13–16, 29–32, 35–38	Input/Output	<b>Bidirectional Data I/O lines.</b> Used as input or output lines depending on operation.
NC	22, 23, 28	No Connect	<b>No Connects.</b> This pin is not connected to the die.
WE	17	Input/Control	<b>Write Enable Input, active LOW.</b> When selected LOW, a Write is conducted. When selected HIGH, a Read is conducted.
CE	6	Input/Control	<b>Chip Enable Input, active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{BHE}}$ , $\overline{\text{BLE}}$	40, 39	Input/Control	<b>Byte Write Select Inputs, active LOW.</b> $\overline{\text{BHE}}$ controls I/O <sub>15</sub> –I/O <sub>8</sub> , $\overline{\text{BLE}}$ controls I/O <sub>7</sub> –I/O <sub>0</sub> .
OE	41	Input/Control	<b>Output Enable, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When de-asserted HIGH, I/O pins are tri-stated, and act as input data pins.
V <sub>SS</sub>	12, 34	Ground	<b>Ground for the device.</b> Should be connected to ground of the system.
V <sub>CC</sub>	11, 33	Power Supply	<b>Power Supply inputs to the device.</b>

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  to relative GND<sup>[3]</sup> ..... -0.5 V to +4.6 V

DC voltage applied to outputs in high Z state<sup>[3]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage<sup>[3]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Automotive	-40 °C to +125 °C	2.5 V–2.7 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-15		Unit
			Min	Max	
$V_{OH}$	Output HIGH voltage	$V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2.3	–	V
$V_{OL}$	Output LOW voltage	$V_{CC} = \text{Min}, I_{OL} = 1.0 \text{ mA}$	–	0.4	V
$V_{IH}$	Input HIGH voltage		2.0	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW voltage <sup>[3]</sup>		-0.3	0.8	V
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	-3	+3	μA
$I_{OZ}$	Output leakage current	$GND \leq V_I \leq V_{CC}$ , output disabled	-3	+3	μA
$I_{CC}$	$V_{CC}$ operating supply current	$V_{CC} = \text{Max}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	–	80	mA
$I_{SB1}$	Automatic CE power-down Current – TTL inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	–	15	mA
$I_{SB2}$	Automatic CE power-down Current – CMOS inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.3 \text{ V}$ , or $V_{IN} \leq 0.3 \text{ V}$ , $f = 0$	–	10	mA

### Note

3.  $V_{IL}(\text{min.}) = -2.0\text{V}$  and  $V_{IH}(\text{max.}) = V_{CC} + 0.5 \text{ V}$  for pulse durations of less than 20 ns.

## Capacitance

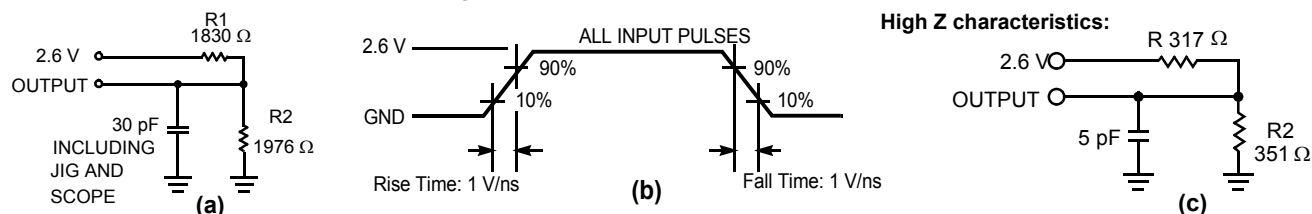
Parameter <sup>[4]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 2.6\text{ V}$	8	pF
$C_{OUT}$	Output capacitance		8	pF

## Thermal Resistance

Parameter <sup>[4]</sup>	Description	Test Conditions	44-pin TSOP II	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still Air, soldered on a $3 \times 4.5$ inch, four-layer printed circuit board	76.92	$^{\circ}\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		15.86	$^{\circ}\text{C/W}$

## AC Test Loads and Waveforms

**Figure 3. AC Test Loads and Waveforms <sup>[5]</sup>**



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except high Z) are tested using the Thevenin load shown in Figure 3 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 3 (c).

## Switching Characteristics

Over the Operating Range

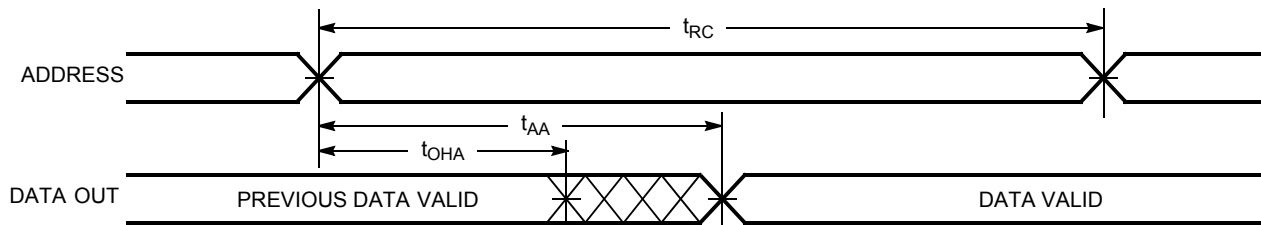
Parameter <sup>[6]</sup>	Description	-15		Unit
		Min	Max	
Read Cycle				
t <sub>RC</sub>	Read cycle time	15	–	ns
t <sub>AA</sub>	Address to data valid	–	15	ns
t <sub>OHA</sub>	Data hold from address change	3	–	ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to data valid	–	15	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to data valid	–	7	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to low Z <sup>[7]</sup>	0	–	ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to high Z <sup>[7, 8]</sup>	–	7	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to low Z <sup>[7]</sup>	3	–	ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to high Z <sup>[7, 8]</sup>	–	7	ns
t <sub>PU</sub> <sup>[9]</sup>	$\overline{\text{CE}}$ LOW to power-up	0	–	ns
t <sub>PD</sub> <sup>[9]</sup>	$\overline{\text{CE}}$ HIGH to power-down	–	15	ns
t <sub>DBE</sub>	Byte enable to data valid	–	7	ns
t <sub>LZBE</sub>	Byte enable to low Z	0	–	ns
t <sub>HZBE</sub>	Byte disable to high Z	–	7	ns
Write Cycle <sup>[10, 11]</sup>				
t <sub>WC</sub>	Write cycle time	15	–	ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to write end	10	–	ns
t <sub>AW</sub>	Address set-up to write end	10	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address set-up to write start	0	–	ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ pulse width	10	–	ns
t <sub>SD</sub>	Data set-up to write end	8	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to low Z <sup>[7]</sup>	3	–	ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to high Z <sup>[7, 8]</sup>	–	7	ns
t <sub>BW</sub>	Byte enable to end of write	9	–	ns

### Notes

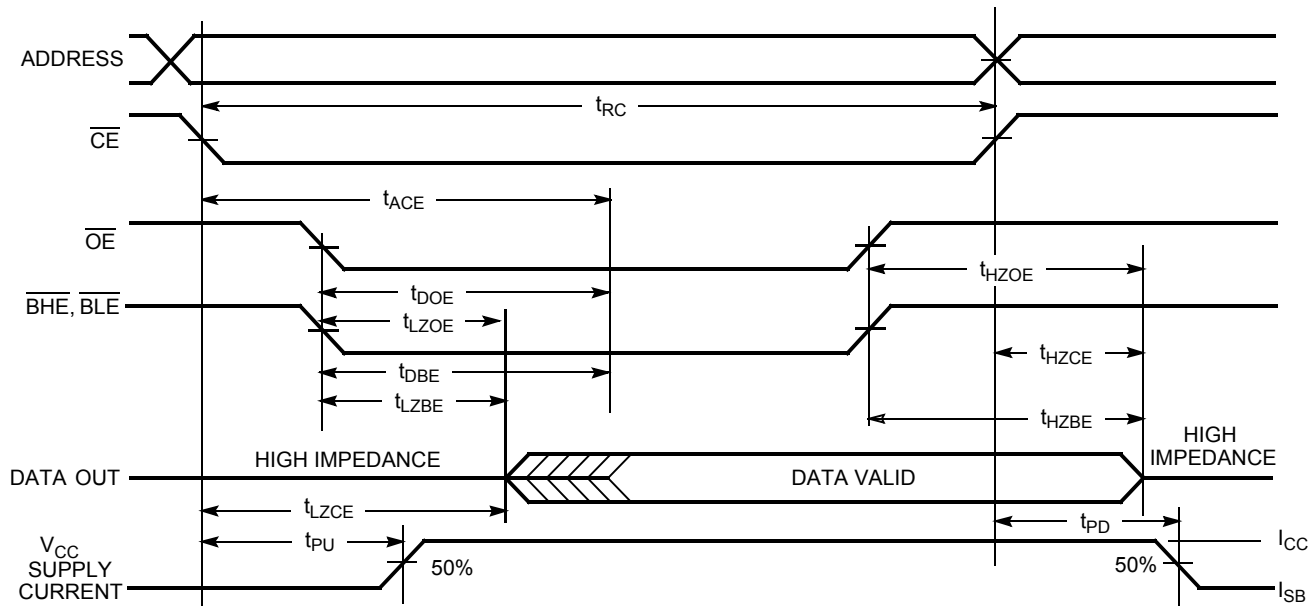
- Test conditions assume signal transition time of 2.6 ns or less, timing reference levels of 1.3 V, input pulse levels of 0 to 2.6 V.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (c) of Figure 3. Transition is measured  $\pm 500$  mV from steady-state voltage.
- This parameter is guaranteed by design and is not tested.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and  $\overline{BHE}/\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$  and  $\overline{BHE}/\overline{BLE}$  must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum write pulse width for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms

**Figure 4. Read Cycle No. 1** [12, 13]



**Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [13, 14]

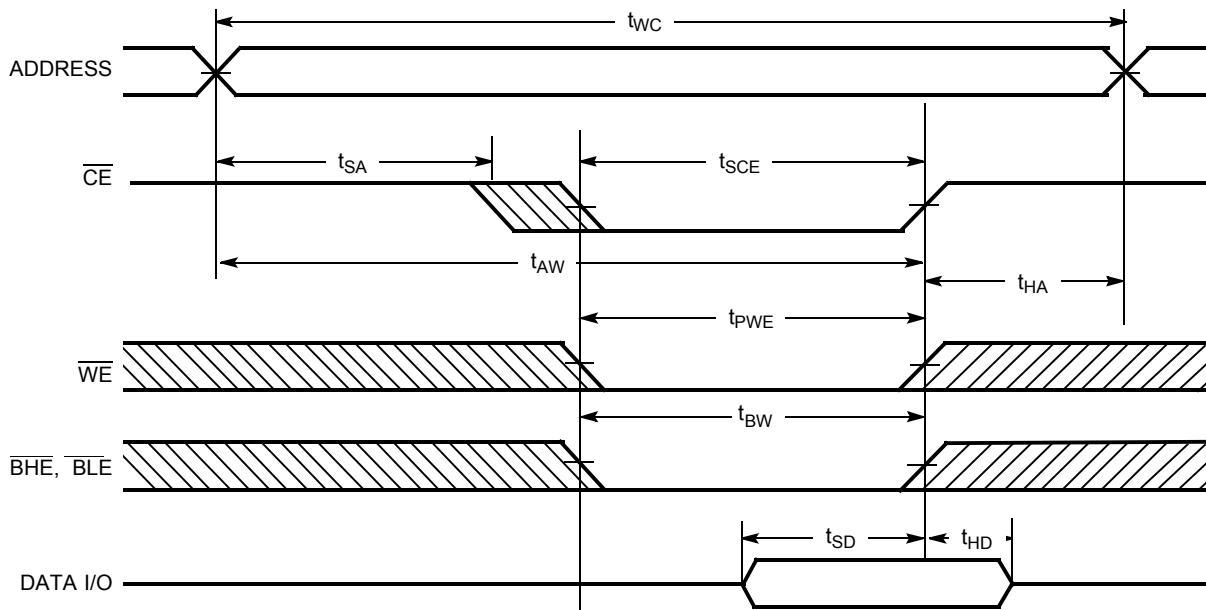


### Notes

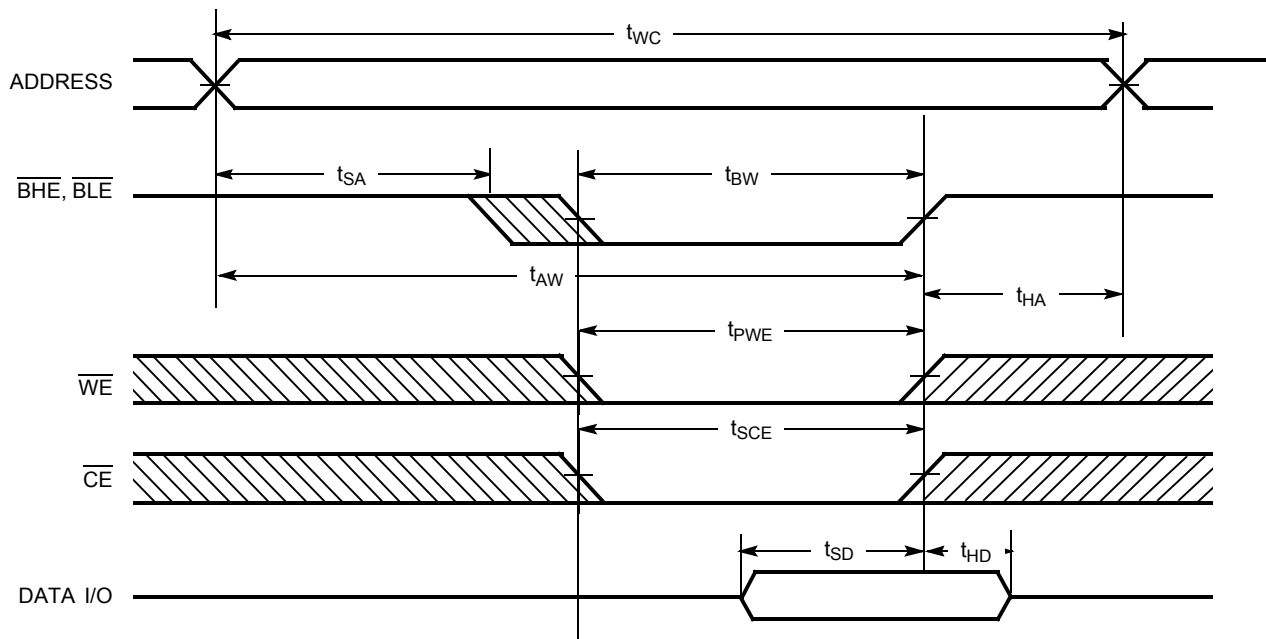
12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IL}$ .
13.  $\overline{WE}$  is HIGH for Read cycle.
14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms** (continued)

**Figure 6. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)** [15, 16]



**Figure 7. Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**



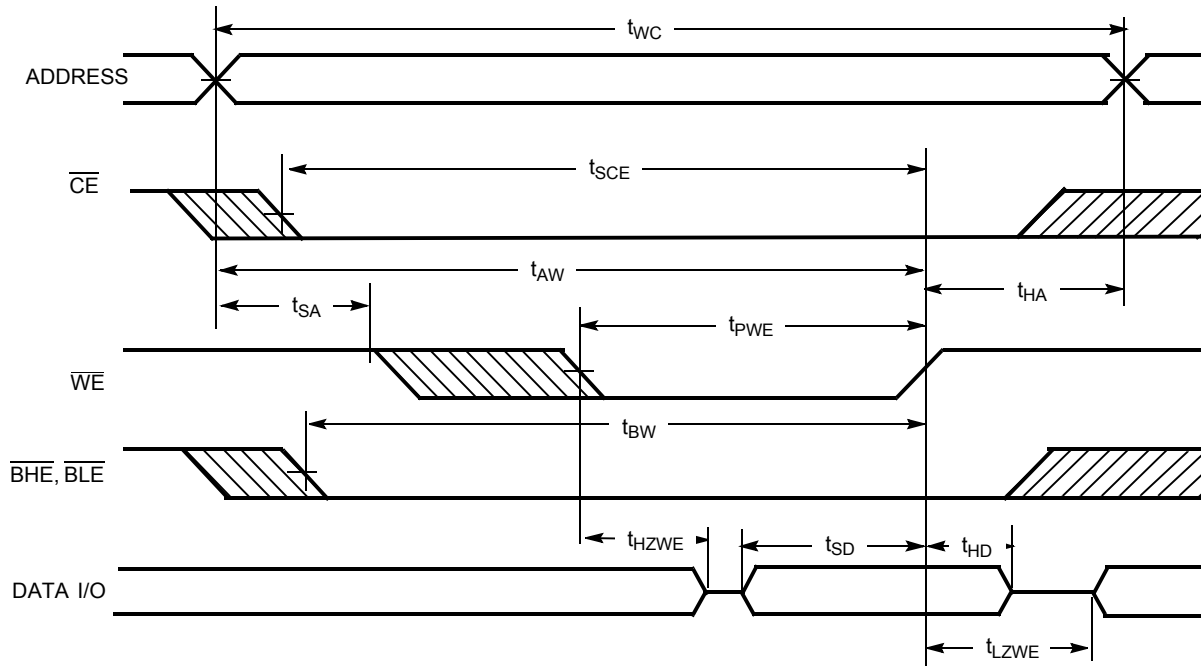
**Notes**

15. Data I/O is high-impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .  
 16. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.



## Switching Waveforms *(continued)*

**Figure 8. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) <sup>[17]</sup>**

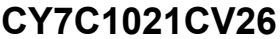


### Note

17. The minimum write pulse width for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) should be sum of  $t_{SD}$  and  $t_{HZWE}$ .

**Truth Table**

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I <sub>CC</sub> )
			L	H	Data Out	High Z	Read – Lower bits only	Active (I <sub>CC</sub> )
			H	L	High Z	Data Out	Read – Upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I <sub>CC</sub> )
			L	H	Data In	High Z	Write – Lower bits only	Active (I <sub>CC</sub> )
			H	L	High Z	Data In	Write – Upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )



Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at <http://www.cypress.com> and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative.

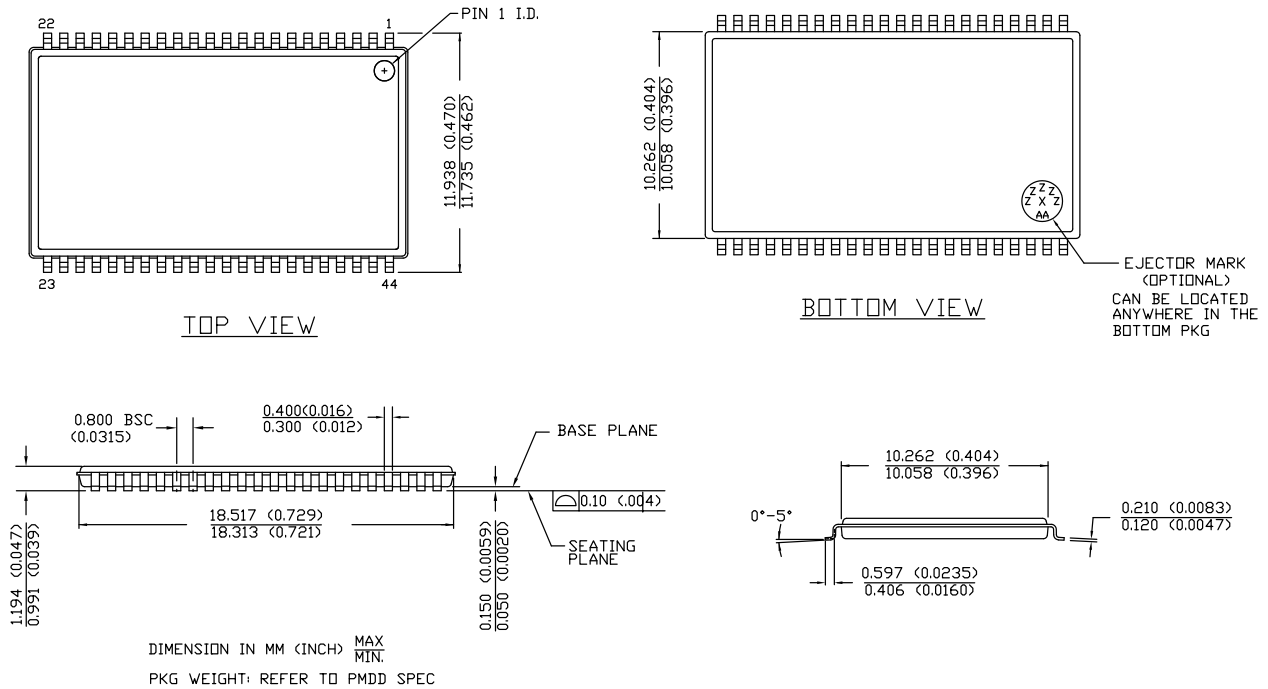
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1021CV26-15ZSXE	51-85087	44-pin TSOP Type II (Pb-free)	Automotive
	CY7C1021CV26-15ZSXET	51-85087	44-pin TSOP Type II (Pb-free)	

The diagram shows the part number CY7C1021C-V26-15XX-XE-X broken down into its constituent fields. Each field is represented by a vertical line segment, and a horizontal line connects it to its description. The fields and their descriptions are as follows:

- CY**: Company ID: CY = Cypress
- 7**: Marketing Code: 7 = SRAM
- C**: Technology Code: C = CMOS
- 1021**: Part Identifier
- C**: Process Technology: C = 0.16  $\mu\text{m}$
- V26**: V26 = 2.6 V
- : Separator
- 15**: Speed Grade: 15 ns
- XX**: Package Type: XX = ZS  
ZS = 44-pin TSOP Type II
- X**: Pb-free
- E**: Temperature Range: E = Automotive
- X**: X = T or Blank  
T = Tape and Reel; Blank = Tube

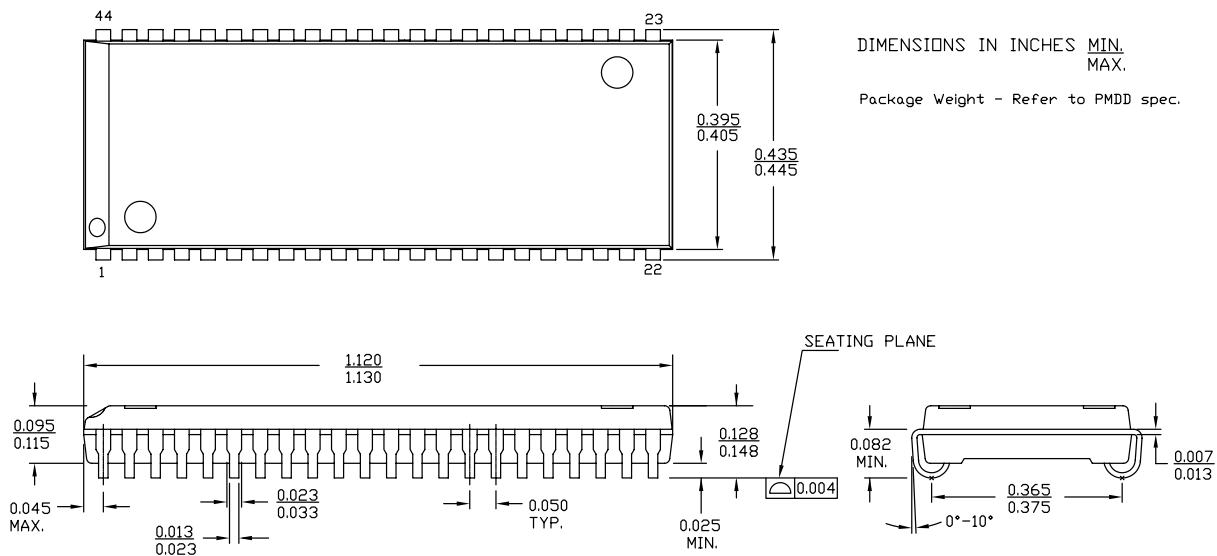
## Package Diagrams

Figure 9. 44-pin TSOP Z44-II Package Outline, 51-85087



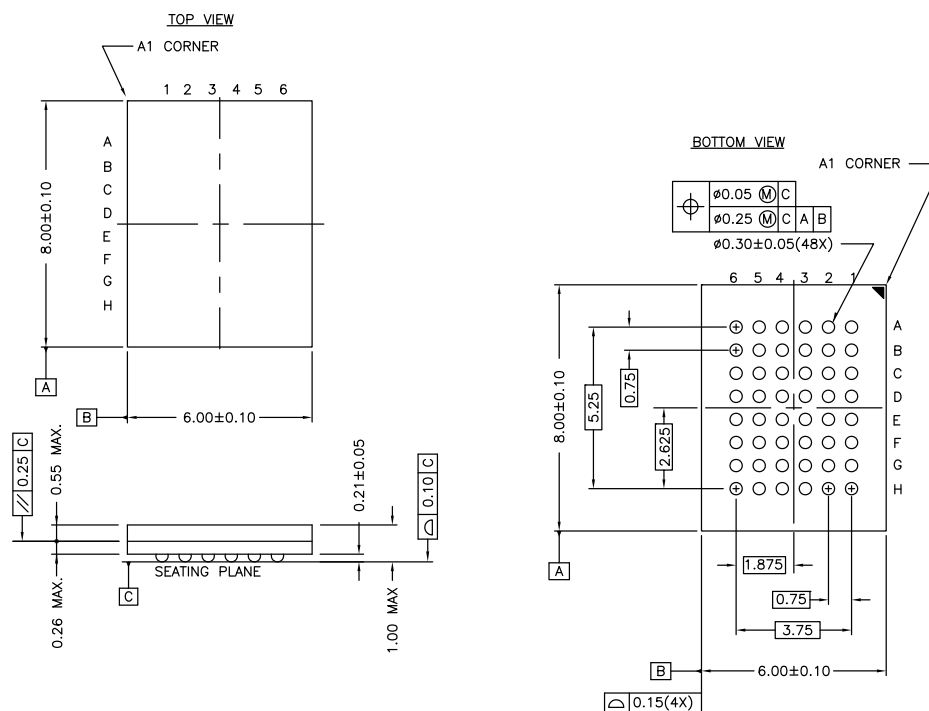
51-85087 \*E

Figure 10. 44-pin SOJ (400 Mils) V44.4 Package Outline, 51-85082



51-85082 \*E

**Figure 11. 48-ball FBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150**



NOTE:  
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)  
posted on the Cypress web.

51-85150 \*H

## Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{\text{CE}}$	Chip Enable
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TSOP	Thin Small-Outline Package
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mm	millimeter
mW	milliwatt
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1021CV26, 1-Mbit (64 K × 16) Static RAM Document Number: 38-05589				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	238454	See ECN	RKF	New data sheet for Automotive.
*A	335861	See ECN	SYT	Added 44-pin SOJ Package related information in all instances across the document. Updated <a href="#">Ordering Information</a> : Updated part numbers (Added Lead-Free Product Information).
*B	493543	See ECN	NXR	Updated <a href="#">Electrical Characteristics</a> : Changed description of I <sub>LX</sub> parameter from "Input Load Current" to "Input Leakage Current". Removed I <sub>OS</sub> parameter and its details. Updated <a href="#">Ordering Information</a> : Updated part numbers.
*C	2897087	03/22/10	AJU	Updated <a href="#">Ordering Information</a> : Removed obsolete parts. Updated <a href="#">Package Diagrams</a> .
*D	3057593	10/13/2010	PRAS	Updated <a href="#">Ordering Information</a> : Updated part numbers. Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> .
*E	3098812	12/01/2010	PRAS	Minor edits across the document. Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated to new template.
*F	3277371	06/08/2011	AJU	Updated <a href="#">Pin Configurations</a> (Included pin configurations for 44-pin SOJ and 48-ball FBGA packages).
*G	4141238	09/30/2013	VINI	Updated <a href="#">Package Diagrams</a> : spec 51-85087 – Changed revision from *C to *E. spec 51-85082 – Changed revision from *C to *E. spec 51-85150 – Changed revision from *F to *H. Updated to new template. Completing Sunset Review.
*H	4567793	11/12/2014	VINI	Updated <a href="#">Functional Description</a> : Added "For a complete list of related resources, <a href="#">click here</a> ." at the end. Updated <a href="#">Switching Characteristics</a> : Added Note 11 and referred the same note in "Write Cycle". Updated <a href="#">Switching Waveforms</a> : Added Note 17 and referred the same note in <a href="#">Figure 8</a> . Completing Sunset Review.
*I	4573200	11/18/2014	VINI	Updated <a href="#">Ordering Information</a> : Removed prune part numbers namely CY7C1021CV26-15VXE, CY7C1021CV26-15BAE, CY7C1021CV26-15BAET, and CY7C1021CV26-15VXET.
*J	5004033	11/05/2015	VINI	Updated to new template. Completing Sunset Review.

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