Contents

Selection Guide

Description [1]	-15	Unit
Maximum Access Time	15	ns
Maximum Operating Current	80	mA
Maximum CMOS Standby Current	10	mA

Pin Configurations

Figure 1. 44-pin SOJ/TSOP II pinout [2]

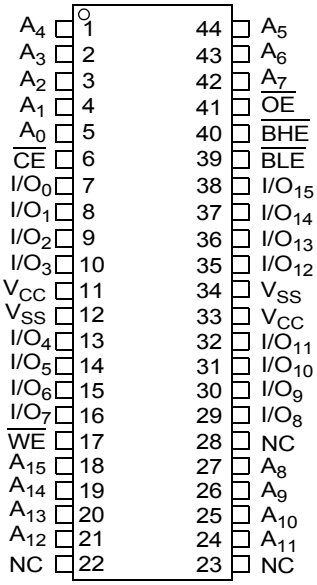
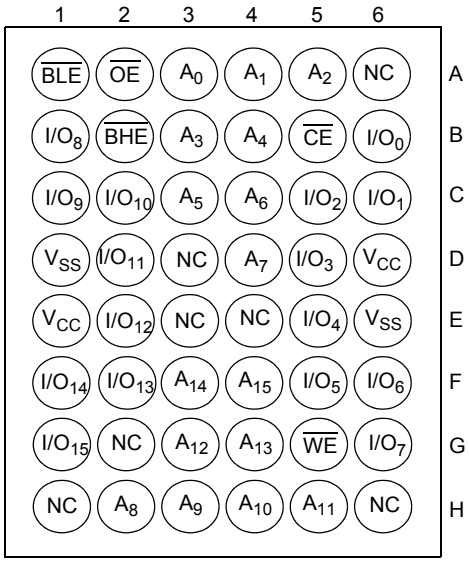


Figure 2. 48-ball FBGA pinout [2]



Notes
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25$ °C.
2. NC pins are not connected on the die.

Pin Definitions

Pin Name	Pin Number	I/O Type	Description
A_0–A_{15}	1–5, 18–21, 24–27, 42–44	Input	**Address Inputs used to select one of the address locations.**
I/O_0–I/O_{15}	7–10, 13–16, 29–32, 35–38	Input/Output	**Bidirectional Data I/O lines**. Used as input or output lines depending on operation.
NC	22, 23, 28	No Connect	**No Connects**. This pin is not connected to the die.
WE	17	Input/Control	**Write Enable Input, active LOW**. When selected LOW, a Write is conducted. When selected HIGH, a Read is conducted.
CE	6	Input/Control	**Chip Enable Input, active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{BHE}$, $\overline{BLE}$	40, 39	Input/Control	**Byte Write Select Inputs, active LOW**. $\overline{BHE}$ controls I/O_{15}–I/O_8, $\overline{BLE}$ controls I/O_7–I/O_0.
OE	41	Input/Control	**Output Enable, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When de-asserted HIGH, I/O pins are tri-stated, and act as input data pins.
V_{SS}	12, 34	Ground	**Ground for the device**. Should be connected to ground of the system.
V_{CC}	11, 33	Power Supply	**Power Supply inputs to the device**.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to relative GND[3] .....–0.5 V to +4.6 V

DC voltage applied to outputs in high Z state[3] .....–0.5 V to V_{CC} + 0.5 V

DC input voltage[3] ..... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Automotive	–40 °C to +125 °C	2.5 V–2.7 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-15		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –1.0 mA	2.3	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 1.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage[3]		–0.3	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}	–3	+3	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{CC}, output disabled	–3	+3	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	–	80	mA
I_{SB1}	Automatic CE power-down Current – TTL inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	15	mA
I_{SB2}	Automatic CE power-down Current – CMOS inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0	–	10	mA

Note
3. V_{IL} (min.) = –2.0V and V_{IH}(max) = V_{CC} + 0.5 V for pulse durations of less than 20 ns.

Capacitance

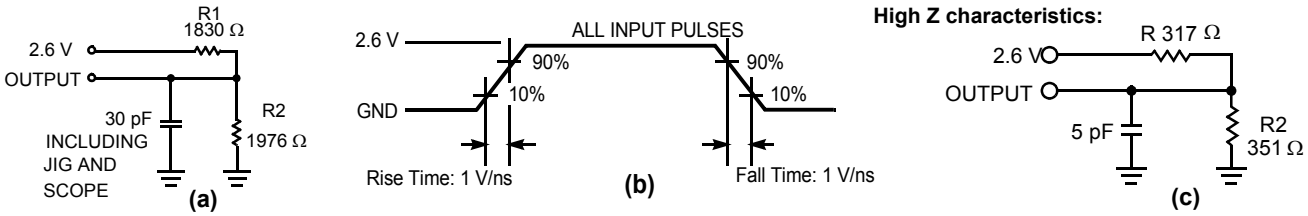
Parameter [4]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 2.6 V	8	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter [4]	Description	Test Conditions	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	76.92	°C/W
Θ_{JC}	Thermal resistance (junction to case)		15.86	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [5]



Notes
4. Tested initially and after any design or process changes that may affect these parameters.
5. AC characteristics (except high Z) are tested using the Thevenin load shown in Figure 3 (a). High Z characteristics are tested for all speeds using the test load shown inFigure 3 (c).

Switching Characteristics

Over the Operating Range

Parameter [6]	Description	-15		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	15	–	ns
t_{AA}	Address to data valid	–	15	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	15	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	7	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [7]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [7, 8]	–	7	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [7]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [7, 8]	–	7	ns
t_{PU} [9]	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD} [9]	$\overline{CE}$ HIGH to power-down	–	15	ns
t_{DBE}	Byte enable to data valid	–	7	ns
t_{LZBE}	Byte enable to low Z	0	–	ns
t_{HZBE}	Byte disable to high Z	–	7	ns
Write Cycle [10, 11]				
t_{WC}	Write cycle time	15	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	10	–	ns
t_{AW}	Address set-up to write end	10	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	10	–	ns
t_{SD}	Data set-up to write end	8	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [7]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [7, 8]	–	7	ns
t_{BW}	Byte enable to end of write	9	–	ns

Notes

6. Test conditions assume signal transition time of 2.6 ns or less, timing reference levels of 1.3 V, input pulse levels of 0 to 2.6 V.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of Figure 3. Transition is measured ±500 mV from steady-state voltage.
9. This parameter is guaranteed by design and is not tested.
10. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}$/$\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}$/$\overline{BLE}$ must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
11. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 [12, 13]

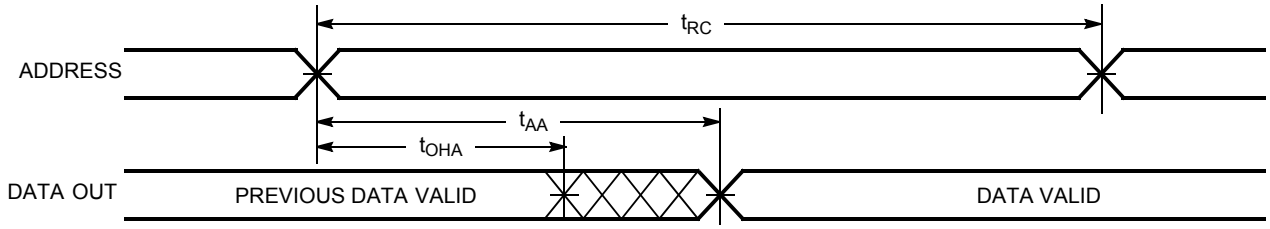
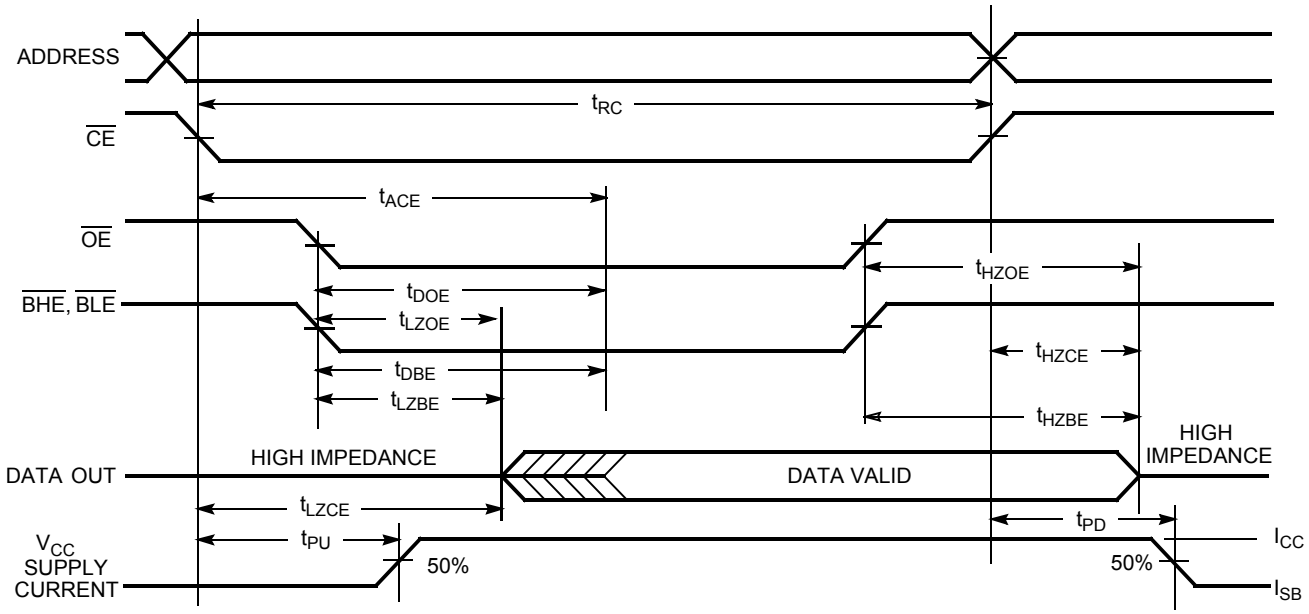


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [13, 14]



Notes
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for Read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms *(continued)*

Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled) [15, 16]

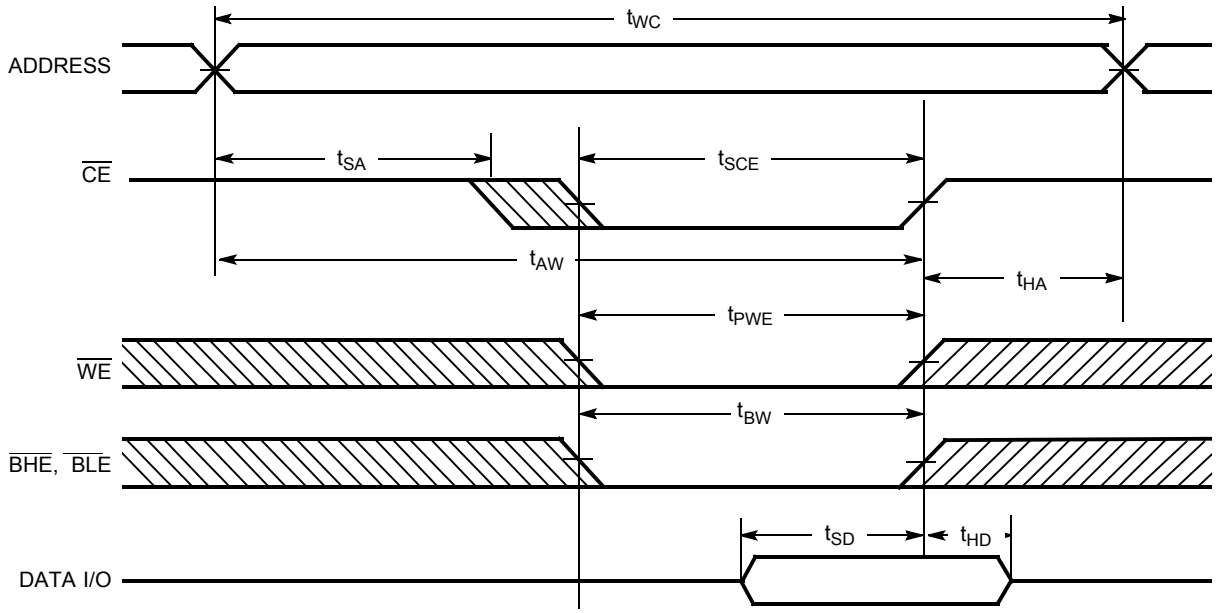
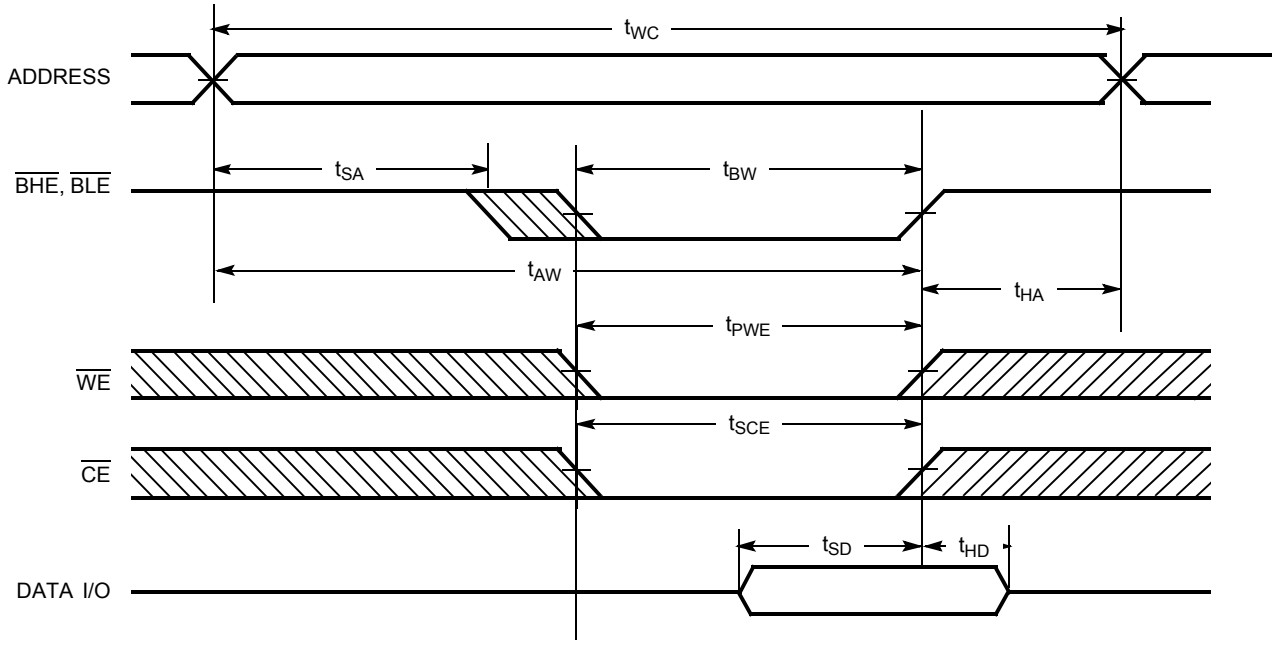


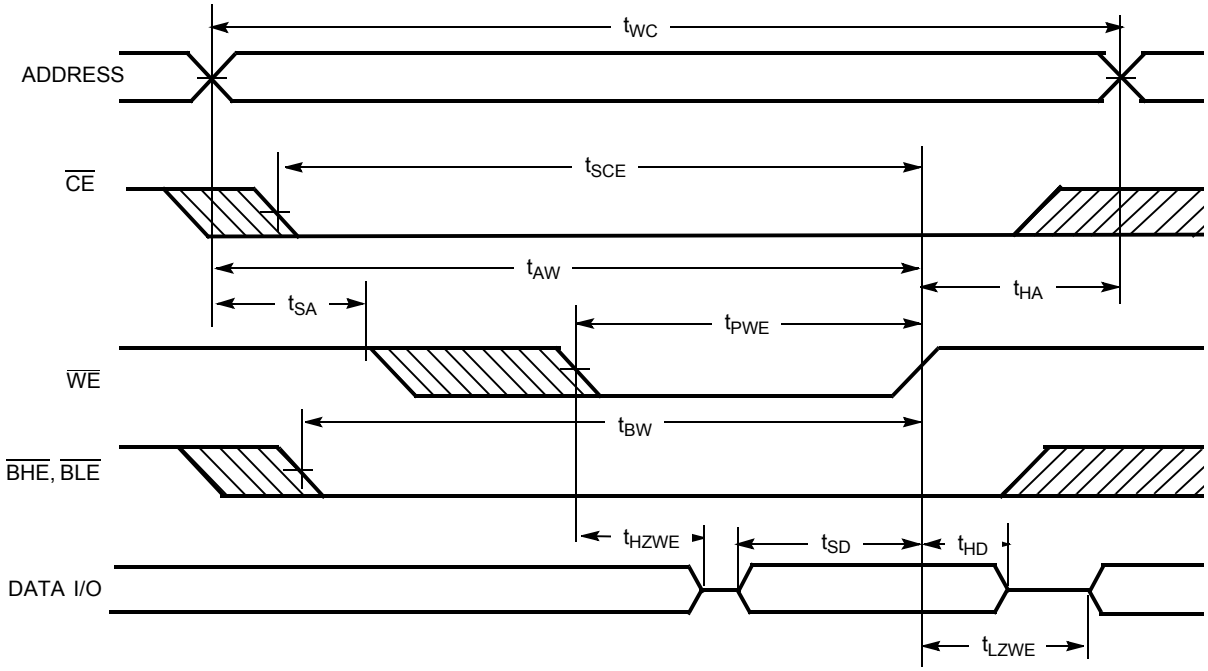
Figure 7. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
15. Data I/O is high-impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$= V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms *(continued)*

Figure 8. Write Cycle No. 3 (WE Controlled, OE LOW) [17]



Note
17. The minimum write pulse width for Write Cycle No. 3 (WE controlled, OE LOW) should be sum of t_{SD} and t_{HZWE}.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read – Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High Z	Write – Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at http://www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.

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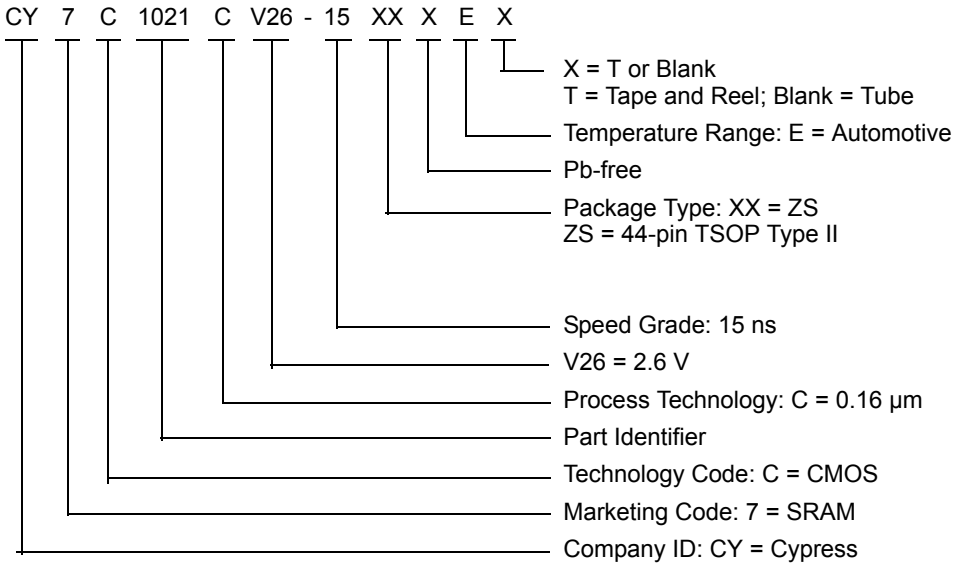
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1021CV26-15ZSXE	51-85087	44-pin TSOP Type II (Pb-free)	Automotive
	CY7C1021CV26-15ZSXET	51-85087	44-pin TSOP Type II (Pb-free)	

Ordering Code Definitions



Package Diagrams

Figure 9. 44-pin TSOP Z44-II Package Outline, 51-85087

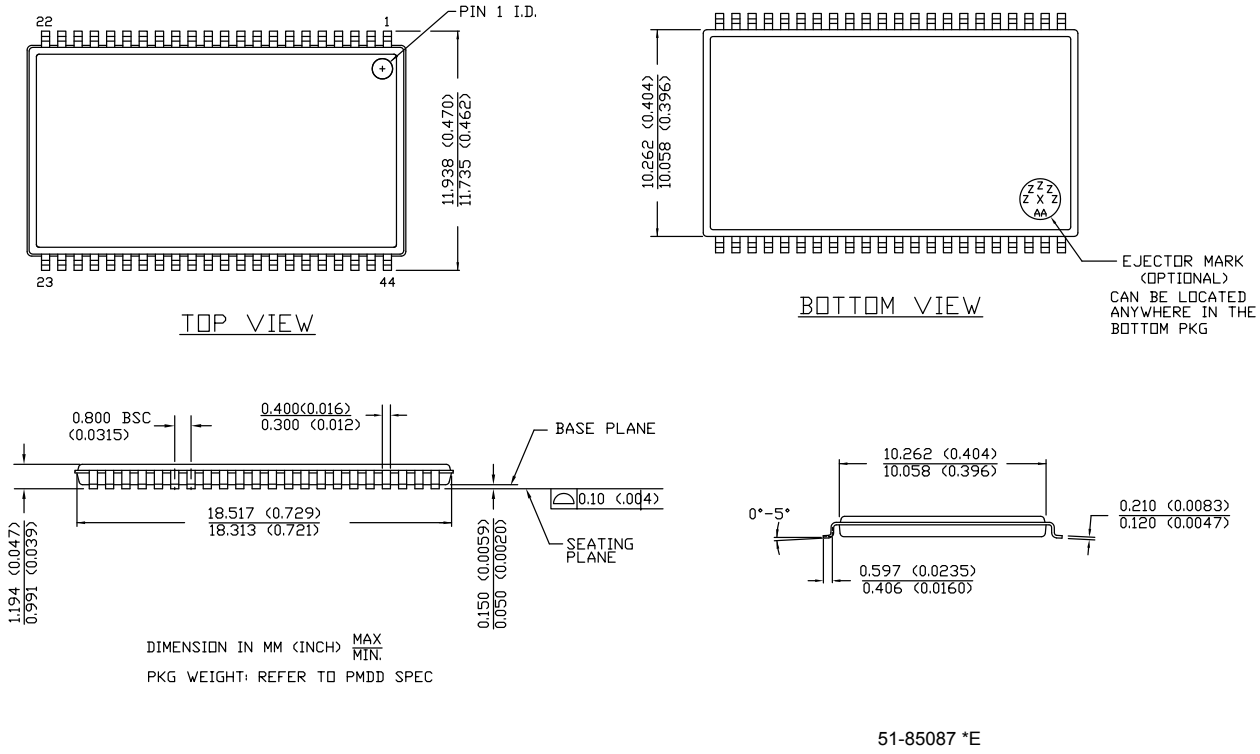
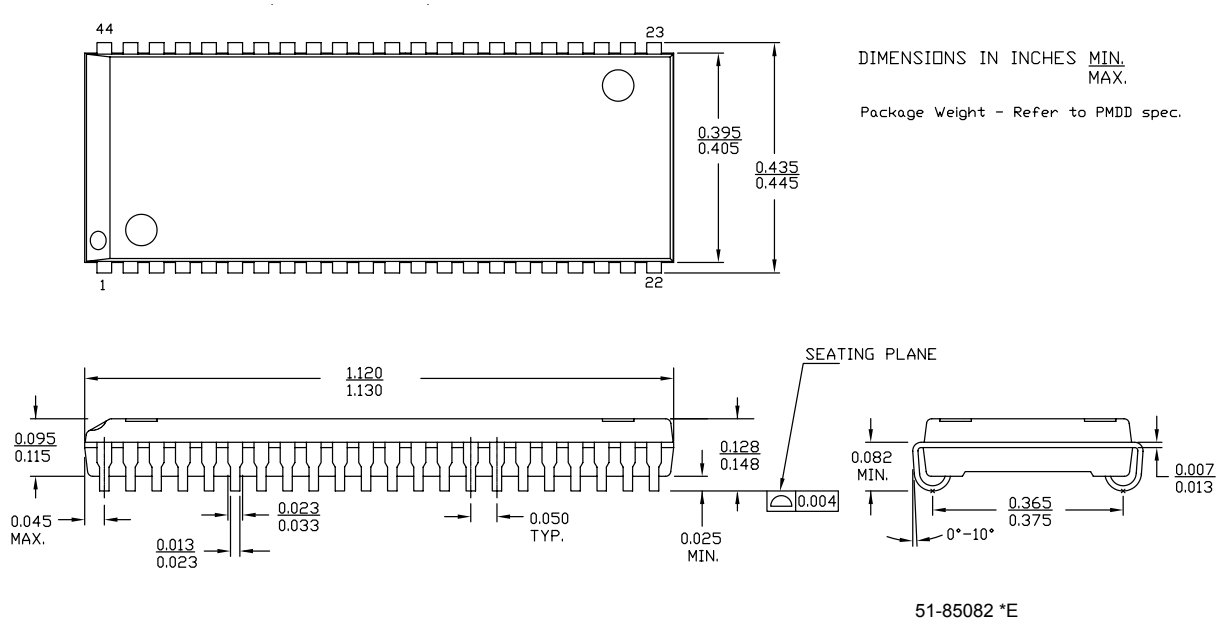
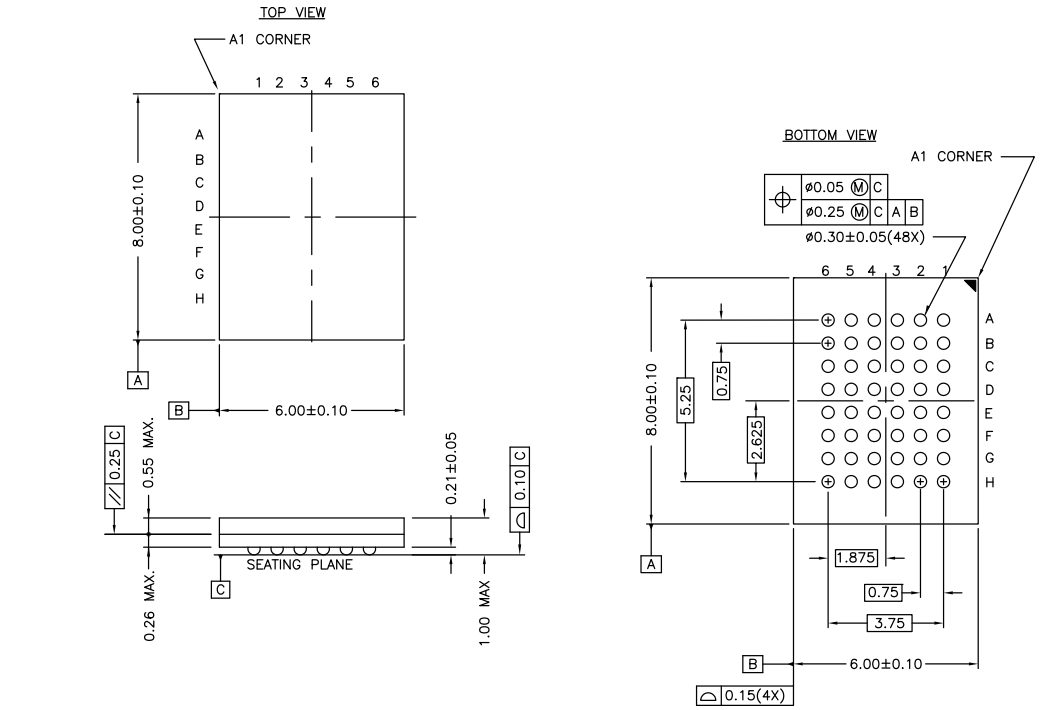


Figure 10. 44-pin SOJ (400 Mils) V44.4 Package Outline, 51-85082



Package Diagrams *(continued)*

Figure 11. 48-ball FBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{OE}$	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TSOP	Thin Small-Outline Package
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
mW	milliwatt
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1021CV26, 1-Mbit (64 K × 16) Static RAM Document Number: 38-05589				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	238454	See ECN	RKF	New data sheet for Automotive.
*A	335861	See ECN	SYT	Added 44-pin SOJ Package related information in all instances across the document. Updated Ordering Information: Updated part numbers (Added Lead-Free Product Information).
*B	493543	See ECN	NXR	Updated Electrical Characteristics: Changed description of I_{IX} parameter from “Input Load Current” to “Input Leakage Current”. Removed I_{OS} parameter and its details. Updated Ordering Information: Updated part numbers.
*C	2897087	03/22/10	AJU	Updated Ordering Information: Removed obsolete parts. Updated Package Diagrams.
*D	3057593	10/13/2010	PRAS	Updated Ordering Information: Updated part numbers. Added Ordering Code Definitions. Updated Package Diagrams.
*E	3098812	12/01/2010	PRAS	Minor edits across the document. Added Acronyms and Units of Measure. Updated to new template.
*F	3277371	06/08/2011	AJU	Updated Pin Configurations (Included pin configurations for 44-pin SOJ and 48-ball FBGA packages).
*G	4141238	09/30/2013	VINI	Updated Package Diagrams: spec 51-85087 – Changed revision from *C to *E. spec 51-85082 – Changed revision from *C to *E. spec 51-85150 – Changed revision from *F to *H. Updated to new template. Completing Sunset Review.
*H	4567793	11/12/2014	VINI	Updated Functional Description: Added “For a complete list of related resources, click here.” at the end. Updated Switching Characteristics: Added Note 11 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 17 and referred the same note in Figure 8. Completing Sunset Review.
*I	4573200	11/18/2014	VINI	Updated Ordering Information: Removed prune part numbers namely CY7C1021CV26-15VXE, CY7C1021CV26-15BAE, CY7C1021CV26-15BAET, and CY7C1021CV26-15VXET.
*J	5004033	11/05/2015	VINI	Updated to new template. Completing Sunset Review.

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