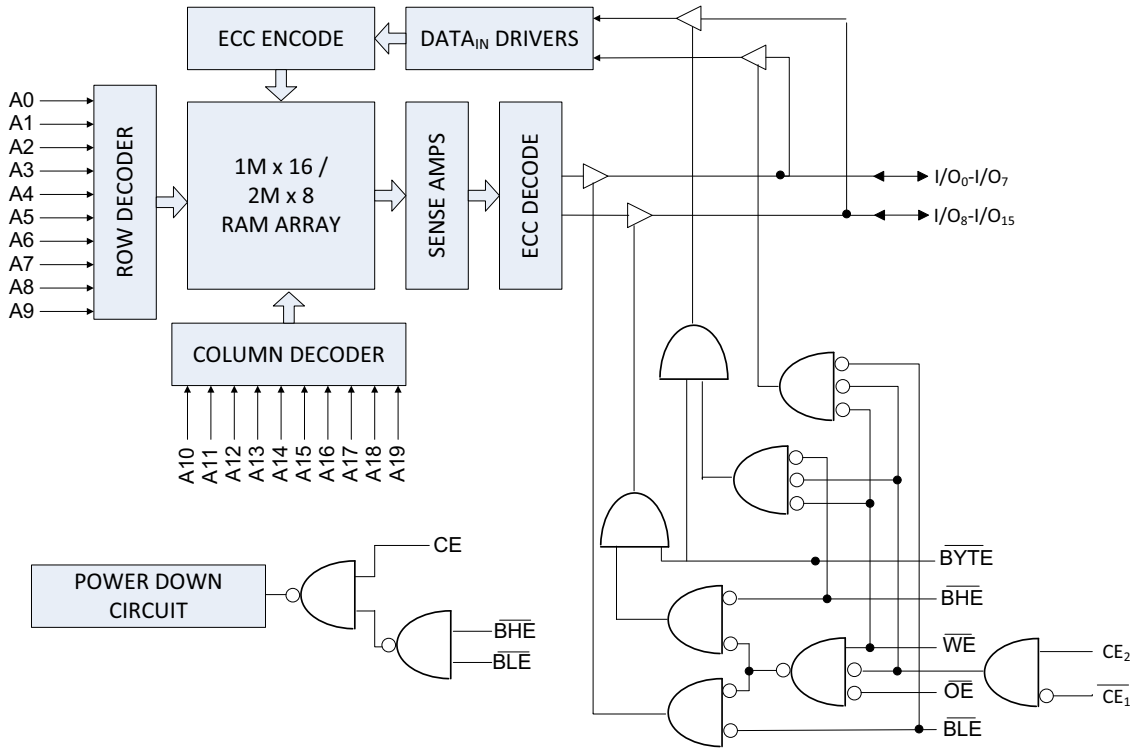
Logic Block Diagram – CY62167G



Contents

Pin Configurations

Figure 1. 48-ball VFBGA pinout [2]
CY62167G

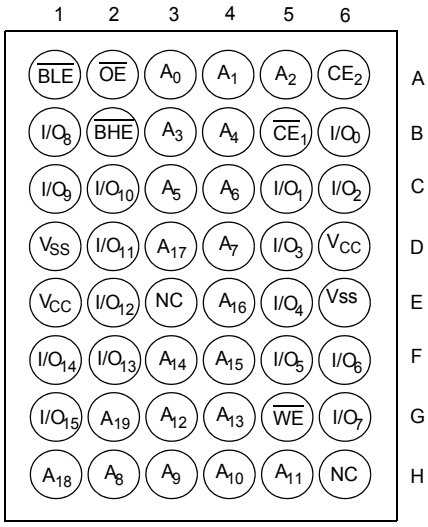
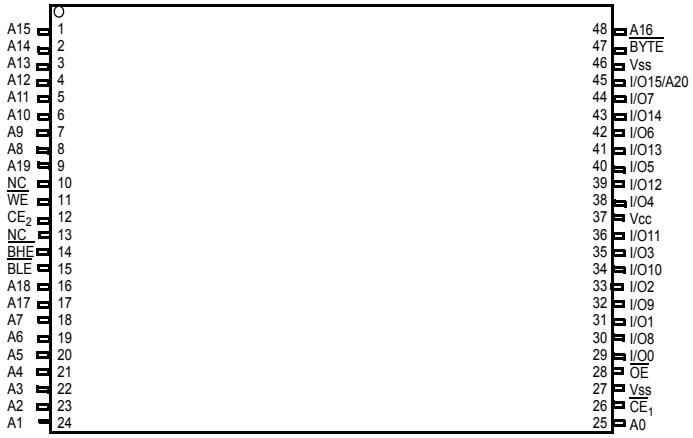


Figure 2. 48-pin TSOP I pinout (Dual Chip Enable without ERR) – CY62167G [2, 3]



Product Portfolio

Product	Range	V_{CC} Range (V)	Speed (ns)	Power Dissipation			
				Operating I_{CC}, (mA), f = f_{max}		Standby, I_{SB2} (µA)	
				Typ [4]	Max	Typ [4]	Max
CY62167G30	Automotive-E	2.2 V–3.6 V	55	29.0	40.0	5.5	75.0
	Automotive-A		45	29.0	36.0	5.5	16.0

Notes
2. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
3. The BYTE pin in the 48-pin TSOP I package must be tied to V_{CC} to use the device as a 1M × 16 SRAM. The 48-pin TSOP I package can also be used as a 2M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2 M × 8 configuration, pin 45 is A20, while BHE, BLE and I/O_8 to I/O_{14} pins are not used.
4. Indicates the value for the center of Distribution at 3.0 V, 25 °C and not 100% tested.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential [5] ..... –0.5 V to V_{CC} + 0.5 V

DC voltage applied to outputs in HI-Z state [5] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage [5] ..... –0.5 V to V_{CC} + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Automotive-E	–40 °C to +125 °C	2.2 V to 3.6 V
Automotive-A	–40 °C to +85 °C	

DC Electrical Characteristics

Over the Operating Range

Parameter	Description		Test Conditions		55 ns (Automotive-E)			45 ns (Automotive-A)			Unit
					Min	Typ [6]	Max	Min	Typ [6]	Max	
V_{OH}	Output HIGH voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –0.1 mA		2.0	–	–	2.0	–	–	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.4	–	–	2.4	–	–	
V_{OL}	Output LOW voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.4	–	–	0.4	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	–	–	0.4	
V_{IH}	Input HIGH voltage[5]	2.2 V to 2.7 V	–		1.8	–	V_{CC} + 0.3	1.8	–	V_{CC} + 0.3	V
		2.7 V to 3.6 V	–		2.0	–	V_{CC} + 0.3	2.0	–	V_{CC} + 0.3	
V_{IL}	Input LOW voltage[5]	2.2 V to 2.7 V	–		–0.3	–	0.6	–0.3	–	0.6	V
		2.7 V to 3.6 V	–		–0.3	–	0.8	–0.3	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–4.0	–	+4.0	–1.0	–	+1.0	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–4.0	–	+4.0	–1.0	–	+1.0	µA
I_{CC}	V_{CC} operating supply current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = f_{MAX}	–	29.0	40.0	–	29.0	36.0	mA
				f =1 MHz	–	7.0	18.0	–	7.0	9.0	mA
I_{SB1}[7]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 to 3.6 V		$\overline{CE}_1$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), V_{CC} = $V_{CC(max)}$		–	5.5	75.0	–	5.5	16.0	µA
I_{SB2}[7]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 to 3.6 V		$\overline{CE}_1$ ≥ V_{CC} – 0.2V or CE_2 ≤ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = $V_{CC(max)}$		–	5.5	75.0	–	5.5	16.0	µA

Notes
5. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
6. Indicates the value for the center of Distribution at 3.0 V, 25 °C and not 100% tested.
7. Chip enables ($\overline{CE}_1$ and CE_2) and $\overline{BHE}$, $\overline{BLE}$ and $\overline{BYTE}$ must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

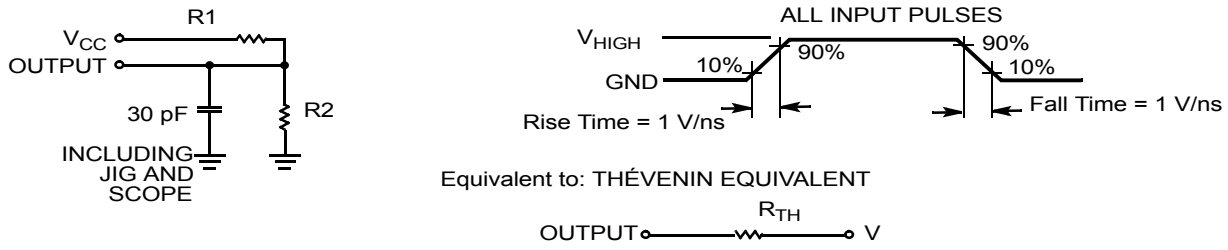
Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	48-ball VFBGA	48-pin TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	31.50	57.99	°C/W
Θ_{JC}	Thermal resistance (junction to case)		15.75	13.42	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	3.0 V	Unit
R1	317	Ω
R2	351	Ω
V_{HIGH}	3.0	V

Note
8. Tested initially and after any design or process changes that may affect these parameters.

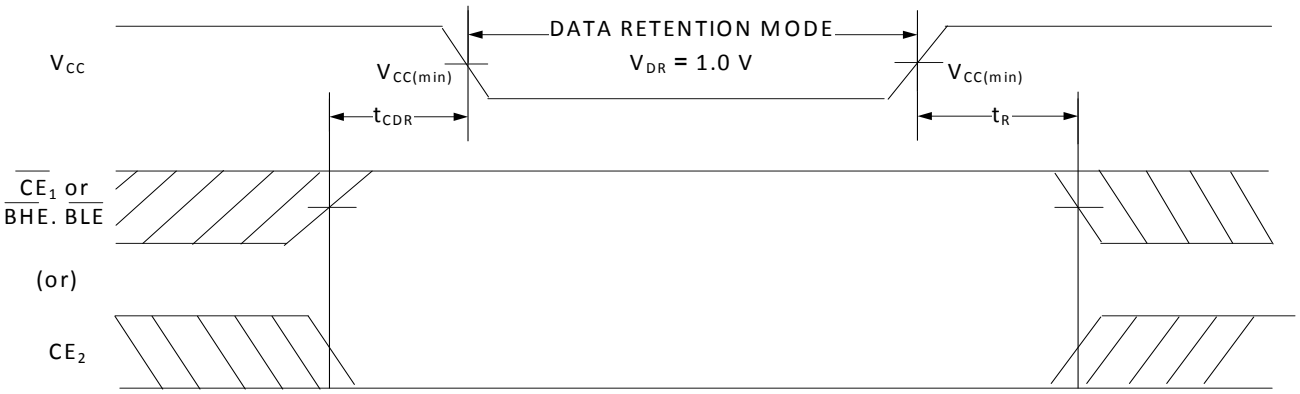
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	55 ns (Automotive-E)			45 ns (Automotive-A)			Unit
			Min	Typ [9]	Max	Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	–	1	–	–	V
I_{CCDR}[10]	Data-retention current	2.2 V < $V_{CC} \leq$ 3.6 V $\overline{CE_1} \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	5.5	75.0	–	5.5	16.0	µA
t_{CDR}[11]	Chip deselect to data-retention time		0	–	–	0	–	–	–
t_R[12]	Operation-recovery time		55	–	–	45	–	–	ns

Data Retention Waveform

Figure 4. Data-Retention Waveform [13]



Notes

9. Indicates the value for the center of distribution at 3.0 V, 25°C and not 100% tested.
10. Chip enables ($\overline{CE_1}$ and CE_2) and $\overline{BYTE}$ must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
13. $\overline{BHE}$.$\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Parameter [14]	Description	55 ns (Automotive-E)		45 ns (Automotive-A)		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	55	–	45	–	ns
t_{AA}	Address to data valid	–	55	–	45	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid / $\overline{CE}$ LOW	–	55	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid / $\overline{OE}$ LOW	–	25	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [15]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [15, 16]	–	20	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z [15]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z [15, 16]	–	20	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down	–	55	–	45	ns
t_{DBE}	BLE / BHE LOW to data valid	–	55	–	45	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z [15]	5	–	5	–	ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High Z [15, 16]	–	20	–	18	ns
Write Cycle [17]						
t_{WC}	Write cycle time	55	–	45	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	40	–	35	–	ns
t_{AW}	Address setup to write end	40	–	35	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	40	–	35	–	ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	40	–	35	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [15, 16]	–	20	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [15]	10	–	10	–	ns

Notes

14. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
16. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
17. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write. Any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

Switching Waveforms

Figure 5. Read Cycle No. 1 of CY62167G (Address Transition Controlled) [18, 19]

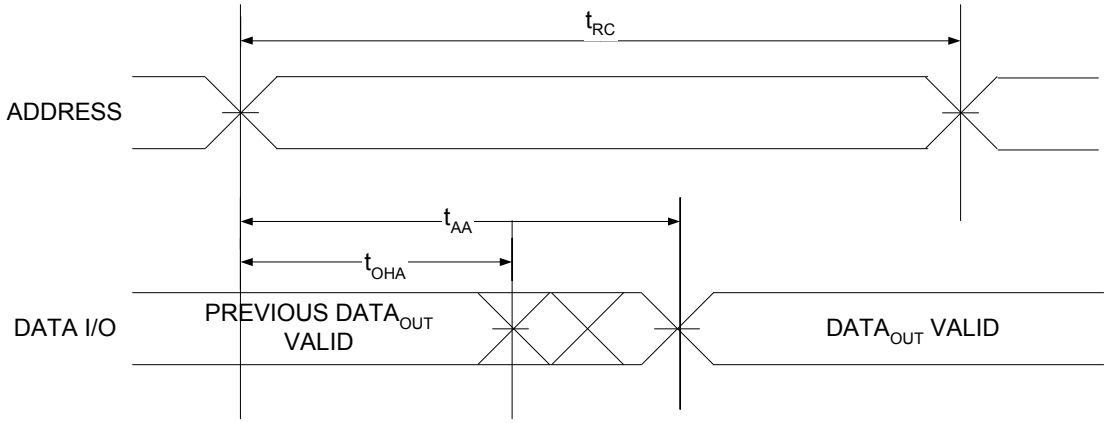
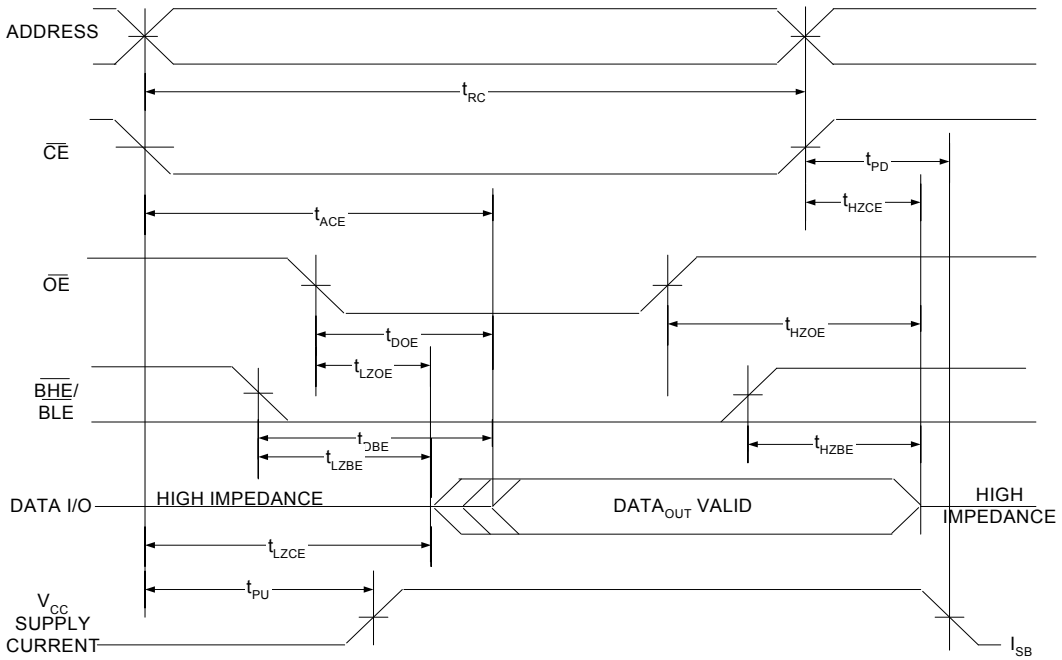


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [19, 20, 21]

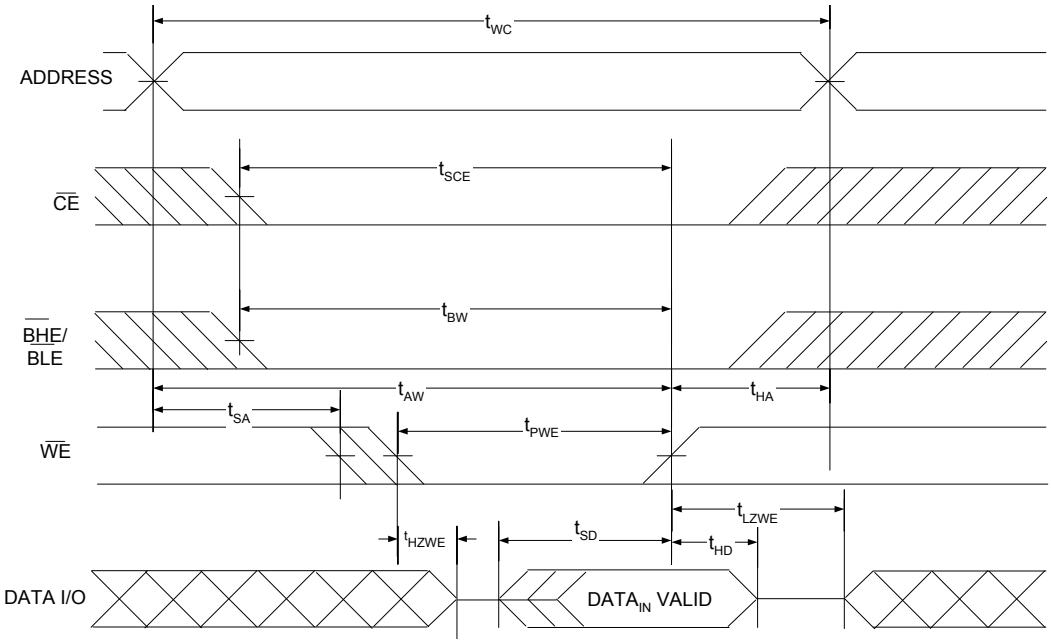


Notes

18. The device is continuously selected. $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}.
19. $\overline{WE}$ is HIGH for read cycle.
20. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
21. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{WE}$ Controlled) [22, 23, 24]

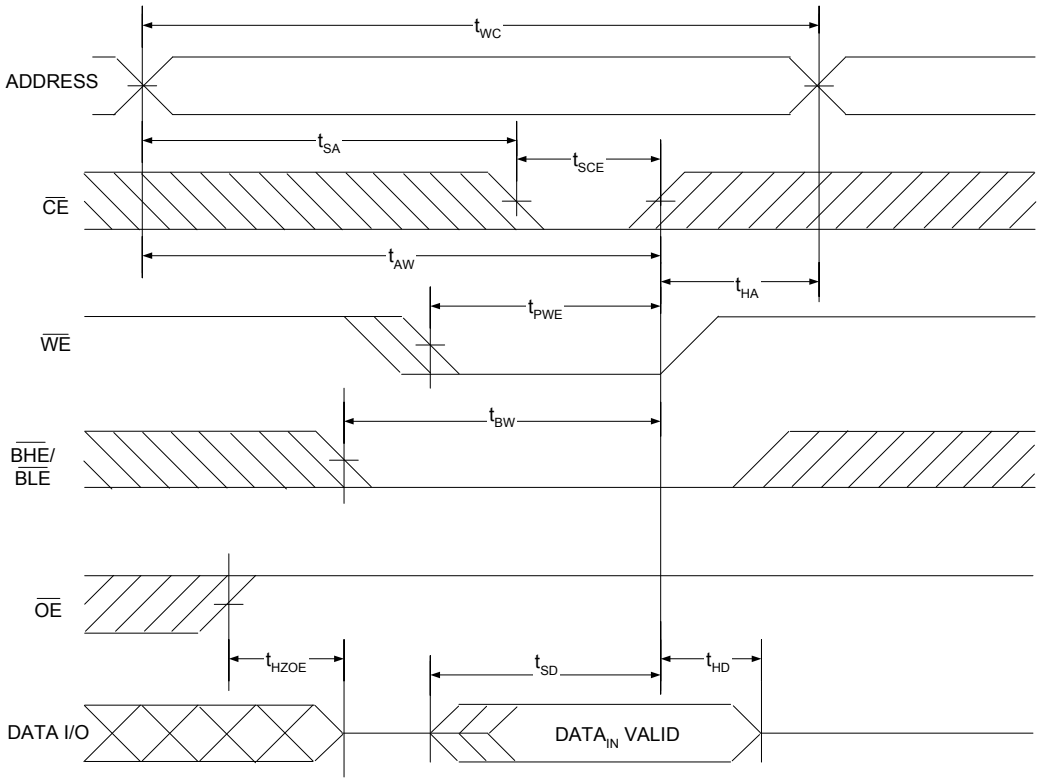


Notes

22. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
23. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
24. Data I/O is in HI-Z state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 2 ($\overline{CE}$ Controlled) [25, 26, 27]

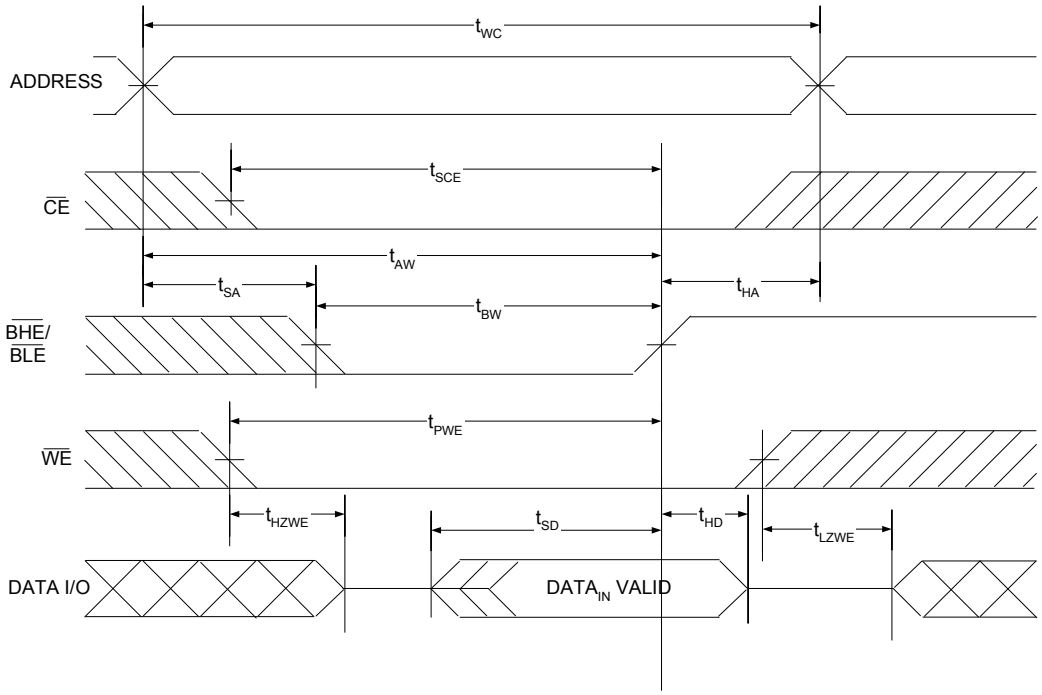


Notes

25. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
26. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
27. Data I/O is in high impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW) [28, 29, 30]



Notes

28. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
29. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
30. Data I/O is in high impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.

Truth Table – CY62167G

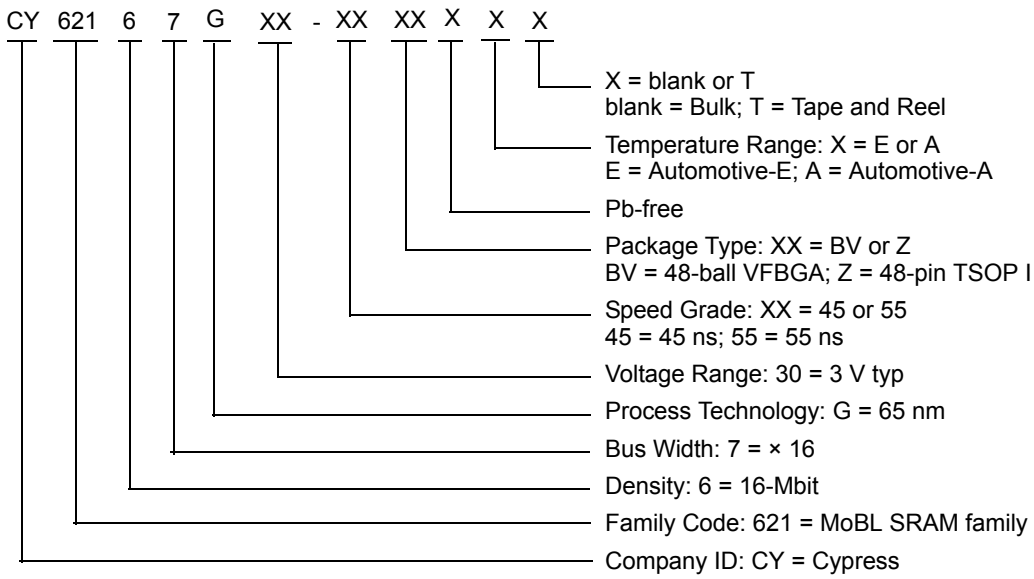
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X[31]	X	X	X	X	HI-Z	Deselect/Power-down	Standby (I_{SB})
X[31]	L	X	X	X	X	HI-Z	Deselect/Power-down	Standby (I_{SB})
X[31]	X[31]	X	X	H	H	HI-Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); HI-Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	HI-Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	X	X	HI-Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); HI-Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	HI-Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

Note
31. The ‘X’ (Don’t care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

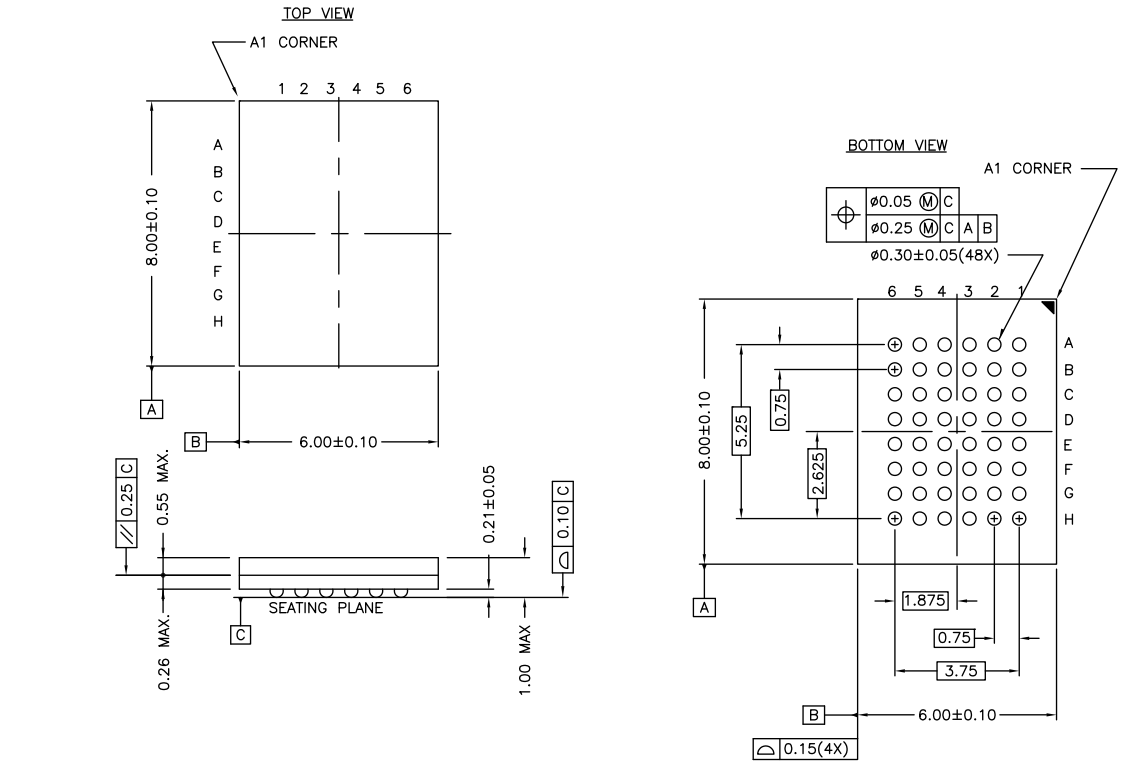
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62167G30-55BVXE	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	Automotive-E
	CY62167G30-55BVXET			
	CY62167G30-55ZXE	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) (Pb-free), Package Code: Z48A	
	CY62167G30-55ZXET			
45	CY62167G30-45ZXA	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) (Pb-free), Package Code: Z48A	Automotive-A
	CY62167G30-45ZXAT			
	CY62167G30-45BVXA	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	
	CY62167G30-45BVXAT			

Ordering Code Definitions



Package Diagram

Figure 10. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150

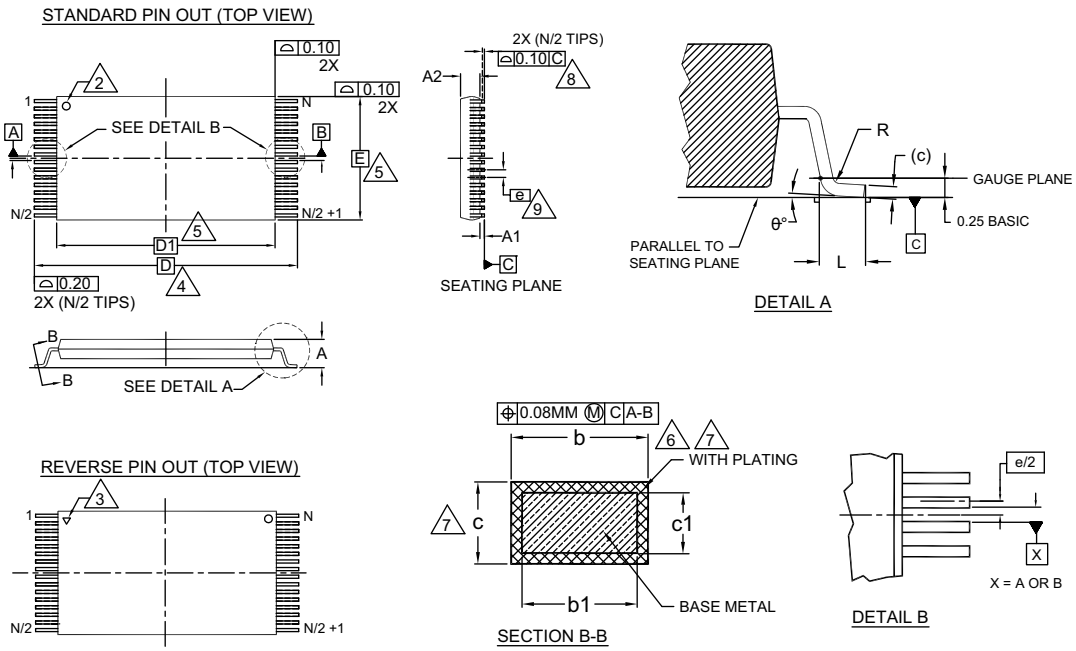


NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Package Diagram (continued)

Figure 11. 48-pin TSOP I (18.4 × 12 × 1.2 mm) Package Outline, 51-85183



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

Acronyms

Acronym	Description
$\overline{BHE}$	byte high enable
$\overline{BLE}$	byte low enable
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
VFBGA	very fine-pitch ball grid array
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
MHz	megahertz
µA	microamperes
µs	microseconds
mA	milliamperes
mm	millimeters
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

Document History Page

Document Title: CY62167G Automotive, 16-Mbit (1M Words × 16-Bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-84902				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*C	5083752	NILE	01/13/2016	Changed status from Preliminary to Final.
*D	5130998	NILE	02/12/2016	Updated Logic Block Diagram – CY62167G. Updated Pin Configurations: Added Note 3 and referred the same note in Figure 2. Updated DC Electrical Characteristics: Updated Note 7. Updated Data Retention Characteristics: Updated Note 10.
*E	5555173	VINI	01/18/2017	Updated Features: Added “AEC-Q100 qualified”. Updated Maximum Ratings: Updated Note 5 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics: Replaced “55 ns (Automotive-E)” with “45 ns (Automotive-A)” in column heading. Replaced “55 ns (Automotive-A)” with “55 ns (Automotive-E)” in column heading. Changed minimum value of V_{OH} parameter from 2.2 V to 2.4 V corresponding to Operating Range “2.7 V to 3.6 V”. Changed minimum value of V_{IH} parameter from 2.0 V to 1.8 V corresponding to Operating Range “2.2 V to 2.7 V”. Updated Ordering Information: Updated part numbers. Updated Ordering Code Definitions. Updated Package Diagram: spec 51-85183 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*F	5725191	NILE	05/03/2017	Updated DC Electrical Characteristics: Fixed typo in values of I_{IX} and I_{OZ} parameters (both “Min” and “Max” columns). Fixed typo in values of I_{SB1} and I_{SB2} parameters (only “Max” column). Updated Data Retention Characteristics: Fixed typo in values of I_{CCDR} parameter (only “Max” column). Updated to new template.

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