Contents

Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [2]	Max		Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62147EV30LL	Automotive-A	2.2	3.0	3.6	45 ns	2	2.5	15	20	1	7
	Automotive-E	2.2	3.0	3.6	55 ns	2	3	15	25	1	20

Note

[2] Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Pin Configurations

Figure 1. 48-Ball VFBGA Pinout (Single Chip Enable) [3, 4]

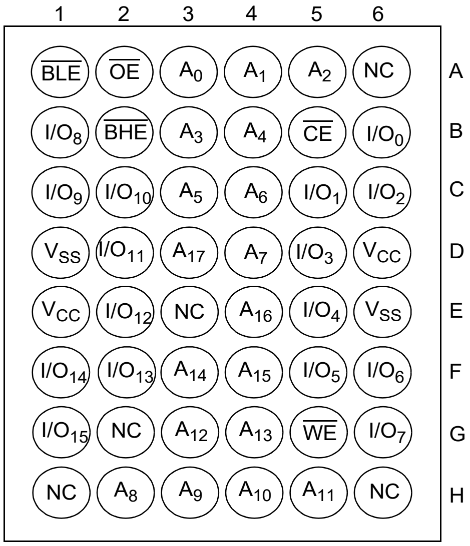


Figure 2. 48-Ball VFBGA Pinout (Dual Chip Enable) [3, 4]

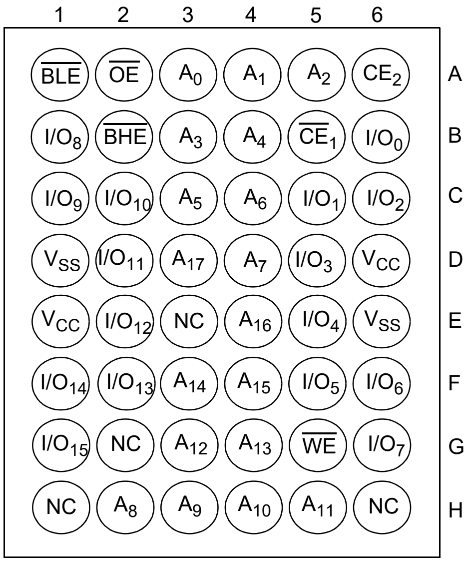
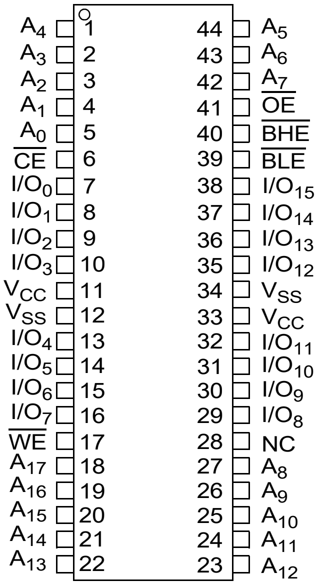


Figure 3. 44-Pin TSOP II Pinout [3]



Notes

[3] NC pins are not connected on the die.

[4] Pins H1, G2, and H6 in the BGA package are address expansion pins for 8Mb, 16Mb, and 32Mb, respectively.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to + 150 °C

Ambient temperature with power applied .... –55 °C to + 125 °C

Supply voltage to ground potential ....–0.3 V to + 3.9 V (V_{CCmax} + 0.3 V)

DC voltage applied to outputs in High Z state [5, 6] ....–0.3 V to 3.9 V (V_{CCmax} + 0.3 V)

DC input voltage [5, 6]..........–0.3 V to 3.9 V (V_{CCmax} + 0.3 V)

Output current into outputs (LOW) .... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) .... >2001 V

Latch-up current .... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [7]
CY62147EV30LL	Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V
	Automotive-E	–40 °C to +125 °C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Automotive-A)			55 ns (Automotive-E)			Unit
			Min	Typ [8]	Max	Min	Typ [8]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA	2.0	–	–	2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V	2.4	–	–	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA	–	–	0.4	–	–	0.4	V
		I_{OL} = 2.1 mA, V_{CC} = 2.70 V	–	–	0.4	–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2.7 V	1.8	–	V_{CC} + 0.3	1.8	–	V_{CC} + 0.3	V
		V_{CC}= 2.7 V to 3.6 V	2.2	–	V_{CC} + 0.3	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V	–0.3	–	0.6	–0.3	–	0.6	V
		V_{CC}= 2.7 V to 3.6 V	–0.3	–	0.8	–0.3		0.8	V
I_{IX}	Input leakage current	GND $\leq V_I \leq V_{CC}$	–1	–	+1	–4	–	+4	µA
I_{OZ}	Output leakage current	GND $\leq V_O \leq V_{CC}$, output disabled	–1	–	+1	–4	–	+4	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = 1/t_{RC} V_{CC} = $V_{CC(max)}$ I_{OUT} = 0 mA CMOS levels	–	15	20	–	15	25	mA
		f = 1 MHz	–	2	2.5	–	2	3	
I_{SB1}	Automatic CE power-down current – CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), V_{CC} = 3.60 V	–	1	7	–	1	20	µA
I_{SB2} [9]	Automatic CE power-down current – CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, V_{CC} = 3.60 V	–	1	7	–	1	20	µA

Notes

5. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
6. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
7. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
9. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

For all packages.

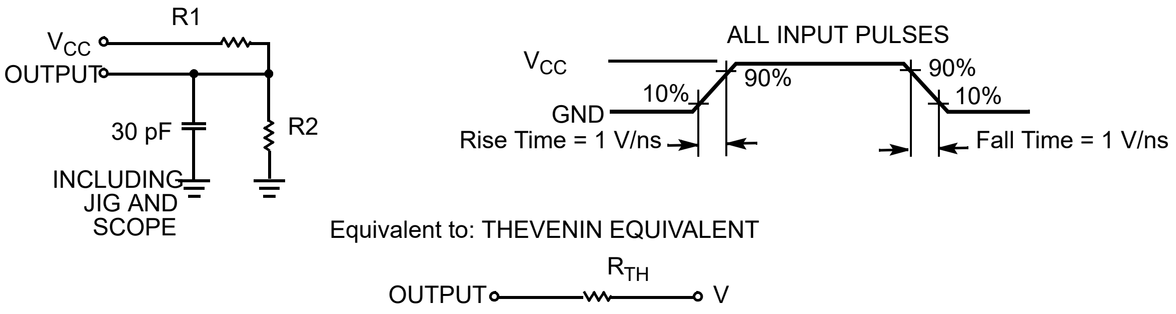
Parameter [10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25\ °C$, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [10]	Description	Test Conditions	VFBGA Package	TSOP II Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	42.10	55.52	°C/W
Θ_{JC}	Thermal resistance (junction to case)		23.45	16.03	°C/W

AC Test Load and Waveforms

Figure 4. AC Test Load and Waveforms



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note

10. Tested initially and after any design or process changes that may affect these parameters.

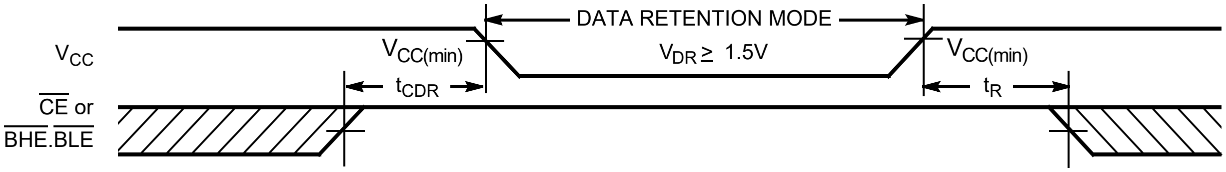
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [11]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR}[12]	Data retention current	V_{CC} = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Automotive-A	–	0.8	7	µA
			Automotive-E	–	–	12	
t_{CDR} [13]	Chip deselect to data retention time			0	–	–	ns
t_R [14]	Operation recovery time		CY62147EV30LL-45	45	–	–	ns
			CY62147EV30LL-55	55	–	–	

Data Retention Waveform

Figure 5. Data Retention Waveform [15, 16]



Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
12. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
15. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
16. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter [17, 18]	Description	45 ns (Automotive-A)		55 ns (Automotive-E)		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{\text{CE}}$ LOW to data valid	–	45	–	55	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{\text{OE}}$ LOW to Low Z [19]	5	–	5	–	ns
t_{HZOE}	$\overline{\text{OE}}$ HIGH to High Z [19, 20]	–	18	–	20	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to Low Z [19]	10	–	10	–	ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to High Z [19, 20]	–	18	–	20	ns
t_{PU}	$\overline{\text{CE}}$ LOW to power-up	0	–	0	–	ns
t_{PD}	$\overline{\text{CE}}$ HIGH to power-down	–	45	–	55	ns
t_{DBE}	$\overline{\text{BLE}}$/$\overline{\text{BHE}}$ LOW to data valid	–	45	–	55	ns
t_{LZBE}	$\overline{\text{BLE}}$/$\overline{\text{BHE}}$ LOW to Low Z [19]	10	–	10	–	ns
t_{HZBE}	$\overline{\text{BLE}}$/$\overline{\text{BHE}}$ HIGH to High Z [19, 20]	–	18	–	20	ns
Write Cycle [21]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{\text{CE}}$ LOW to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{\text{WE}}$ pulse width	35	–	40	–	ns
t_{BW}	$\overline{\text{BLE}}$/$\overline{\text{BHE}}$ LOW to write end	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0		ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High Z [19, 20]	–	18	–	20	ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z [19]	10	–	10	–	ns

---

Notes

17. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 4 on page 6.
18. AC timing parameters are subject to byte enable signals ($\overline{\text{BHE}}$ or $\overline{\text{BLE}}$) not switching when chip is disabled. See application note AN13842 for further clarification.
19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
20. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
21. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}}$, $\overline{\text{CE}}$ = V_{IL}, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$, or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

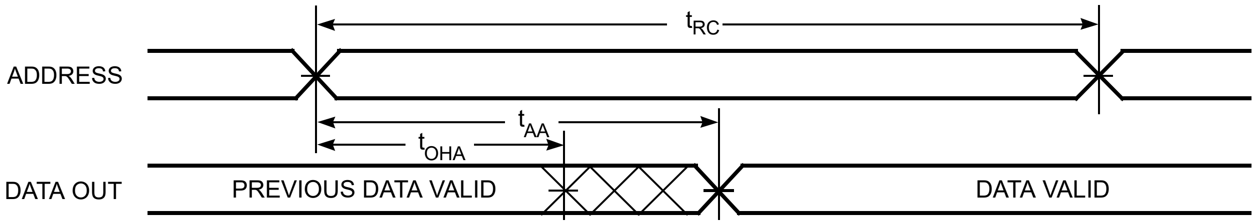


Figure 6. Read Cycle No. 1: Address Transition Controlled [22, 23]

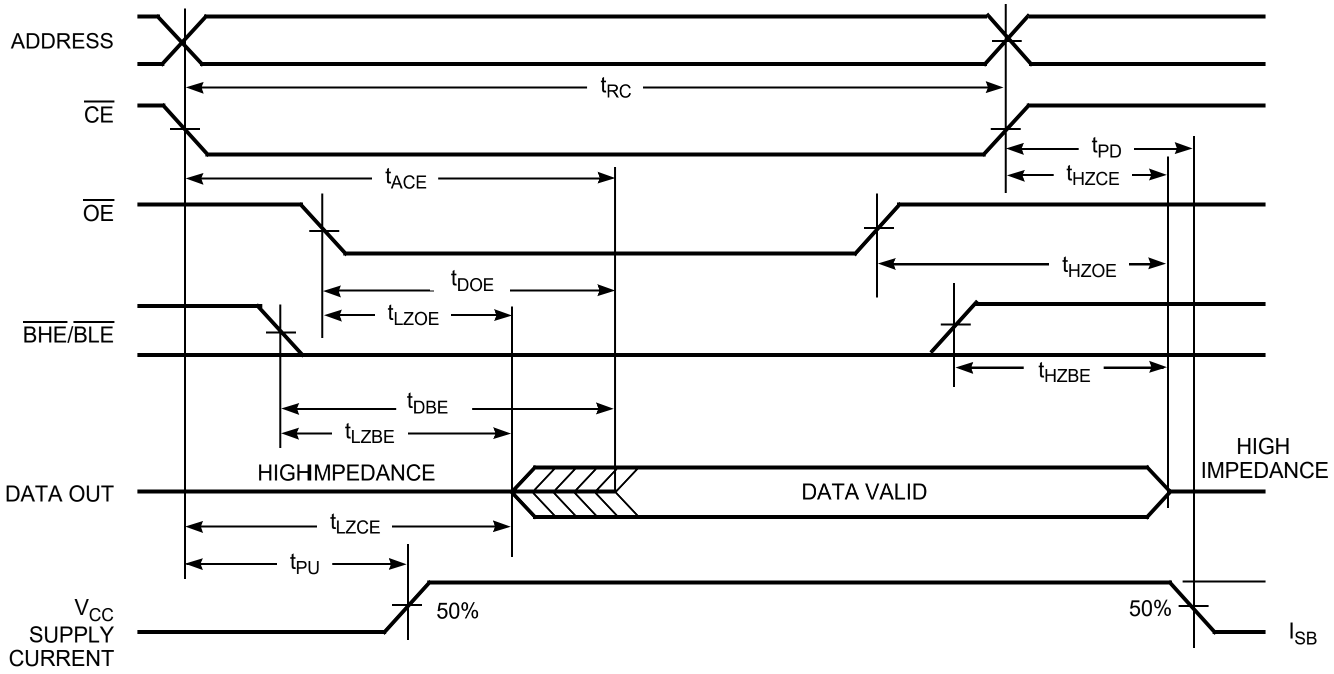


Figure 7. Read Cycle No. 2: $\overline{OE}$ Controlled [23, 24, 25]

Notes

22. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}.
23. $\overline{WE}$ is HIGH for read cycle.
24. BGA packaged device is offered in single CE and dual CE options. In this datasheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
25. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1: $\overline{WE}$ Controlled [26, 27, 28, 29]

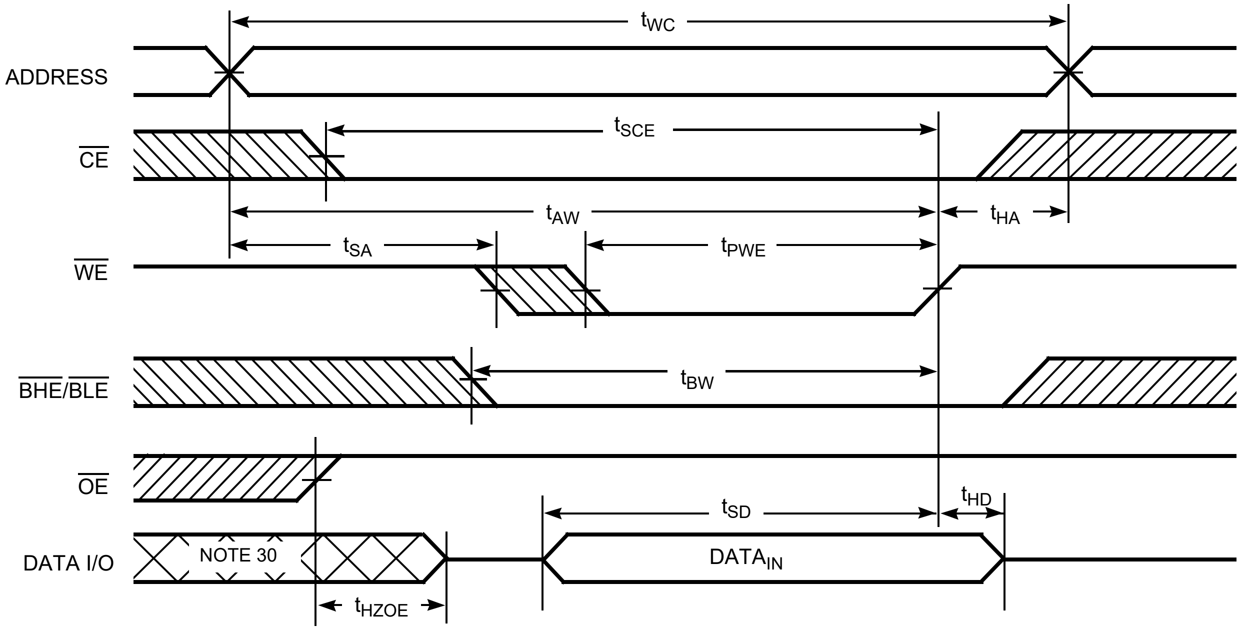
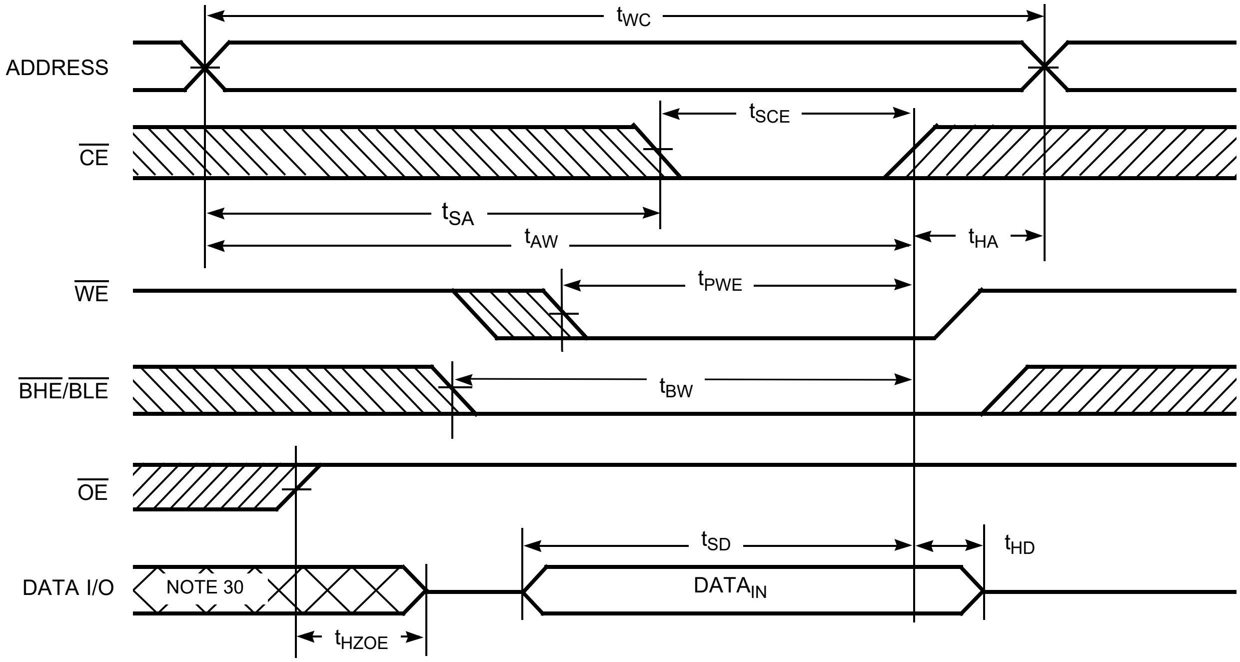


Figure 9. Write Cycle No. 2: $\overline{CE}$ Controlled [26, 27, 28, 29]



Notes

[26] BGA packaged device is offered in single CE and dual CE options. In this datasheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.

[27] The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$, $\overline{BLE}$, or both $= V_{IL}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

[28] Data I/O is high impedance if $\overline{OE} = V_{IH}$.

[29] If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.

[30] During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

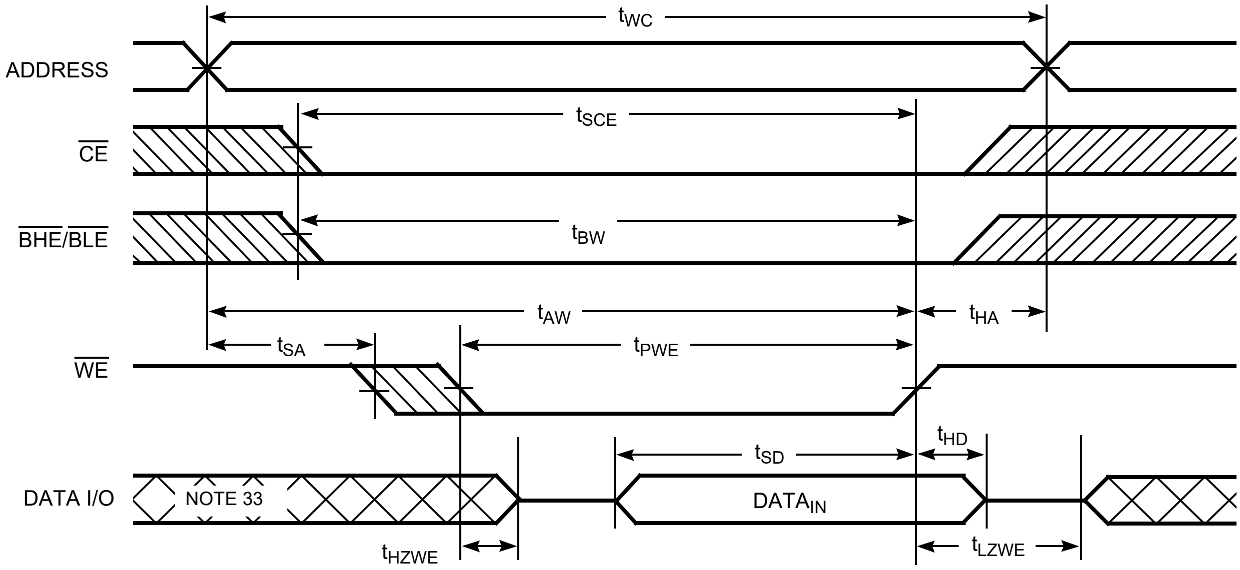


Figure 10. Write Cycle No. 3: $\overline{WE}$ Controlled, $\overline{OE}$ LOW [31, 32]

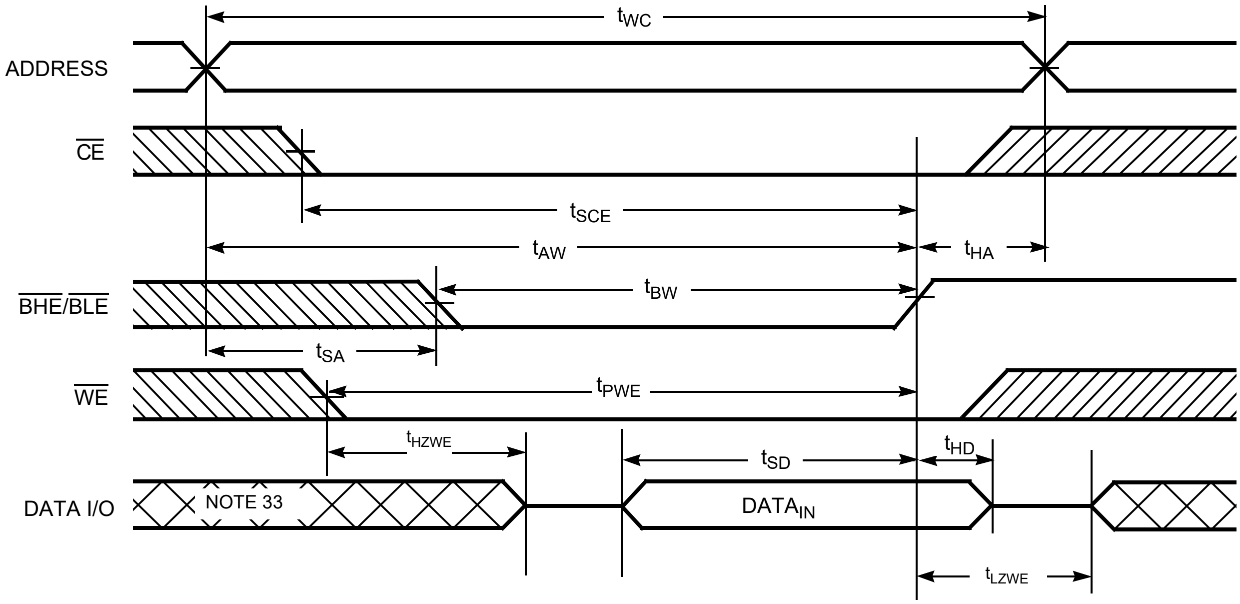


Figure 11. Write Cycle No. 4: $\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW [31, 32]

Notes

31. BGA packaged device is offered in single CE and dual CE options. In this datasheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
32. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high-impedance state.
33. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$ [34, 35]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	I/Os	Mode	Power
H	X	X	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	X	X	H	H	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

Notes

[34] BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.

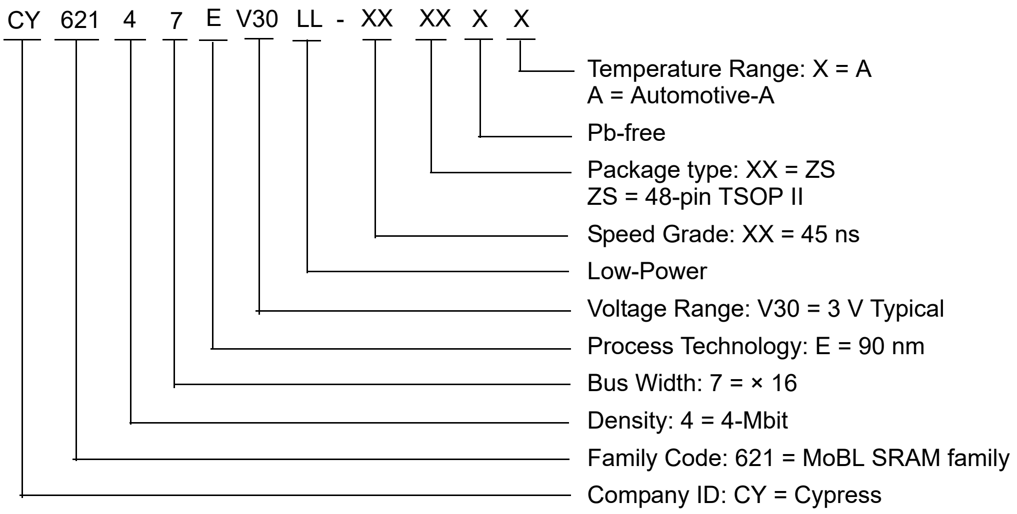
[35] For the Dual Chip Enable device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH. Intermediate voltage levels is not permitted on any of the Chip Enable pins ($\overline{CE}$ for the Single Chip Enable device; $\overline{CE}_1$ and CE_2 for the Dual Chip Enable device).

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62147EV30LL-45ZSXA	51-85087	44-pin TSOP II (Pb-free)	Automotive-A

Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions

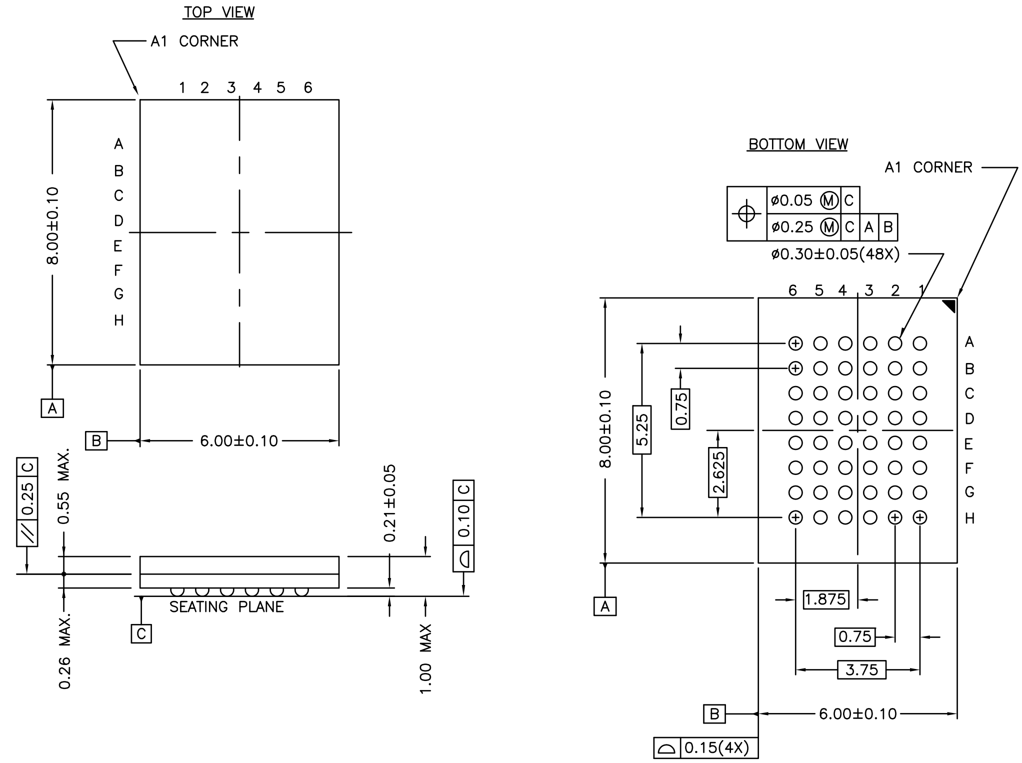


CY 621 4 7 E V30 LL - XX XX X X

Temperature Range: X = A
A = Automotive-A
Pb-free
Package type: XX = ZS
ZS = 48-pin TSOP II
Speed Grade: XX = 45 ns
Low-Power
Voltage Range: V30 = 3 V Typical
Process Technology: E = 90 nm
Bus Width: 7 = × 16
Density: 4 = 4-Mbit
Family Code: 621 = MoBL SRAM family
Company ID: CY = Cypress

Package Diagrams

Figure 12. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



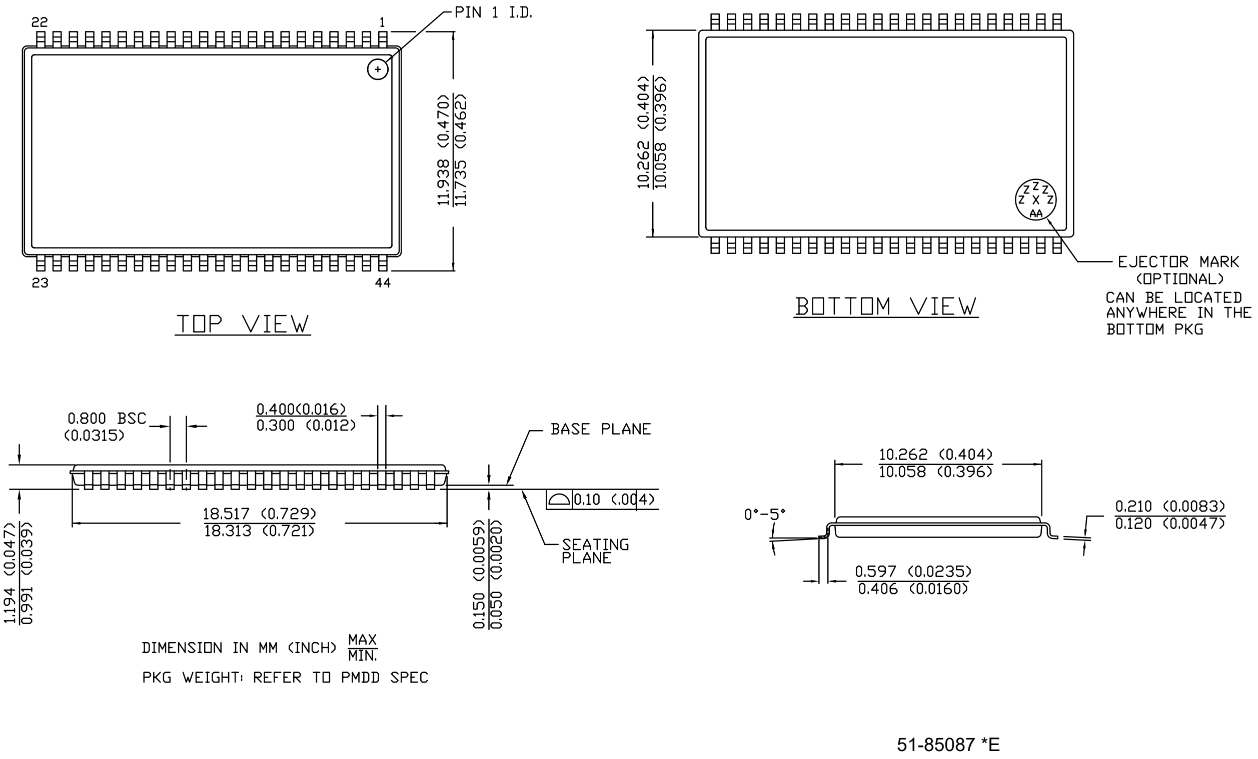
NOTE:

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 13. 44-pin TSOP Z44-II Package Outline, 51-85087



Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
SRAM	Static Random Access Memory
VFBGA	Very Fine-Pitch Ball Grid Array
TSOP	Thin Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62147EV30 MoBL® Automotive, 4-Mbit (256K × 16) Static RAM Document Number: 001-66256				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3123973	RAME	01/31/2011	Created new datasheet for Automotive parts from document number 38-05440 Rev. *I
*A	3937956	MEMJ	03/19/2013	Updated Package Diagrams: spec 51-85150 – Changed revision from *F to *H. spec 51-85087 – Changed revision from *C to *E. Completing Sunset Review.
*B	4725832	PSR	04/15/2015	Updated Functional Description: Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.” at the end. Added “For a complete list of related resources, click here.” at the end. Updated to new template.
*C	5221444	VINI	04/14/2016	Updated Thermal Resistance: Updated details in “Test Conditions” column and updated all values in “VFBGA Package” and “TSOP II Package” columns corresponding to Θ_{JA} and Θ_{JC} parameters. Updated to new template. Completing Sunset Review.
*D	6049466	VINI	01/29/2018	Updated Ordering Information: Updated part numbers. Removed Note “This BGA package is offered with single chip enable.” and its reference. Removed Note “This BGA package is offered with dual chip enable.” and its reference. Updated Ordering Code Definitions. Updated to new template. Completing Sunset Review.

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