

CAT811, CAT812

Table 1. THRESHOLD SUFFIX SELECTOR DESCRIPTION

| Nominal Threshold Voltage | Threshold Suffix Designation |
|---------------------------|------------------------------|
| 4.63 V | L |
| 4.38 V | M |
| 4.00 V | J |
| 3.08 V | T |
| 2.93 V | S |
| 2.63 V | R |
| 2.32 V | Z |

Table 2. PIN DESCRIPTION

| Pin Number | | Pin Name | Description |
|------------|--------|---------------------------|--|
| CAT811 | CAT812 | | |
| 1 | 1 | GND | Ground. |
| 2 | - | $\overline{\text{RESET}}$ | Active LOW reset. $\overline{\text{RESET}}$ is asserted if V_{CC} falls below the reset threshold and remains low for at least 140 ms after V_{CC} rises above the reset threshold. |
| - | 2 | RESET | Active HIGH reset. RESET is asserted if V_{CC} falls below the reset threshold and remains high for at least 140 ms after V_{CC} rises above the reset threshold. |
| 3 | 3 | MR | Manual Reset Input. A logic LOW on MR asserts RESET. RESET remains active as long as MR is LOW and for 140 ms after MR returns HIGH. The active low input has an internal 20 kΩ pull-up resistor. The input should be left open if not used. |
| 4 | 4 | V_{CC} | Power supply voltage that is monitored. |

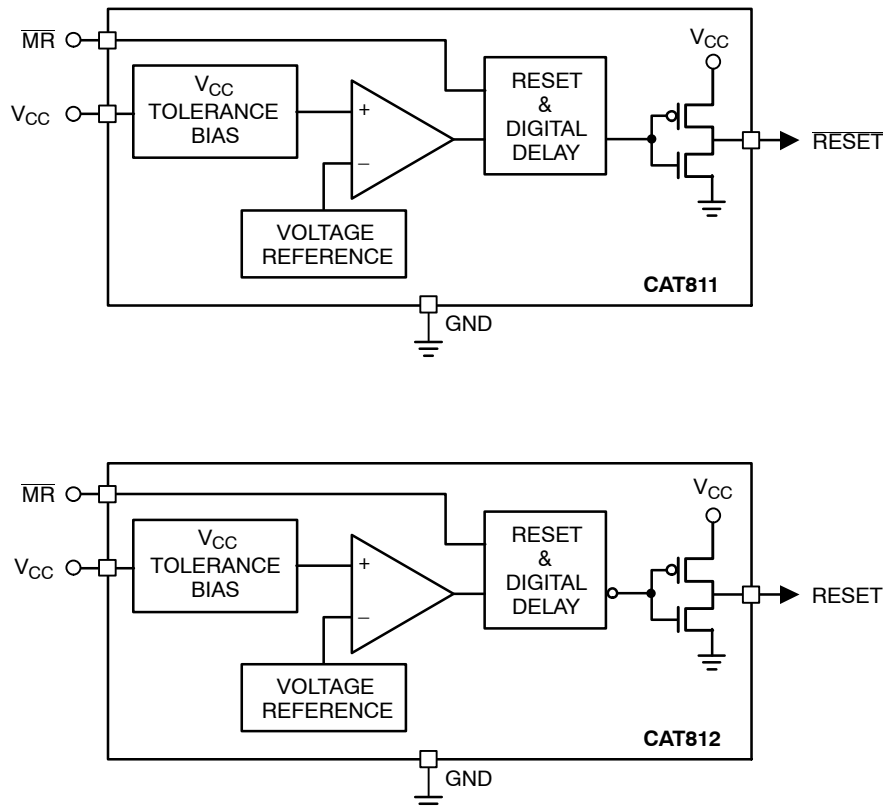


Figure 1. Block Diagrams

CAT811, CAT812

Table 3. ABSOLUTE MAXIMUM RATINGS

| Parameters | Ratings | Units |
|---|--------------|--------------|
| Any pin with respect to ground | -0.3 to +6.0 | V |
| Input Current, V_{CC} | 20 | mA |
| Output Current RESET, $\overline{\text{RESET}}$ | 20 | mA |
| Rate of Raise, V_{CC} | 100 | V/ μ s |
| Continuous Power Dissipations Derate 4 mW/ $^{\circ}$ C above +70 $^{\circ}$ C (SOT-143) | 320 | mW |
| Storage Temperature Range | -65 to +105 | $^{\circ}$ C |
| Operating Ambient Temperature Range | -40 to +85 | $^{\circ}$ C |
| Lead Soldering Temperature (10 seconds) | +300 | $^{\circ}$ C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. ELECTRICAL OPERATING CHARACTERISTICS

(V_{CC} = Full range, T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C unless otherwise noted. Typical values at T_A = +25 $^{\circ}$ C and V_{CC} = 5 V for the L/M/J versions, V_{CC} = 3.3 V for the T/S versions, V_{CC} = 3 V for the R version and V_{CC} = 2.5 V for the Z version.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | |
|----------------------------------|--|--|--|------|------|-------------------|---------|
| V_{CC} Range | | T_A = 0 $^{\circ}$ C to +70 $^{\circ}$ C | 1.0 | | 5.5 | V | |
| | | T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C | 1.2 | | 5.5 | | |
| Supply Current | I_{CC} | T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C | V_{CC} < 5.5 V, J/L/M | | 8 | 20 | μ A |
| | | | V_{CC} < 3.6 V, R/S/T/Z | | 6 | 15 | |
| Reset Threshold Voltage | V_{TH} | L Threshold | T_A = +25 $^{\circ}$ C | 4.56 | 4.63 | 4.70 | V |
| | | | T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C | 4.50 | | 4.75 | |
| | | M Threshold | T_A = +25 $^{\circ}$ C | 4.31 | 4.38 | 4.45 | |
| | | | T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C | 4.25 | | 4.50 | |
| | | J Threshold | T_A = +25 $^{\circ}$ C | 3.93 | 4.00 | 4.06 | |
| | | | T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C | 3.89 | | 4.10 | |
| | | T Threshold | T_A = +25 $^{\circ}$ C | 3.04 | 3.08 | 3.11 | |
| | | | T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C | 3.00 | | 3.15 | |
| | | S Threshold | T_A = +25 $^{\circ}$ C | 2.89 | 2.93 | 2.96 | |
| | | | T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C | 2.85 | | 3.00 | |
| | | R Threshold | T_A = +25 $^{\circ}$ C | 2.59 | 2.63 | 2.66 | |
| | | | T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C | 2.55 | | 2.70 | |
| Z Threshold | T_A = +25 $^{\circ}$ C | 2.28 | 2.32 | 2.35 | | | |
| | T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C | 2.25 | | 2.38 | | | |
| Reset Threshold Tempco | | | | 30 | | ppm/ $^{\circ}$ C | |
| V_{CC} to Reset Delay (Note 3) | | $V_{CC} = V_{TH}$ to ($V_{TH} - 100$ mV) | | 20 | | μ s | |
| Reset Active Timeout Period | | T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C | 140 | 240 | 400 | ms | |

1. Production testing done at T_A = +25 $^{\circ}$ C; limits over temperature guaranteed by design only.
2. Glitches of 100 ns or less typically will not generate a reset pulse.
3. $\overline{\text{RESET}}$ output for the CAT811; RESET output for the CAT812.

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Table 4. ELECTRICAL OPERATING CHARACTERISTICS

(V_{CC} = Full range, T_A = -40°C to $+85^{\circ}\text{C}$ unless otherwise noted. Typical values at T_A = $+25^{\circ}\text{C}$ and V_{CC} = 5 V for the L/M/J versions, V_{CC} = 3.3 V for the T/S versions, V_{CC} = 3 V for the R version and V_{CC} = 2.5 V for the Z version.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|----------|--|----------------|-----|--------------|------------------|
| RESET Output Voltage Low (Push-pull, active LOW, CAT811) | V_{OL} | $V_{CC} = V_{TH \min}$, $I_{SINK} = 1.2 \text{ mA}$ CAT811R/S/T/Z | | | 0.3 | V |
| | | $V_{CC} = V_{TH \min}$, $I_{SINK} = 3.2 \text{ mA}$ CAT811J/L/M | | | 0.4 | |
| | | $V_{CC} > 1.0 \text{ V}$, $I_{SINK} = 50 \mu\text{A}$ | | | 0.3 | |
| RESET Output Voltage High (Push-pull, active LOW, CAT811) | V_{OH} | $V_{CC} = V_{TH \max}$, $I_{SOURCE} = 500 \mu\text{A}$ CAT811R/S/T/Z | $0.8V_{CC}$ | | | V |
| | | $V_{CC} = V_{TH \max}$, $I_{SOURCE} = 800 \mu\text{A}$ CAT811J/L/M | $V_{CC} - 1.5$ | | | V |
| RESET Output Voltage Low (Push-pull, active HIGH, CAT812) | V_{OL} | $V_{CC} > V_{TH \max}$, $I_{SINK} = 1.2 \text{ mA}$ CAT812R/S/T/Z | | | 0.3 | V |
| | | $V_{CC} > V_{TH \max}$, $I_{SINK} = 3.2 \text{ mA}$ CAT812J/L/M | | | 0.4 | |
| RESET Output Voltage High (Push-pull active HIGH, CAT812) | V_{OH} | $1.8 \text{ V} < V_{CC} \leq V_{TH \min}$, $I_{SOURCE} = 150 \mu\text{A}$ | $0.8V_{CC}$ | | | V |
| $\overline{\text{MR}}$ Minimum Pulse Width | t_{MR} | | 10 | | | μs |
| $\overline{\text{MR}}$ Glitch Immunity | | (Note 2) | | 100 | | ns |
| $\overline{\text{MR}}$ to RESET Propagation Delay | t_{MD} | (Note 3) | | 0.5 | | μs |
| $\overline{\text{MR}}$ Input Threshold | V_{IH} | $V_{CC} > V_{TH (MAX)}$, CAT811/812L/M/J | 2.3V | | | V |
| | V_{IL} | | | | 0.8 | |
| | V_{IH} | $V_{CC} > V_{IH (MAX)}$, CAT811/812R/S/T/Z | $0.7V_{CC}$ | | | |
| | V_{IL} | | | | $0.25V_{CC}$ | |
| $\overline{\text{MR}}$ Pull-up Resistance | | | 10 | 20 | 75 | $\text{k}\Omega$ |

1. Production testing done at T_A = $+25^{\circ}\text{C}$; limits over temperature guaranteed by design only.
2. Glitches of 100 ns or less typically will not generate a reset pulse.
3. RESET output for the CAT811; RESET output for the CAT812.

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TYPICAL OPERATING CHARACTERISTICS

(V_{CC} = Full range, T_A = -40°C to $+85^{\circ}\text{C}$ unless otherwise noted. Typical values at T_A = $+25^{\circ}\text{C}$ and V_{CC} = 5 V for the L/M/J versions, V_{CC} = 3.3 V for the T/S versions, V_{CC} = 3 V for the R version and V_{CC} = 2.5 V for the Z version.)

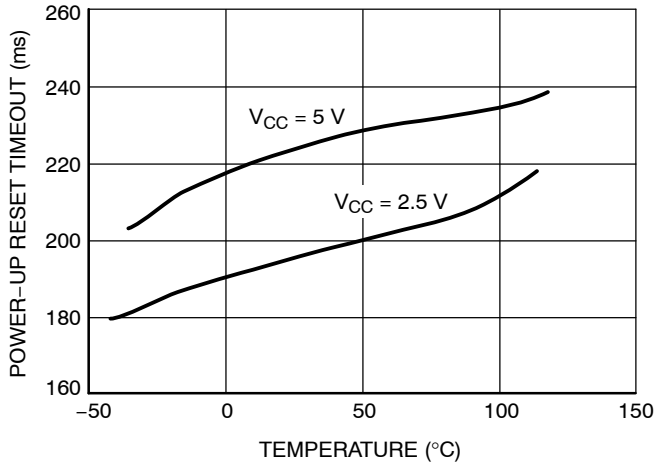


Figure 2. Power-Up Reset Timeout vs. Temperature

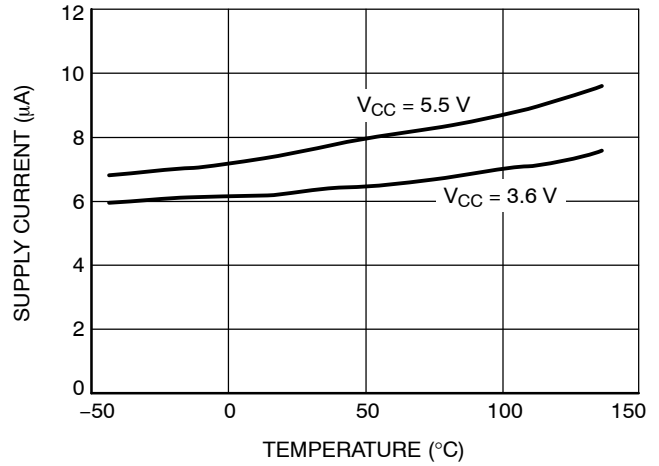


Figure 3. Supply Current vs. Temperature (No Load, CAT8xxR/S/T/Z)

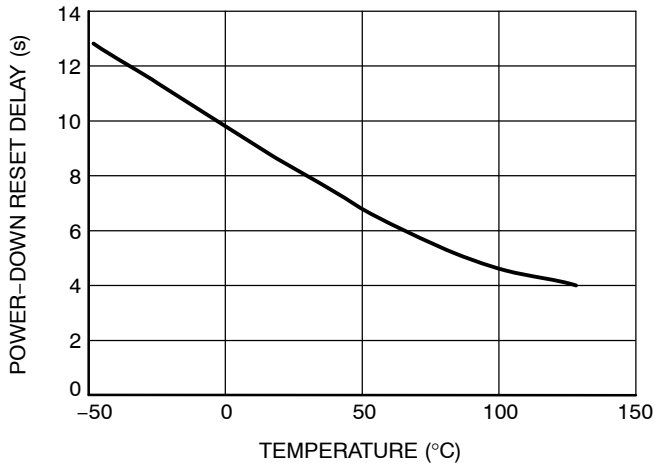


Figure 4. Power-Down Reset Delay vs. Temperature (CAT8xxR/S/T/Z)

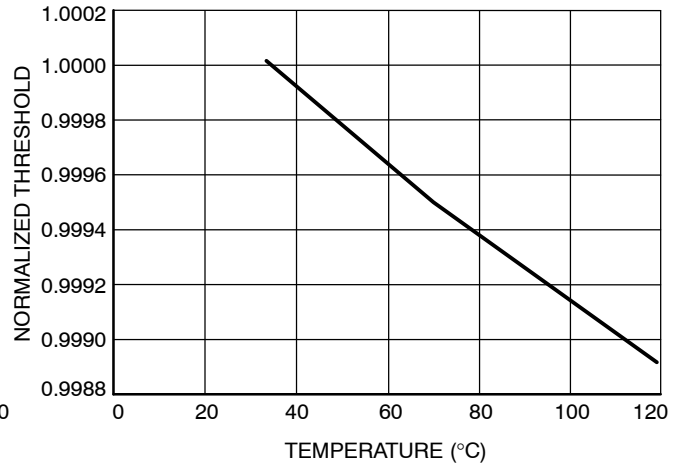


Figure 5. Normalized Reset Threshold vs. Temperature

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DETAILED DESCRIPTION

Reset Timing

The reset signal is asserted LOW for the CAT811 and HIGH for the CAT812 when the power supply voltage falls below the threshold trip voltage and remains asserted for at least 140 ms after the power supply voltage has risen above the threshold.

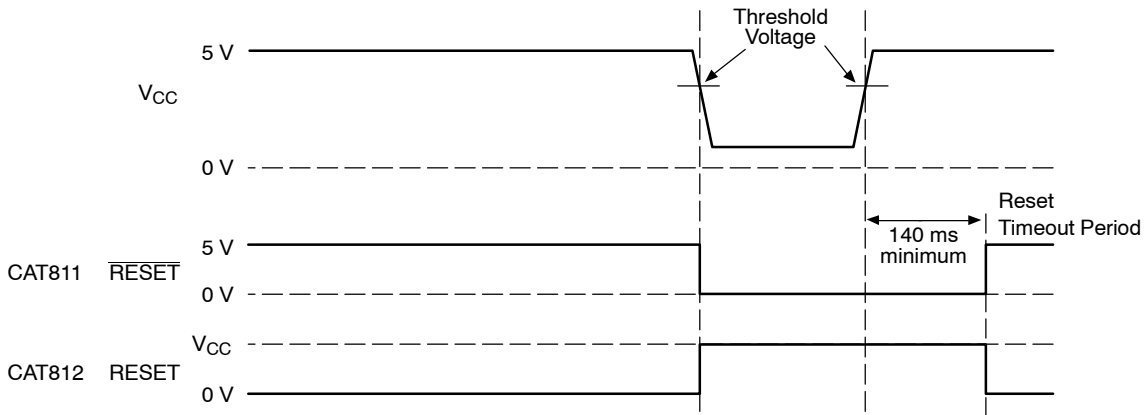


Figure 6. Reset Timing Diagram

V_{CC} Transient Response

The CAT811/812 protect μ Ps against brownout failure. Short duration transients of 4 μ s or less and 100 mV amplitude typically do not cause a false RESET.

Figure 7 shows the maximum pulse duration of negative-going V_{CC} transients that do not cause a reset condition. As the amplitude of the transient goes further below the threshold (increasing $V_{TH} - V_{CC}$), the maximum pulse duration decreases. In this test, the V_{CC} starts from an initial voltage of 0.5 V above the threshold and drops below it by the amplitude of the overdrive voltage ($V_{TH} - V_{CC}$).

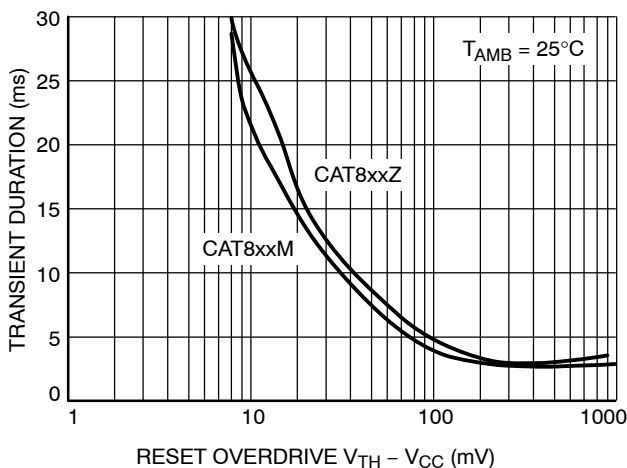


Figure 7. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

Valid Reset with V_{CC} under 1.0 V

To ensure that the CAT811 $\overline{\text{RESET}}$ pin is in a known state when V_{CC} is under 1.0 V, a 100 k Ω pull-down resistor between $\overline{\text{RESET}}$ pin and GND is recommended; the value is not critical. For the CAT812, a pull-up resistor from RESET pin to V_{CC} is needed.

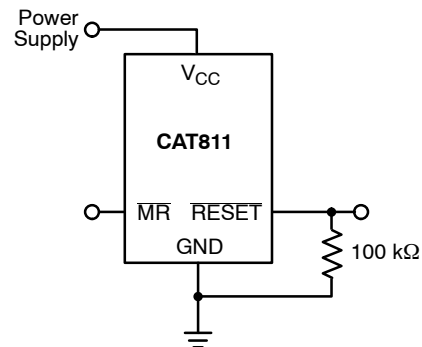


Figure 8. RESET Valid with V_{CC} Under 1.0 V

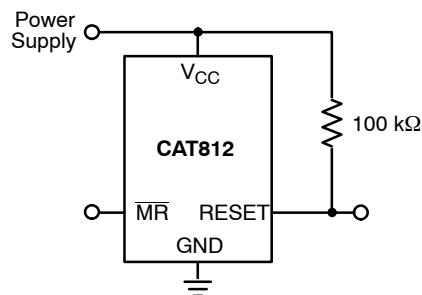


Figure 9. RESET Valid with V_{CC} Under 1.1 V

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Bi-directional Reset Pin Interfacing

The CAT811/812 can interface with $\mu\text{P}/\mu\text{C}$ bi-directional reset pins by connecting a 4.7 k Ω resistor in series with the CAT811/812 reset output and the $\mu\text{P}/\mu\text{C}$ bi-directional reset pin.

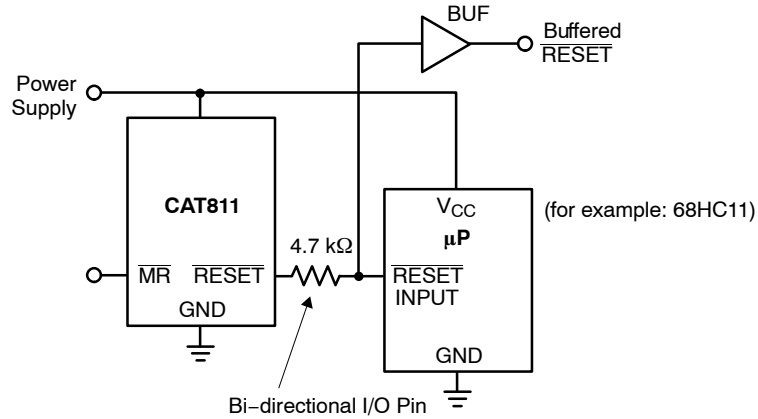


Figure 10. Bi-directional Reset Pin Interfacing

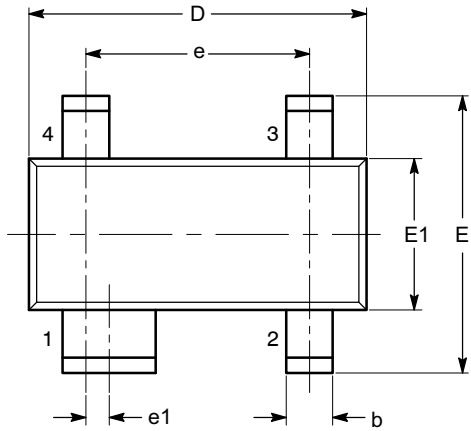
Table 5. OTHER SUPERVISORY PRODUCTS

| Function | CAT1161/3 | CAT1162 | CAT809 | CAT810 | CAT811 | CAT812 |
|-----------------------------------|--------------------|--------------------|-----------------------|-----------------------|---------------|---------------|
| With 16k Bit Serial EEPROM Memory | ✓ | ✓ | | | | |
| Watchdog Timer | ✓ | | | | | |
| Manual Reset Input | ✓ | ✓ | | | ✓ | ✓ |
| Active Low Reset | | | ✓ | | ✓ | |
| Active High Reset | | | | ✓ | | ✓ |
| Dual Polarity Reset Outputs | ✓ | ✓ | | | | |
| Package | 8-pin DIP and SOIC | 8-pin DIP and SOIC | 3-pin SOT-23 and SC70 | 3-pin SOT-23 and SC70 | 4-pin SOT-143 | 4-pin SOT-143 |

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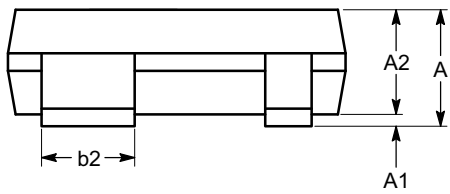
PACKAGE DIMENSIONS

SOT-143, 4 Lead
CASE 527AF-01
ISSUE A

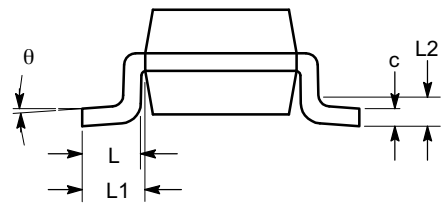


TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|----------|----------|------|------|
| A | 0.80 | | 1.22 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.75 | 0.90 | 1.07 |
| b | 0.30 | | 0.50 |
| b2 | 0.76 | | 0.89 |
| c | 0.08 | | 0.20 |
| D | 2.80 | 2.90 | 3.04 |
| E | 2.10 | | 2.64 |
| E1 | 1.20 | 1.30 | 1.40 |
| e | 1.92 BSC | | |
| e1 | 0.20 BSC | | |
| L | 0.40 | 0.50 | 0.60 |
| L1 | 0.54 REF | | |
| L2 | | 0.25 | |
| θ | 0° | | 8° |



SIDE VIEW



END VIEW

Notes:


- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC TO-253.

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ORDERING INFORMATION

| Order Number | | Voltage | Top Mark (Note 4) | | Output | Reset | Package | Quantity per Reel (Note 5) |
|----------------|---------------|---------|-------------------|-----------|--------------|-------|-----------|----------------------------|
| NiPdAu | Matte-Tin | | NiPdAu | Matte-Tin | | | | |
| CAT811LTBI-GT3 | CAT811LTBI-T3 | 4.63 V | VEA | VES | Manual Reset | LOW | SOT-143-4 | 3,000 |
| CAT811MTBI-GT3 | CAT811MTBI-T3 | 4.38 V | VEA | VES | | | | |
| CAT811JTBI-GT3 | CAT811JTBI-T3 | 4.00 V | VEA | VES | | | | |
| CAT811TTBI-GT3 | CAT811TTBI-T3 | 3.08 V | VEA | VES | | | | |
| CAT811STBI-GT3 | CAT811STBI-T3 | 2.93 V | VEA | VES | | | | |
| CAT811RTBI-GT3 | CAT811RTBI-T3 | 2.63 V | VEA | VES | | | | |
| CAT811ZTBI-GT3 | CAT811ZTBI-T3 | 2.32 V | VEA | VES | | | | |
| CAT812LTBI-GT3 | CAT812LTBI-T3 | 4.63 V | VTA | VTS | Manual Reset | HIGH | SOT-143-4 | 3,000 |
| CAT812MTBI-GT3 | CAT812MTBI-T3 | 4.38 V | VTA | VTS | | | | |
| CAT812JTBI-GT3 | CAT812JTBI-T3 | 4.00 V | VTA | VTS | | | | |
| CAT812TTBI-GT3 | CAT812TTBI-T3 | 3.08 V | VTA | VTS | | | | |
| CAT812STBI-GT3 | CAT812STBI-T3 | 2.93 V | VTA | VTS | | | | |
| CAT812RTBI-GT3 | CAT812RTBI-T3 | 2.63 V | VTA | VTS | | | | |
| CAT812ZTBI-GT3 | CAT812ZTBI-T3 | 2.32 V | VTA | VTS | | | | |

- Threshold and full part numbers will be provided on box and reel labels as well as all Shipping documents.
- For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
- For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

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