

●Operating conditions (Ta=-25~+75°C)

| Item | Symbol | BD6380EFV | BD6381EFV | Unit |
|-------------------------------|------------------|-------------------|-------------------|------|
| Supply voltage VCC | V _{CC} | 2.5~5.5 | 2.5~5.5 | V |
| Supply voltage VM | V _M | 4.0~13.5 | 6.0~13.5 | V |
| Input voltage for control pin | V _{IN} | 0~V _{CC} | 0~V _{CC} | V |
| Output current (DC) | I _{OUT} | 0.5※4 | 0.8※4 | A/ch |

※4 Do not exceed Pd, ASO

●Electrical characteristics

Applicable to BD6380EFV, BD6381EFV (Unless otherwise specified Ta=25°C, VCC=3.3V, VM=6.0V)

| Item | Symbol | Limit | | | Unit | Conditions |
|--|--------------------|-------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Whole | | | | | | |
| VCC current at standby | I _{CCST} | - | 0 | 10 | μ A | PS=L |
| VCC current | I _{CC} | - | 1.6 | 3.0 | mA | PS=H, VLIMX=0.5V |
| VM current at standby | I _{VMST} | - | 0 | 10 | μ A | PS=L |
| VM current | I _{VM} | - | 0.08 | 0.50 | mA | PS=H, VLIMX=0.5V |
| Control input (PS, IN1A, IN1B, IN2A, IN2B) | | | | | | |
| H level input voltage | V _{INH} | 2.0 | - | 3.3 | V | |
| L level input voltage | V _{INL} | 0 | - | 0.8 | V | |
| H level input current | I _{INH} | 15 | 30 | 60 | μ A | V _{IN} =3V |
| L level input current | I _{INL} | -10 | 0 | - | μ A | V _{IN} =0V |
| Output (OUT1A, OUT1B, OUT2A, OUT2B) | | | | | | |
| Output ON resistance (BD6380EFV) | R _{ON} | - | 1.2 | 1.5 | Ω | I _{OUT} =±0.3A, VM=6V Sum of upper and lower |
| Output ON resistance (BD6381EFV) | R _{ON} | - | 1.0 | 1.25 | Ω | I _{OUT} =±0.6A, VM=7.2V Sum of upper and lower |
| Output leak current | I _{LEAK} | - | - | 10 | μ A | |
| Current control | | | | | | |
| RNFX input current | I _{RNF} | -40 | -20 | - | μ A | RNFX=0V |
| SENSEX input current | I _{SENSE} | -2.0 | -0.1 | - | μ A | SENSEX=0V |
| VLIMX input current | I _{VLIM} | -2.0 | -0.1 | - | μ A | VLIMX=0V |
| VLIMX input voltage range | V _{VLIM} | 0 | - | 0.5 | V | |
| Comparator offset voltage | V _{OFS} | -10 | - | 10 | mV | |
| Noise cancel time | t _n | 0.3 | 0.7 | 1.2 | μ s | R=39kΩ, C=1000pF |
| VREF voltage | V _{VREF} | 0.97 | 1.00 | 1.03 | V | I _{VREF} =0~1mA |

●Terminal function・Block diagram・Application circuit diagram

1) BD6380EFV / BD6381EFV

| Pin No. | Pin name | Function | Pin No. | Pin name | Function |
|---------|----------|--|---------|----------|--|
| 1 | GND | Ground terminal | 13 | RNF2 | Connection terminal of resistor for output current detection |
| 2 | PS | Power save terminal | 14 | OUT2B | H bridge output terminal |
| 3 | VLIM1 | Output current limit setting terminal | 15 | OUT2A | H bridge output terminal |
| 4 | SENSE1 | Input terminal of current limit comp. | 16 | VM2 | Power supply terminal for motor |
| 5 | CR1 | Connection terminal of CR for setting PWM frequency | 17 | NC | Non connection |
| 6 | IN1A | Logic input terminal | 18 | IN2B | Logic input terminal |
| 7 | IN1B | Logic input terminal | 19 | IN2A | Logic input terminal |
| 8 | NC | Non connection | 20 | CR2 | Connection terminal of CR for setting PWM frequency |
| 9 | VM1 | Power supply terminal for motor | 21 | SENSE2 | Input terminal of current limit comp. |
| 10 | OUT1A | H bridge output terminal | 22 | VLIM2 | Output current limit setting terminal |
| 11 | OUT1B | H bridge output terminal | 23 | VREF | Reference voltage output terminal |
| 12 | RNF1 | Connection terminal of resistor for output current detection | 24 | VCC | Power supply terminal |

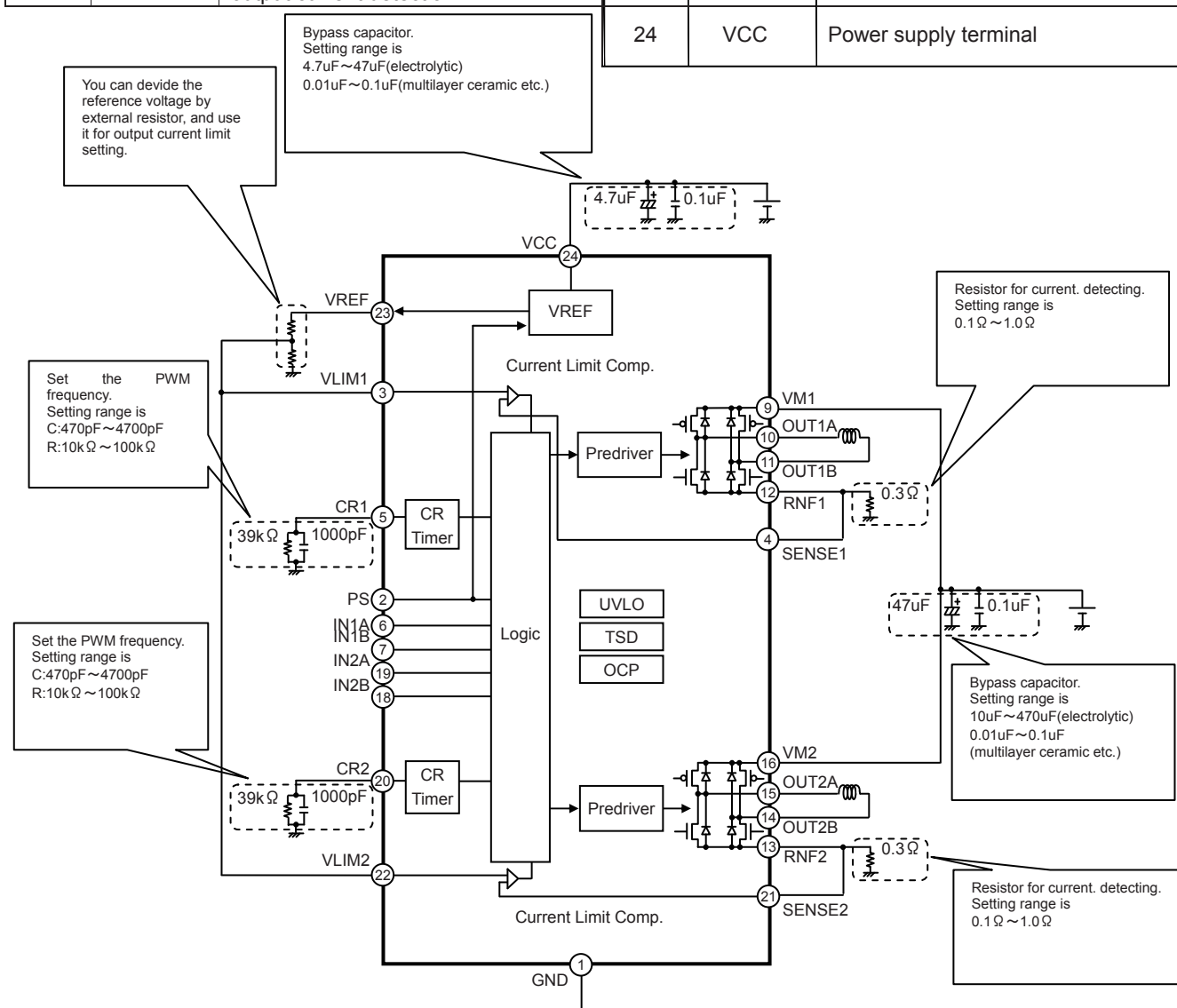


Fig.1 Block diagram & Application circuit diagram of BD6380EFV / BD6381EFV

●Points to notice for terminal description

OPS/Power save terminal

PS can make circuit standby state and make motor output OPEN. Please be careful because there is a delay of 40 μ s(max.) before it is returned from standby state to normal state and the motor output becomes ACTIVE at PS=L→H.

If you don't use power save mode, you may short PS terminal to VCC.

| PS | State |
|----|-----------------------|
| L | Standby state (RESET) |
| H | ACTIVE |

OIN1A,IN1B,IN2A,IN2B/Logic input terminal

These pins decide output state.

| | Input | | Output | | |
|----|--------------|--------------|----------------|----------------|-----------------------|
| PS | IN1A IN2A | IN1B IN2B | OUT1A OUT2A | OUT1B OUT2B | |
| L | X | X | OPEN | OPEN | Standby state (RESET) |
| H | L | L | OPEN | OPEN | Standby |
| H | H | L | H | L | Forward |
| H | L | H | L | H | Reverse |
| H | H | H | L | L | Brake |

X: H or L

●Protection Circuits

○Thermal Shutdown (TSD)

This IC has a built-in thermal shutdown circuit for thermal protection. When the IC's chip temperature rises above 175°C (typ.), the motor output becomes OPEN. Also, when the temperature returns to under 150°C (typ.), it automatically returns to normal operation. However, even when TSD is in operation, if heat is continued to be added externally, heat overdrive can lead to destruction.

○Over current Protection (OCP)

This IC has a built in over current protection circuit as a provision against destruction when the motor outputs are shorted each other or VCC-output or motor output-GND is shorted. This circuit latches the motor output to OPEN condition when the regulated threshold current flows for 4 μ s (typ.). It returns with VCC power reactivation or a reset of the PS terminal. The over current protection circuit's only aim is to prevent the destruction of the IC from irregular situations such as motor output shorts, and is not meant to be used as protection or security for the set. Therefore, sets should not be designed to take into account this circuit's functions. After OCP operating, if irregular situations continues and the return by power reactivation or a reset of the PS terminal is carried out repeatedly, then OCP operates repeatedly and the IC may generate heat or otherwise deteriorate. When the L value of the wiring is great due to the wiring being long, after the over current has flowed and the output terminal voltage jumps up and the absolute maximum values may be exceeded and as a result, there is a possibility of destruction. Also, when current which is over the output current rating and under the OCP detection current flows, the IC can heat up to over Tjmax=150°C and can deteriorate, so current which exceeds the output rating should not be applied.

○Under voltage lock out (UVLO)

This IC has a built-in under voltage lock out function to prevent false operation such as IC output during power supply under voltage. When the applied voltage to the VCC terminal goes under 1.95V (typ.), the motor output is set to OPEN. This switching voltage has a 0.25V (typ.) hysteresis to prevent false operation by noise etc. Please be aware that this circuit does not operate during power save mode.

○False operation prevention function in no power supply (Ghost Supply Prevention)

If a logic control signal is input when there is no power supplied to this IC, there is a function which prevents the false operation by voltage supplied via the electrostatic destruction prevention diode from the logic control input terminal to the VCC, to this IC or to another IC's power supply. Therefore, there is no chance of malfunction of the circuit even when voltage is supplied to the logic control input terminal while there is no power supply.

●Power dissipation

OHTSSOP-B24 Package

HTSSOP-B24 has exposed metal on the back, and it is possible to dissipate heat from a through hole in the back. Also, the back of board as well as the surfaces has large areas of copper foil heat dissipation patterns, greatly increasing power dissipation. The back metal is shorted with the back side of the IC chip, being a GND potential, therefore there is a possibility for malfunction if it is shorted with any potential other than GND, which should be avoided. Also, it is recommended that the back metal is soldered onto the GND to short. Please note that it has been assumed that this product will be used in the condition of this back metal performed heat dissipation treatment for increasing heat dissipation efficiency.

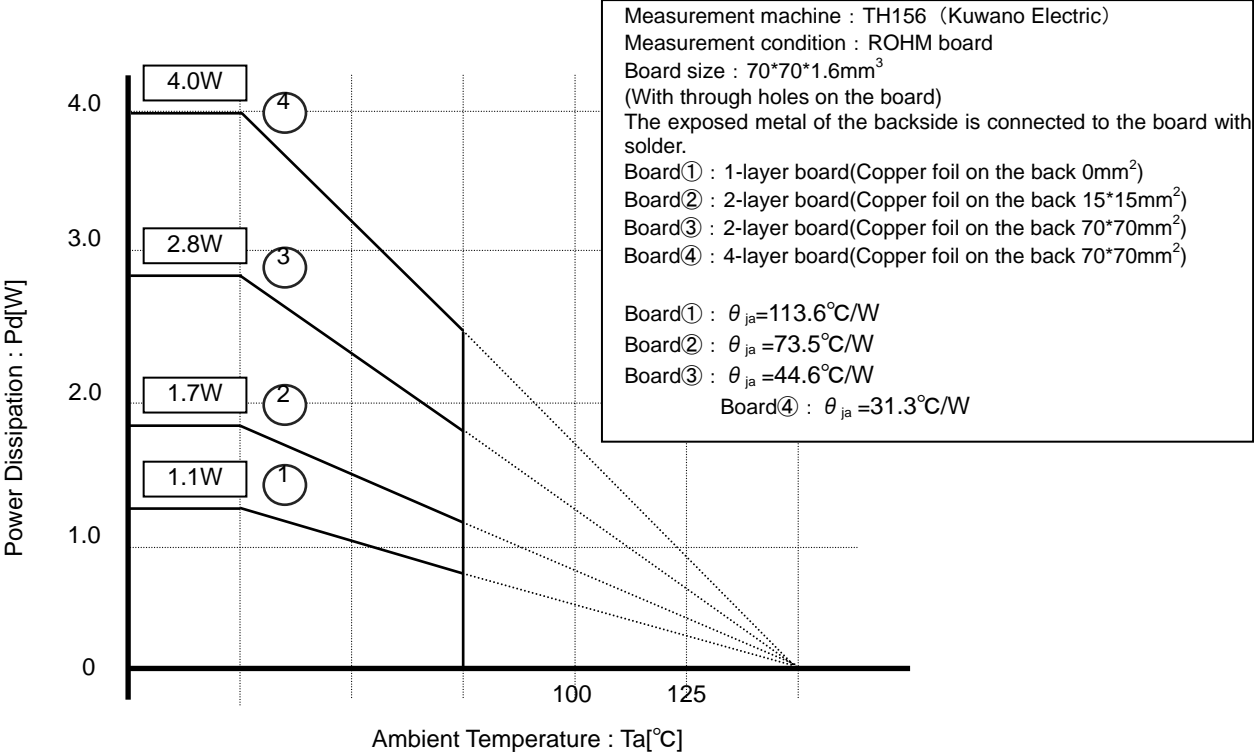


Fig.2 HTSSOP-B24 Derating curve

● Usage Notes

(1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3) Power supply Lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

(4) GND Potential

The potential of GND pin must be minimum potential in all operating conditions.

(5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (P_d) in actual operating conditions. Users should be aware that BD6380EFV and BD6381EFV have been designed to expose their frames at the back of the package, and should be used with suitable heat dissipation treatment in this area to improve dissipation. As large a dissipation pattern should be taken as possible, not only on the front of the baseboard but also on the back surface.

(6) Inter-pin shorts and mounting errors

When attaching to a printed circuit board, pay close attention to the direction of the IC and displacement. Improper attachment may lead to destruction of the IC. There is also possibility of destruction from short circuits which can be caused by foreign matter entering between outputs or an output and the power supply or GND.

(7) Operation in a strong electric field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(8) ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

(9) Thermal shutdown circuit

The IC has a built-in thermal shutdown circuit (TSD circuit). If the chip temperature becomes $T_{jmax}=150^{\circ}\text{C}$, and higher, coil output to the motor will be open. The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect or indemnify peripheral equipment. Do not use the TSD function to protect peripheral equipment.

| TSD ON Temperature [$^{\circ}\text{C}$] (typ.) | Hysteresis Temperature [$^{\circ}\text{C}$] (typ.) |
|--|--|
| 175 | 25 |

(10) Inspection of the application board

During inspection of the application board, if a capacitor is connected to a pin with low impedance there is a possibility that it could cause stress to the IC, therefore an electrical discharge should be performed after each process. Also, as a measure against electrostatic discharge, it should be earthed during the assembly process and special care should be taken during transport or storage. Furthermore, when connecting to the jig during the inspection process, the power supply should first be turned off and then removed before the inspection.

(11) Input terminal of IC

This IC is a monolithic IC, and between each element there is a P+ isolation for element partition and a P substrate. This P layer and each element's N layer make up the P-N junction, and various parasitic elements are made up. For example, when the resistance and transistor are connected to the terminal as shown in figure 3,

○When $GND > (\text{Terminal A})$ at the resistance and $GND > (\text{Terminal B})$ at the transistor (NPN), the P-N junction operates as a parasitic diode.

○Also, when $GND > (\text{Terminal B})$ at the transistor (NPN)

The parasitic NPN transistor operates with the N layers of other elements close to the aforementioned parasitic diode.

Because of the IC's structure, the creation of parasitic elements is inevitable from the electrical potential relationship. The operation of parasitic elements causes interference in circuit operation, and can lead to malfunction and destruction. Therefore, be careful not to use it in a way which causes the parasitic elements to operate, such as by applying voltage that is lower than the GND (P substrate) to the input terminal.

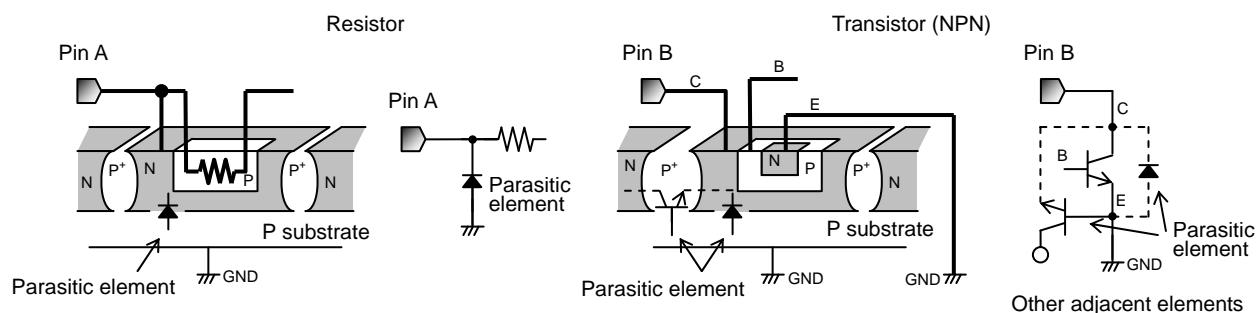


Fig.3 Pattern Diagram of Parasitic Element

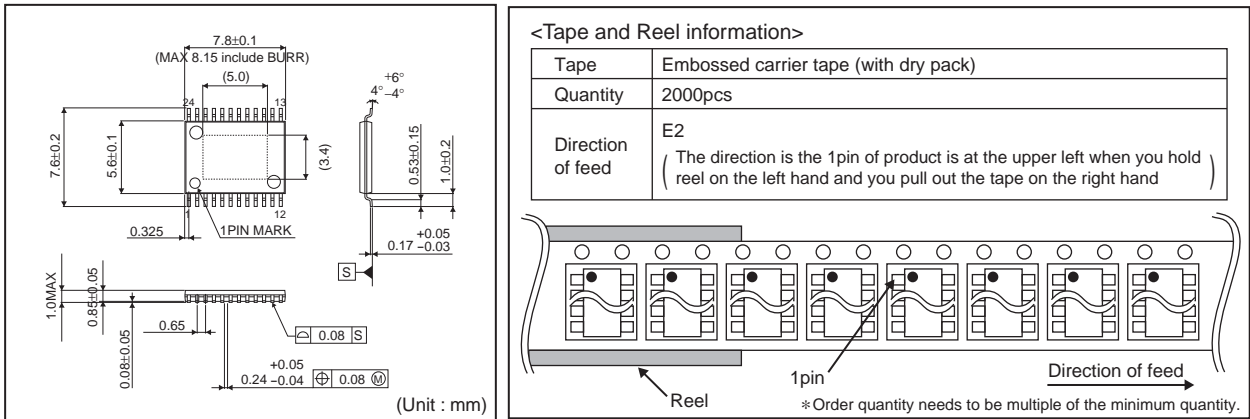
(12) Ground Wiring Patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern potential of any external components, either.

●Ordering part number

| | | | | | | | | | | | |
|-------------|--|--|--|--|--|-------------------------|--|--|---|----------------------------------|--|
| B D 6 3 8 0 | | | | | | E F V | | | - | E 2 | |
| 形名 | | | | | | パッケージ EFV=HTSSOP-B24 | | | | 包装、フォーミング仕様 E2: リール状エンボステーピング | |

HTSSOP-B24



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 - Use of the Products in places subject to dew condensation
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BD6380EFV - Web Page

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| | |
|-----------------------------|------------|
| Part Number | BD6380EFV |
| Package | HTSSOP-B24 |
| Unit Quantity | 2000 |
| Minimum Package Quantity | 2000 |
| Packing Type | Taping |
| Constitution Materials List | inquiry |
| RoHS | Yes |