1. Basic Theory

1.1 Junction Temperature

The junction temperature can be calculated using the following formula.

1. $T_J = T_A + P_{TOT} R_{thja}$

Where:

T_J [°C] = Junction temperature (see note 1)

T_A [°C] = Maximum ambient temperature

P_{TOT} [W] = The total dissipated device power

R_{thja} [K/W] = Thermal resistance from junction to ambient (see note 2)

Notes:
1. To simplify the calculation it is assumed that the temperature is equally distributed on the chip. A more accurate model of the chip's temperature distribution including hot spots or temporary effects is beyond the scope of this note.
2. Although, thermal resistance is specified in the datasheet as R_{thja}, it strongly depends on board design (layout, applied heat sinks, etc.) and might differ from the given value.

1.2 Total Dissipated Power (P_TOT)

With this simplified equation (see note 1) P_{TOT} can be calculated as the sum of the average power dissipated in the power section, P_{PBAT}, and the average power dissipated in the low-power section, P_{VBAT}.

2. $P_{TOT} = P_{VBAT} (I_{VBAT}, I_{Load}, V_{VBAT}, V_{VCC}) + P_{PBAT} (\eta_{CP}, I_{HS}, I_{LS}, V_{PBAT})$

1.2.1 Dissipated Power in Low-power Section (P_VBAT)

P_{VBAT} consists of the power dissipated in the VCC regulator's passive device, P_{VCC} and the power consumed by the internal control circuitry, P_{CONTR}. P_{VCC} is a function of the voltage drop across the regulator's passive device and the average load current (I_{Load}) drawn from the VCC pin. P_{CONTR} depends on voltage VBAT and the average operating current of the control circuitry block, I_{VBAT} (see datasheet, parameter 1.1).

3. $P_{VBAT} (I_{VBAT}, I_{Load}, V_{VBAT}, V_{VCC}) = P_{VCC} (I_{Load}, V_{VBAT}, V_{VCC}) + P_{CONTR} (I_{VBAT}, V_{VBAT})$
4. $P_{VCC} (I_{Load}, V_{VBAT}, V_{VCC}) = I_{Load} (V_{VBAT} - V_{VCC})$
   $P_{CONTR} (I_{VBAT}, V_{VBAT}) = I_{VBAT} V_{VBAT}$

1.2.2 Dissipated Power in Power Section (P_PBAT)

P_{PBAT} mainly consists of the average power dissipated by the charge pump and the drivers, P_{CP}, and the used control circuitry, P_{PBAT_DC}. In equation 5, $P_{PBAT\_DC} << P_{CP}$ and can be neglected. This simplifies to the following:

5. $$P_{PBAT} = P_{CP} + P_{PBAT\_DC} \approx P_{CP} = \frac{V_{PBAT}}{\eta_{CP}} (I_{HS} + I_{LS})$$

I_{HS} and I_{LS} = the average currents sourced by the high-side drivers and low-side drivers, respectively

6. $I_{HS} = f_0 n_{HS} Q_{HS}$

   $I_{LS} = f_0 n_{LS} Q_{LS}$

The high and low-side currents are functions of the switching frequency f_0, the average gate charge to be transferred to switch the respective external NMOS transistor Q_{HS},Q_{LS}, and the number of gates that are switched in each switch period (n_{HS},n_{LS}). η_{CP} stands for charge pump efficiency and for Atmel® ATA6843/ATA6844 which includes a two-stage charge pump $\eta_{CP} \approx 0.3$.

While f_0, n_{HS} and n_{LS} are application-specific, Q_{HS} and Q_{LS} are external NMOS transistor parameters. Combining equations 6 and 5 yields to:

7. $$P_{PBAT} = V_{PBAT} \frac{f_0}{\eta_{CP}} (n_{HS} Q_{HS} + n_{LS} Q_{LS})$$

Thus, the total average power dissipation is:

8. $$P_{\sum} = I_{Load}\,(V_{VBAT} - V_{VCC}) + I_{VBAT}V_{VBAT} + V_{PBAT}\,\frac{f_0}{\eta_{CP}}\,(n_{HS}Q_{HS} + n_{LS}Q_{LS})$$

Using equation 8 enables to calculate junction temperature and its shut-down margin.

2. Power Calculation Example

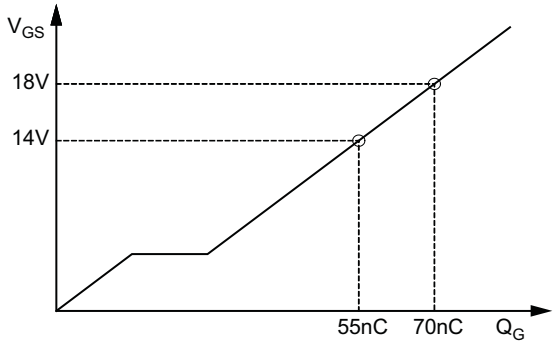
This chapter presents the power calculation for the ATA6843/ATA6844 when operating as a motor control gate driver in an H-bridge configuration. The entire power dissipation for the device is calculated with given operating conditions, which in turn results in the operating junction temperature. Device temperature shut-down can be calculated for a given device power vs. ambient operating temperature.

- V_{VCC} = 5V and I_{Load} = 40mA
- $V_{VBAT} = V_{PBAT}$ = 18V (i.e., assuming that the maximum battery supply voltage is 18V)
- f_0 = 20kHz
- $n_{HS} = n_{LS}$ = 1 (assuming one HS and one LS MOS transistor are switched per PWM period)

Although, all bridge transistors are congeneric, the transferred gate charges for the high and low-side MOS transistors are not equal. This is due to the different gate-source voltages being applied. The gate source voltage of the high-side devices is equal to $V_{CPOUT} - V_{VBAT}$ (datasheet parameter 6.1). The low-side gate-source voltage is set by the VG output (datasheet parameter 7.1). The actual gate charge can then be calculated as:

Q_{HS} ($V_{CPOUT} - V_{PBAT}$ = 18V) = 70nC, and Q_{LS} (V_{VG} = 14V) = 55nC (see Figure 2-1).

Figure 2-1. Gate-source Voltage versus Accumulated Gate Charge



Inserting the given values yields the following results:

P_{VBAT} = 646mW

P_{PBAT} = 150mW

$P_{\sum}$ = 796mW

Assuming R_{thja} = 25K/W, the junction temperature increases to $\Delta T_J = P_{\sum}R_{thja}$ = 20K.

Based on these assumptions ATA6843/ATA6844 would flag temperature prewarning (datasheet parameter 1.11) for $T_A \geq 150°C$, and cause device shut-down for $T_A \geq 180°C$ (datasheet parameter 1.14).

Further, the result shows that the total power dissipation and thus the self-heating is dominated by the load at the VCC output.

As shown in Figure 2-2, this example situation would neither change significantly if a different switching activity is required nor if VCC is be set to 3.3V in conjunction with a smaller load current. In Figure 2-3 the power dissipation is plotted versus an accumulated gate charge that is needed to drive a HS NMOS transistor (gate charge for LS NMOS transistor is scaled accordingly). This figure clearly shows that the power dissipation in the power section begins to dominate only by applying very large external NMOS transistors.

Figure 2-2. Power Dissipation versus VCC Load Current

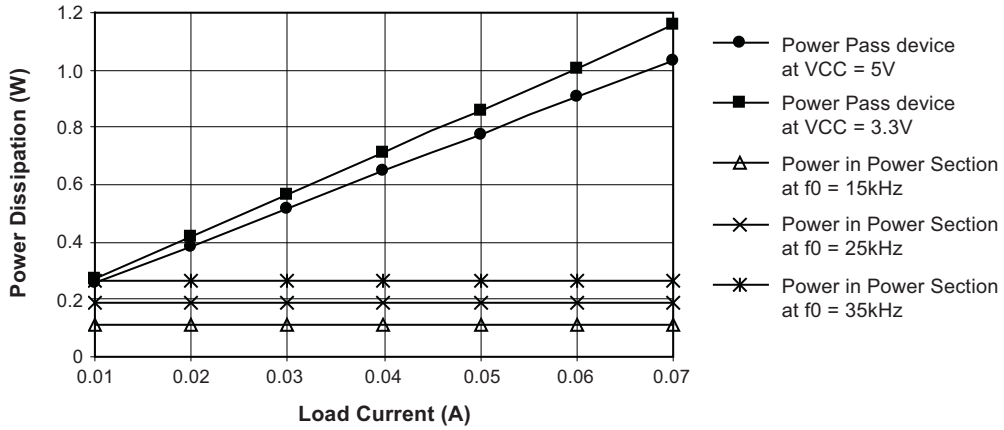
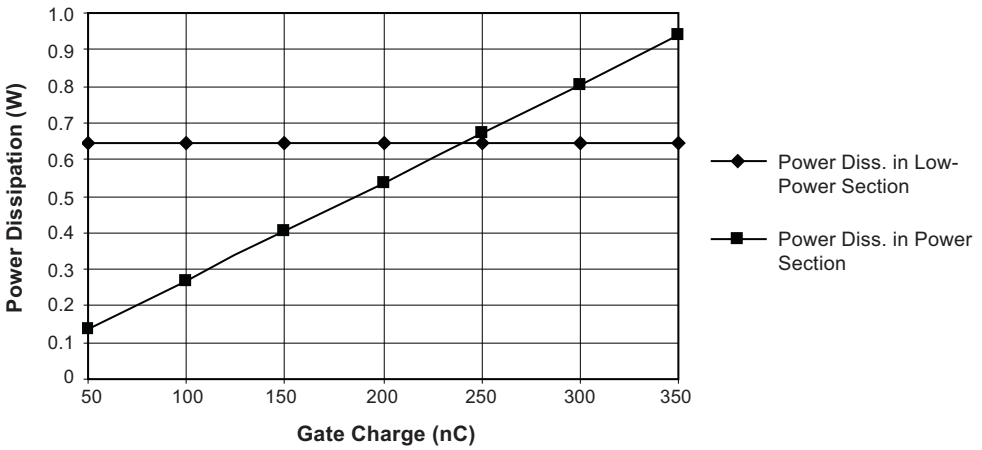


Figure 2-3. Power Dissipation versus Accumulated Gate Charge



3. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9181D-AUTO-04/15	• Put document in the latest template

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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**