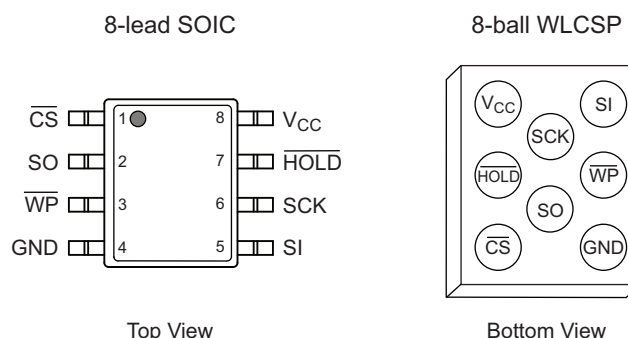


1. Pin Configurations

Figure 1. Pin Configurations

| Pin Name | Function |
|-------------------|-----------------------|
| \overline{CS} | Chip Select |
| SO | Serial Data Output |
| \overline{WP} | Write Protect |
| GND | Ground |
| SI | Serial Data Input |
| SCK | Serial Data Clock |
| \overline{HOLD} | Suspends Serial Input |
| V_{CC} | Device Power Supply |



* Note: Drawings are not to scale.

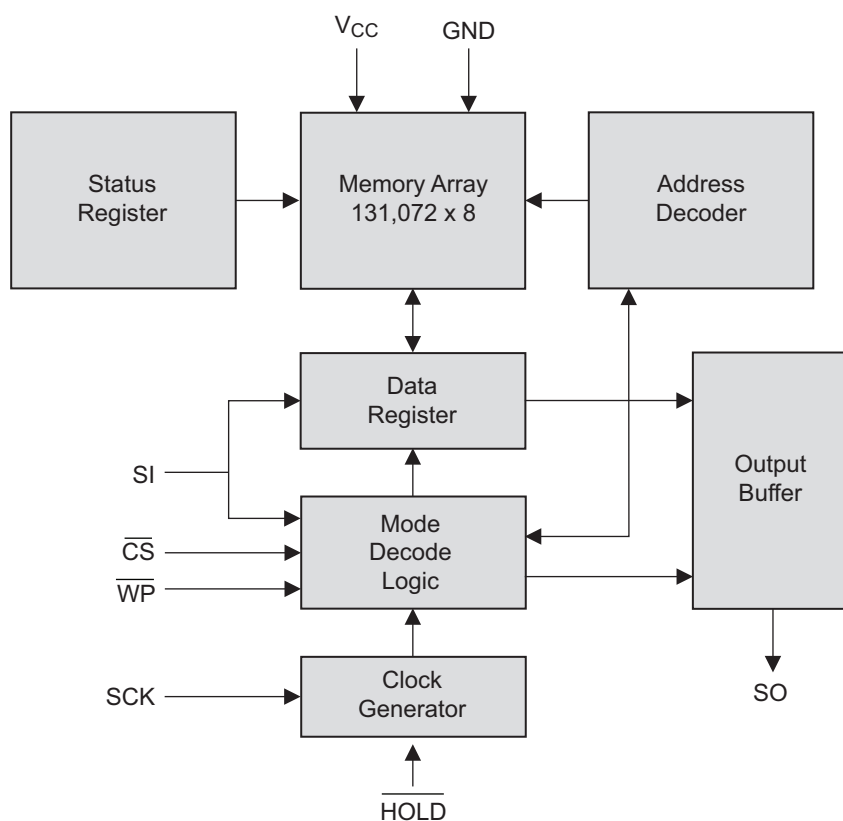
2. Absolute Maximum Ratings*

Operating Temperature -55°C to +125°C
Storage Temperature -65°C to +150°C
Voltage on Any Pin
with Respect to Ground -1.0V to +7.0V
Maximum Operating Voltage 6.25V
DC Output Current 5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram

Figure 3-1. Block Diagram



4. Electrical Specifications

4.1 Pin Capacitance

Table 4-1. Pin Capacitance⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$, $V_{CC} = 5.0\text{V}$ (unless otherwise noted).

| Symbol | Test Conditions | Max | Units | Conditions |
|-----------|--|-----|-------|-----------------------|
| C_{OUT} | Output Capacitance (SO) | 8 | pF | $V_{OUT} = 0\text{V}$ |
| C_{IN} | Input Capacitance (\overline{CS} , SCK, SI, \overline{WP} , \overline{HOLD}) | 6 | pF | $V_{IN} = 0\text{V}$ |

Note: 1. This parameter is characterized and is not 100% tested.

4.2 DC Characteristics

Table 4-2. DC Characteristics

Applicable over recommended operating range from $T_{AI} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 1.7\text{V}$ to 5.5V , (unless otherwise noted).

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|----------------|---------------------|---|----------------------------|-----|---------------------|---------------|
| V_{CC1} | Supply Voltage | | 1.7 | | 5.5 | V |
| V_{CC2} | Supply Voltage | | 2.5 | | 5.5 | V |
| V_{CC3} | Supply Voltage | | 4.5 | | 5.5 | V |
| I_{CC1} | Supply Current | $V_{CC} = 5.0\text{V}$ at 20MHz, SO = Open, Read | | 7.0 | 10.0 | mA |
| I_{CC2} | Supply Current | $V_{CC} = 5.0\text{V}$ at 10MHz, SO = Open, Read, Write | | 5.0 | 7.0 | mA |
| I_{CC3} | Supply Current | $V_{CC} = 5.0\text{V}$ at 1MHz, SO = Open, Read, Write | | 2.2 | 3.5 | mA |
| I_{SB1} | Standby Current | $V_{CC} = 1.7\text{V}$, $\overline{CS} = V_{CC}$ | | 0.2 | 3.0 | μA |
| I_{SB2} | Standby Current | $V_{CC} = 2.5\text{V}$, $\overline{CS} = V_{CC}$ | | 0.4 | 3.0 | μA |
| I_{SB3} | Standby Current | $V_{CC} = 5.0\text{V}$, $\overline{CS} = V_{CC}$ | | 2.0 | 5.0 | μA |
| I_{IL} | Input Leakage | $V_{IN} = 0\text{V}$ to V_{CC} | -3.0 | | 3.0 | μA |
| I_{OL} | Output Leakage | $V_{IN} = 0\text{V}$ to V_{CC} , $T_{AC} = 0^\circ\text{C}$ to 70°C | -3.0 | | 3.0 | μA |
| $V_{IL}^{(1)}$ | Input Low-voltage | | -1.0 | | $V_{CC} \times 0.3$ | V |
| $V_{IH}^{(1)}$ | Input High-voltage | | $V_{CC} \times 0.7$ | | $V_{CC} + 0.5$ | V |
| V_{OL1} | Output Low-voltage | $3.6 \leq V_{CC} \leq 5.5\text{V}$ | $I_{OL} = 3.0\text{mA}$ | | 0.4 | V |
| V_{OH1} | Output High-voltage | | $I_{OH} = -1.6\text{mA}$ | | $V_{CC} - 0.8$ | V |
| V_{OL2} | Output Low-voltage | $1.7\text{V} \leq V_{CC} \leq 3.6\text{V}$ | $I_{OL} = 0.15\text{mA}$ | | 0.2 | V |
| V_{OH2} | Output High-voltage | | $I_{OH} = -100\mu\text{A}$ | | $V_{CC} - 0.2$ | V |

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

4.3 AC Characteristics

Table 4-3. AC Characteristics

Applicable over recommended operating range from $T_{AI} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = \text{As Specified}$, $CL = 1\text{TTL Gate and } 30\text{pF}$ (unless otherwise noted).

| Symbol | Parameter | Voltage | Min | Max | Units |
|-----------|------------------------------|---|-------------------|----------------|-------|
| f_{SCK} | SCK Clock Frequency | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | 0 0 0 | 20 10 5 | MHz |
| t_{RI} | Input Rise Time | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | | 15 40 80 | ns |
| t_{FI} | Input Fall Time | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | | 15 40 80 | ns |
| t_{WH} | SCK High Time | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | 20 40 80 | | ns |
| t_{WL} | SCK Low Time | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | 20 40 80 | | ns |
| t_{CS} | \overline{CS} High Time | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | 100 100 200 | | ns |
| t_{CSS} | \overline{CS} Setup Time | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | 100 100 200 | | ns |
| t_{CSH} | \overline{CS} Hold Time | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | 100 100 200 | | ns |
| t_{SU} | Data In Setup Time | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | 5 10 20 | | ns |
| t_H | Data In Hold Time | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | 5 10 20 | | ns |
| t_{HD} | \overline{Hold} Setup Time | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | 5 10 20 | | ns |
| t_{CD} | \overline{Hold} Hold Time | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | 5 10 20 | | ns |
| t_V | Output Valid | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | 0 0 0 | 20 40 80 | ns |
| t_{HO} | Output Hold Time | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | 0 0 0 | | ns |

Table 4-3. AC Characteristics (Continued)

Applicable over recommended operating range from $T_{AI} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = \text{As Specified}$, $CL = 1\text{TTL Gate and } 30\text{pF}$ (unless otherwise noted).

| Symbol | Parameter | Voltage | Min | Max | Units |
|--------------------------|---|---|-------------|-----------------|--------------|
| t_{LZ} | $\overline{\text{Hold}}$ to Output Low Z | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | 0 0 0 | 25 50 100 | ns |
| t_{HZ} | $\overline{\text{Hold}}$ to Output High Z | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | | 25 50 100 | ns |
| t_{DIS} | Output Disable Time | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | | 25 50 100 | ns |
| t_{WC} | Write Cycle Time | 4.5V – 5.5V 2.5V – 5.5V 1.7V – 5.5V | | 5 5 5 | ms |
| Endurance ⁽¹⁾ | 25°C, Page Mode, 5.0V | | 1,000,000 | | Write Cycles |

Notes: 1. This parameter is characterized and is not 100% tested. Contact Atmel for further information.

5. Serial Interface Description

Master: The device that generates the serial clock.

Slave: Because the Serial Clock pin (SCK) is always an input, the AT25M01 always operates as a slave.

Transmitter/Receiver: The AT25M01 has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

Serial Opcode: After the device is selected with $\overline{\text{CS}}$ going low, the first byte will be received. This byte contains the opcode that defines the operations to be performed.

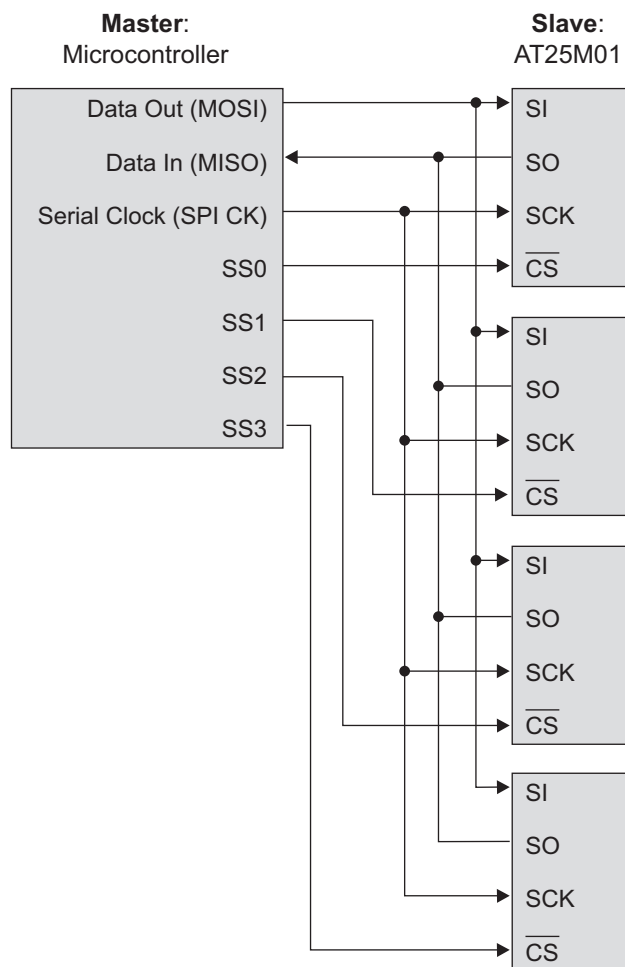
Invalid Opcode: If an invalid opcode is received, no data will be shifted into the AT25M01, and the Serial Output pin (SO) will remain in a high-impedance state until the falling edge of $\overline{\text{CS}}$ is detected again. This will reinitialize the serial communication.

Chip Select: The AT25M01 is selected when the $\overline{\text{CS}}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the Serial Output pin (SO) will remain in a high impedance state.

Hold: The $\overline{\text{HOLD}}$ pin is used in conjunction with the $\overline{\text{CS}}$ pin to select the AT25M01. When the device is selected and a serial sequence is underway, Hold can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{\text{HOLD}}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{\text{HOLD}}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{\text{HOLD}}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

Write Protect: The Write Protect pin ($\overline{\text{WP}}$) will allow normal read/write operations when held high. When the $\overline{\text{WP}}$ pin is brought low, and WPEN bit is one, all write operations to the status register are inhibited. $\overline{\text{WP}}$ going low while $\overline{\text{CS}}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{\text{WP}}$ going low will have no effect on any write operation to the status register. The $\overline{\text{WP}}$ pin function is blocked when the WPEN bit in the status register is zero. This will allow the user to install the AT25M01 in a system with the $\overline{\text{WP}}$ pin tied to ground and still be able to write to the status register. All $\overline{\text{WP}}$ pin functions are enabled when the WPEN bit is set to one.

Figure 5-1. SPI Serial Interface



6. Functional Description

The AT25M01 is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of the 6800 type series of microcontrollers. The AT25M01 utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in [Table 6-1](#). All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low \overline{CS} transition.

Table 6-1. Instruction Set for Atmel AT25M01

| Instruction Name | Instruction Format | Operation |
|------------------|--------------------|-----------------------------|
| WREN | 0000 x110 | Set Write Enable Latch |
| WRDI | 0000 x100 | Reset Write Enable Latch |
| RDSR | 0000 x101 | Read Status Register |
| WRSR | 0000 x001 | Write Status Register |
| READ | 0000 x011 | Read Data from Memory Array |
| WRITE | 0000 x010 | Write Data to Memory Array |

Write Enable (WREN): The device will power-up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

Write Disable (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the \overline{WP} pin.

Read Status Register (RDSR): The Read Status Register instruction provides access to the status register. The Ready/Busy and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 6-2. Status Register Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|------------------|
| WPEN | X | X | X | BP1 | BP0 | WEN | \overline{RDY} |

Table 6-3. Read Status Register Bit Detection

| Bit | Definition |
|---|--|
| Bit 0 (\overline{RDY}) | Bit 0 = 0 (\overline{RDY}) indicates the device is ready. Bit 0 = 1 indicates the write cycle is in progress. |
| Bit 1 (WEN) | Bit 1 = 0 indicates the device <i>is not</i> write enabled. Bit 1 = 1 indicates the device is write enabled. |
| Bit 2 (BP0) | See Table 6-4 on page 9 . |
| Bit 3 (BP1) | See Table 6-4 on page 9 . |
| Bits 4 – 6 are zeros when device is not in an internal write cycle. | |
| Bit 7 (WPEN) | See Table 6-5 on page 9 . |
| Bits 0 – 7 are ones during an internal write cycle. | |

Write Status Register (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25M01 is divided into four array segments. Top quarter ($\frac{1}{4}$), top half ($\frac{1}{2}$), or all of the memory segments can be protected. Any of the data within any selected segment will therefore be read-only. The block write protection levels and corresponding status register control bits are shown in Table 6-4.

The three bits, BP0, BP1, and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g. WREN, t_{WC} , RDSR).

Table 6-4. Block Write Protect Bits

| Level | Status Register Bits | | Array Addresses Protected |
|--------------------|----------------------|-----|---------------------------|
| | BP1 | BP0 | AT25M01 |
| 0 | 0 | 0 | None |
| 1($\frac{1}{4}$) | 0 | 1 | 18000h – 1FFFFh |
| 2($\frac{1}{2}$) | 1 | 0 | 10000h – 1FFFFh |
| 3(All) | 1 | 1 | 00000h – 1FFFFh |

The WRSR instruction also allows the user to enable or disable the Write Protect (\overline{WP}) pin through the use of the Write Protect Enable (WPEN) bit. Hardware Write Protection is enabled when the \overline{WP} pin is low and the WPEN bit is one. Hardware Write Protection is disabled when *either* the \overline{WP} pin is high or the WPEN bit is zero. When the device is hardware write protected, writes to the Status Register, including the Block Protect bits and the WPEN bit, and the block protected sections in the memory array are disabled. Writes are only allowed to sections of the memory which are not block protected (see Table 6-5).

Note: When the WPEN bit is hardware write protected, it cannot be changed back to zero, as long as the \overline{WP} pin is held low.

Table 6-5. WPEN Operation

| WPEN | WP | WEN | Protected Blocks | Unprotected Blocks | Status Register |
|------|------|-----|------------------|--------------------|-----------------|
| 0 | x | 0 | Protected | Protected | Protected |
| 0 | x | 1 | Protected | Writable | Writable |
| 1 | Low | 0 | Protected | Protected | Protected |
| 1 | Low | 1 | Protected | Writable | Protected |
| X | High | 0 | Protected | Protected | Protected |
| X | High | 1 | Protected | Writable | Writable |

Read Sequence (READ): Reading the AT25M01 via the SO pin requires the following sequence. After the \overline{CS} line is pulled low to select a device, the Read opcode is transmitted via the SI line followed by the a 3-byte address to be read (see Table 6-6 on page 10). Upon completion, any data on the SI line will be ignored. The data (D7 – D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the \overline{CS} line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous read cycle.

Write Sequence (Write): In order to program the AT25M01, two separate instructions must be executed. First, the device *must be write enabled* via the Write Enable (WREN) Instruction. Then, a Write instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the block write protection level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write Instruction requires the following sequence. After the \overline{CS} line is pulled low to select the device, the Write opcode is transmitted via the SI line followed by the byte address and the data (D7 – D0) to be programmed (see Table 6-6). Programming will start after the \overline{CS} pin is brought high. (The Low-to-High transition of the \overline{CS} pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

The Ready/Busy status of the device can be determined by initiating a Read Status Register (RDSR) Instruction. If Bit 0 = 1, the Write cycle is still in progress. If Bit 0 = 0, the Write cycle has ended. Only the Read Status Register instruction is enabled during the Write programming cycle.

The AT25M01 is capable of a 256-byte Page Write operation. After each byte of data is received, the eight low order address bits are internally incremented by one; the high order bits of the address will remain constant. If more than 256 bytes of data are transmitted, the address counter will roll-over and the previously written data will be overwritten. The AT25M01 is automatically returned to the write disable state at the completion of a Write cycle.

Note: If the device is not Write Enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when \overline{CS} is brought high. A new \overline{CS} falling edge is required to re-initiate the serial communication.

Table 6-6. Address Key

| Address | AT25M01 |
|---------|----------|
| A(n) | A23 – A0 |

Note: The A23 through A17 address bits of the most significant address byte are don't care values as these bits fall outside the addressable 1Mbit range.

7. Timing Diagrams (for SPI Mode 0 (0, 0))

Figure 7-1. Synchronous Data Timing

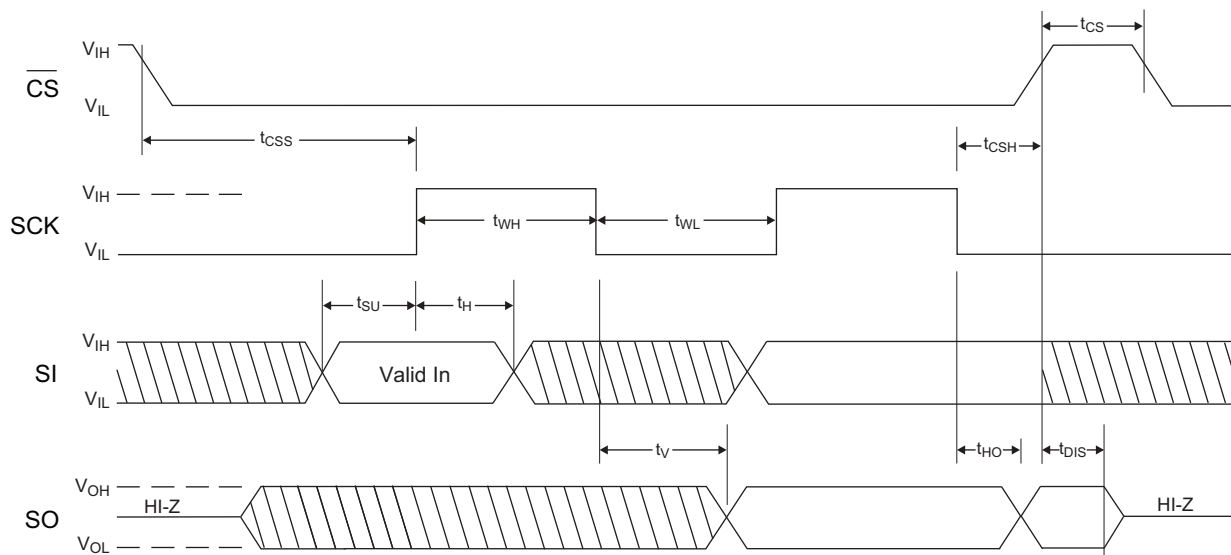


Figure 7-2. WREN Timing

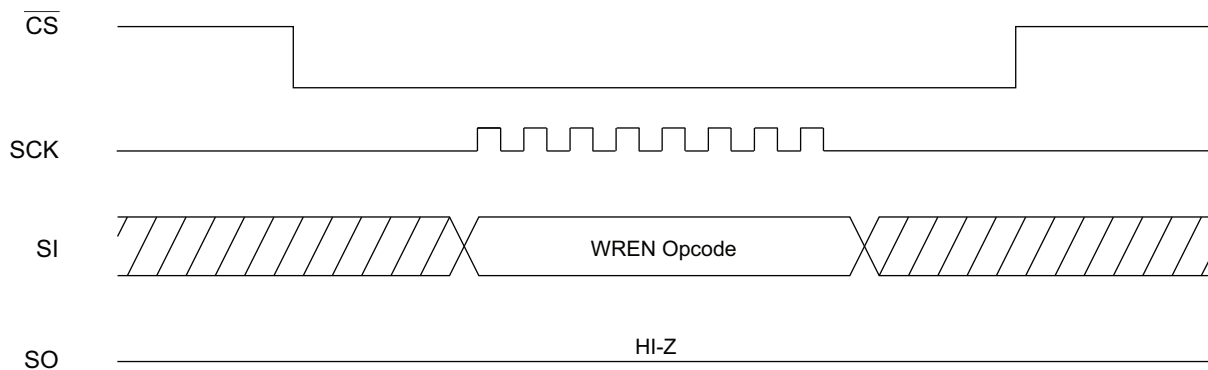


Figure 7-3. WRDI Timing

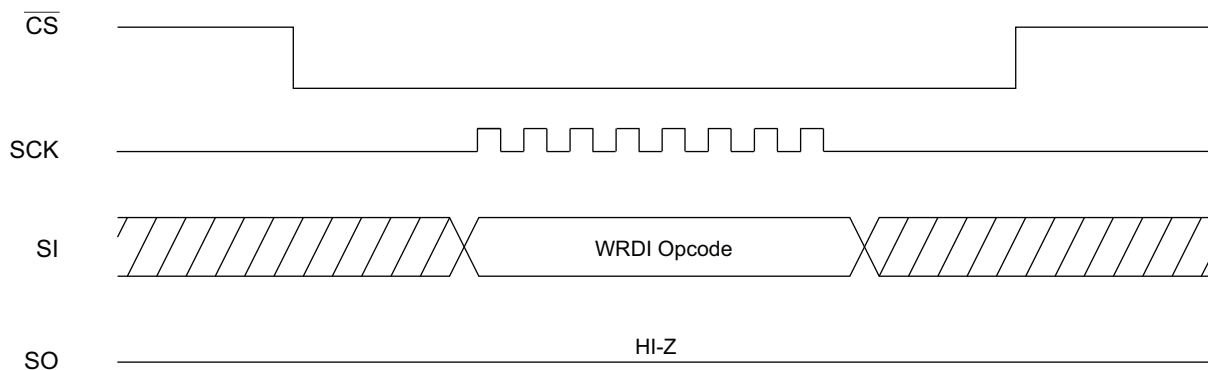


Figure 7-4. RDSR Timing

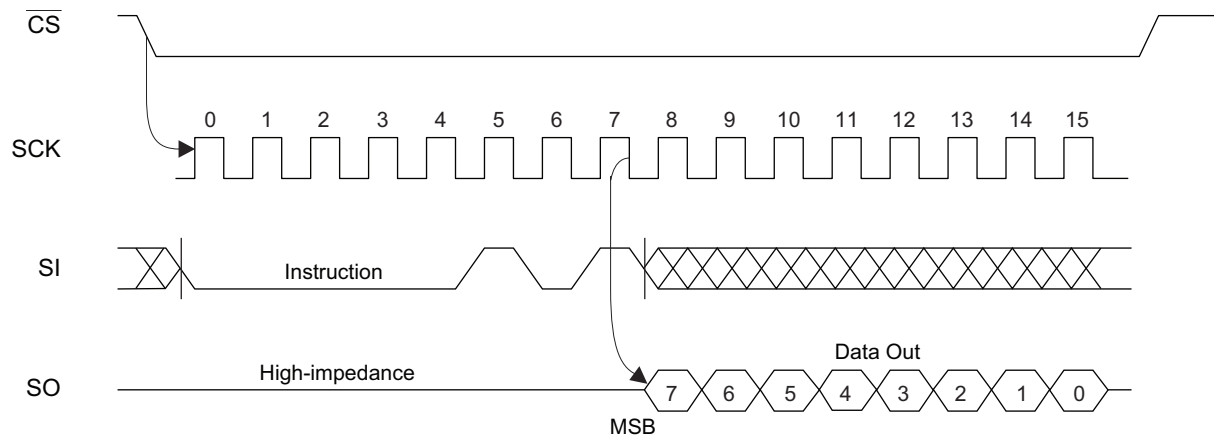


Figure 7-5. WRSR Timing

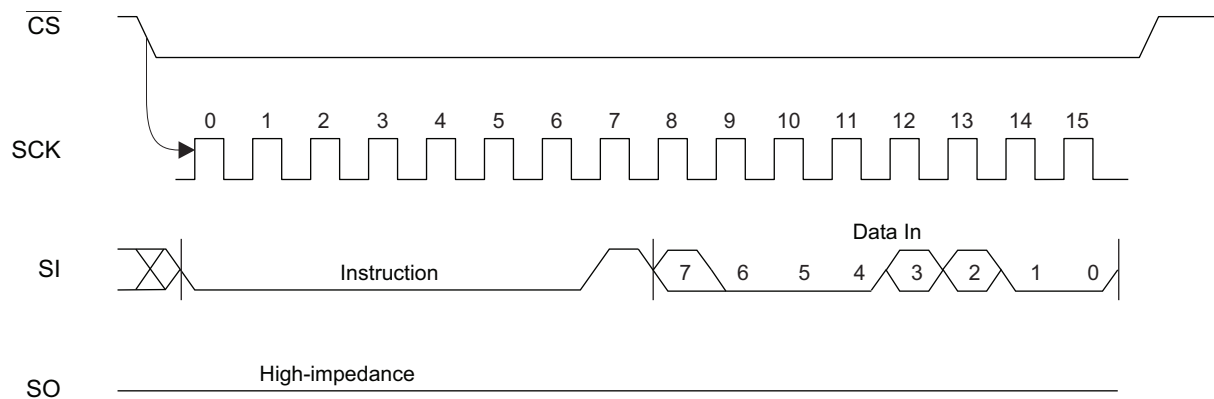


Figure 7-6. READ Timing

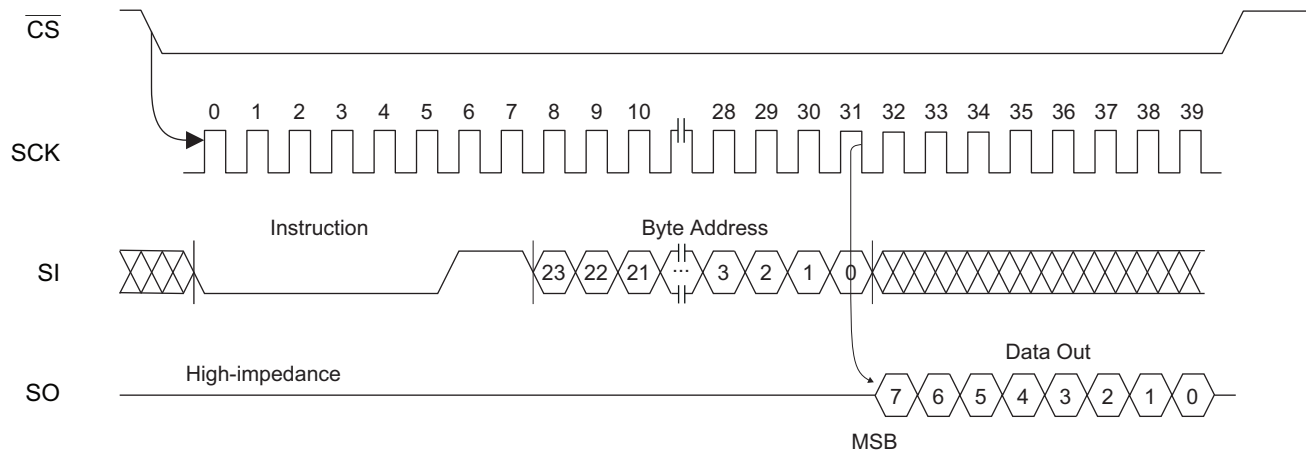


Figure 7-7. Write Timing

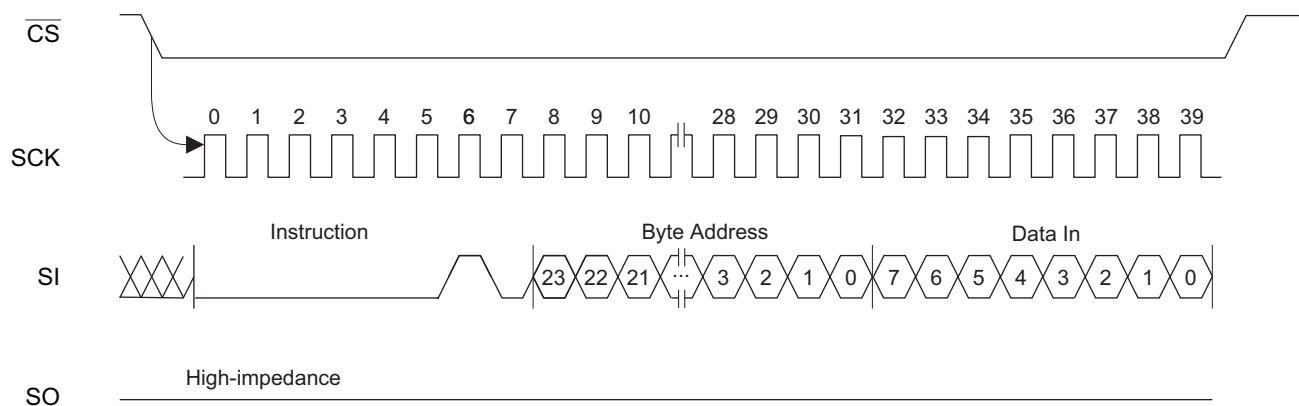
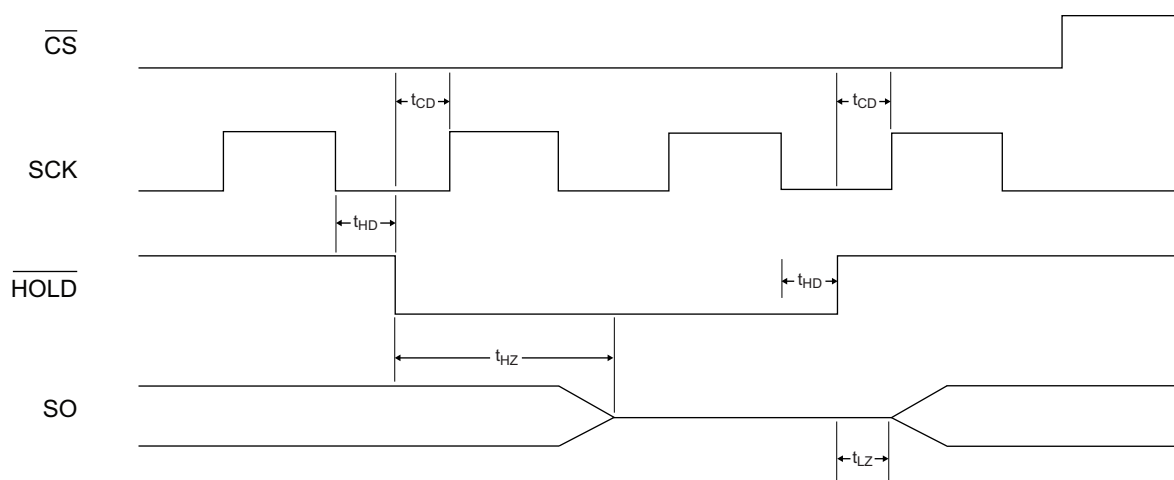
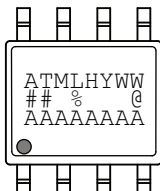
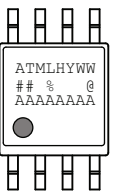
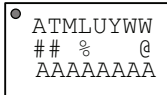


Figure 7-8. Hold Timing



8. Part Marking

AT25M01: Package Marking Information

| 8-lead SOIC | 8-lead EIAJ | 8-ball WLCSP |
|---|---|---|
|  |  |  |

Note 1: ● designates pin 1

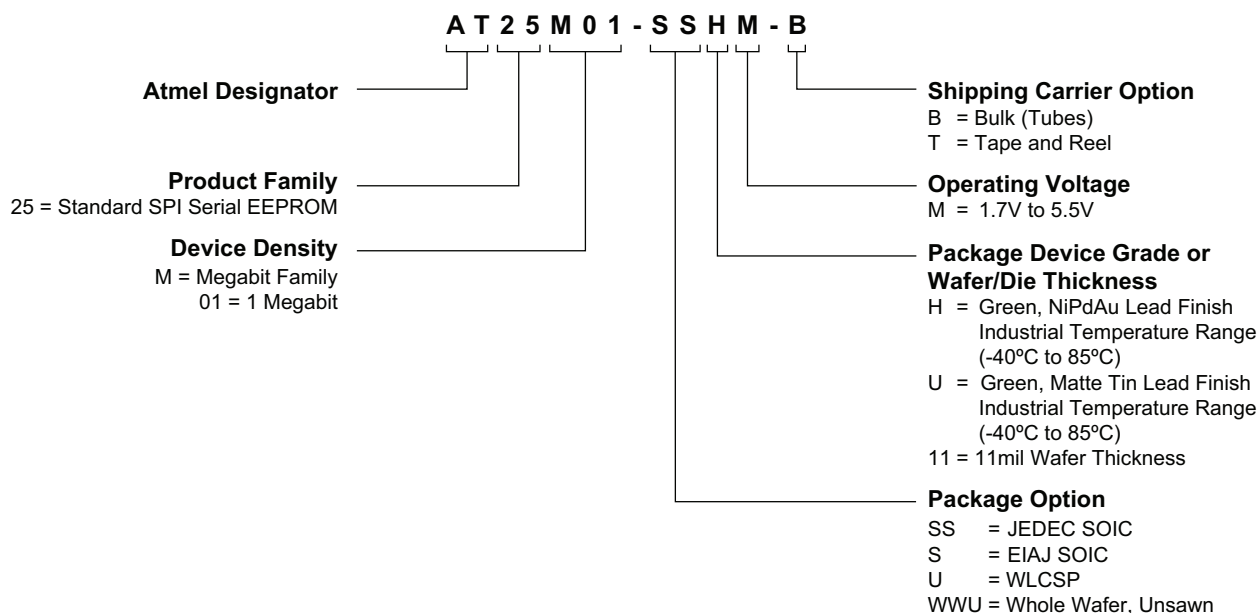
Note 2: Package drawings are not to scale

| Catalog Number Truncation | | |
|---------------------------|----------------------------------|---|
| AT25M01 | | Truncation Code ##: 5G |
| Date Codes | | Voltages |
| Y = Year | | WW = Work Week of Assembly |
| 5: 2015 9: 2019 | | % = Minimum Voltage |
| 6: 2016 0: 2020 | | L: 1.8V min |
| 7: 2017 1: 2021 | | D: 2.5V min |
| 8: 2018 2: 2022 | | ... |
| | | 52: Week 52 |
| Country of Assembly | Lot Number | Grade/Lead Finish Material |
| @ = Country of Assembly | AAA...A = Atmel Wafer Lot Number | U: Industrial/LeadFree Ball H: Industrial/NiPdAu |
| | | Atmel Truncation |
| | | ATML: Atmel |

7/9/15

| | | | |
|---|--|-------------------------------|-------------|
|  Package Mark Contact: DL-CSO-Assy_eng@atmel.com | TITLE 25M01SM, AT25M01 Standard Package Marking Information | DRAWING NO. 25M01SM | REV. |
| | | | B |

9. Ordering Code Detail



10. Ordering Information

Additional package types that are not listed below may be available for order. Please contact Atmel for availability details.

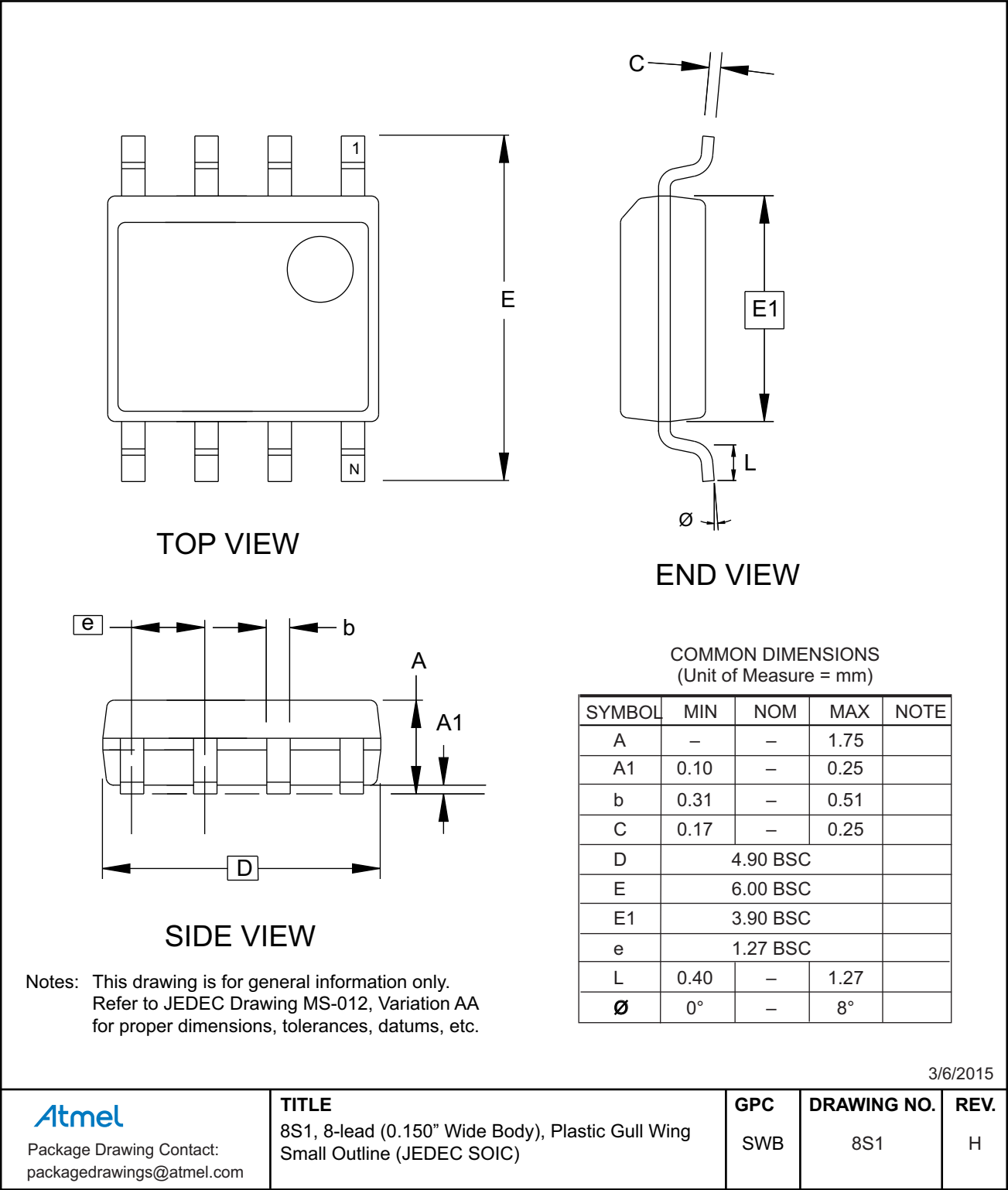
| Atmel Ordering Code | Lead Finish | Package | Delivery Information | | Operation Range |
|-------------------------------|------------------------------------|------------|----------------------|----------------|---|
| | | | Form | Quantity | |
| AT25M01-SSHM-B | NiPdAu (Lead-free/Halogen-free) | 8S1 | Bulk (Tubes) | 100 per Tube | Industrial Temperature (-40°C to 85°C) |
| AT25M01-SSHM-T | | | Tape and Reel | 4,000 per Reel | |
| AT25M01-SHM-B | | 8S2 | Bulk (Tubes) | 95 per Tube | |
| AT25M01-SHM-T | | | Tape and Reel | 2,000 per Reel | |
| AT25M01-UUM-T ⁽¹⁾ | SnAgCu (Lead-free/Halogen-free) | 8U-7 | Tape and Reel | 5,000 per Reel | |
| AT25M01-WWU11M ⁽²⁾ | N/A | Wafer Sale | Note 2 | | |

- Notes:
1. WLCSP Package — **CAUTION**: Exposure to ultraviolet (UV) light can degrade the data stored in the EEPROM cells. Therefore, customers who use a WLCSP product must ensure that exposure to ultraviolet light does **not** occur.
 2. For wafer sales, please contact Atmel Sales.

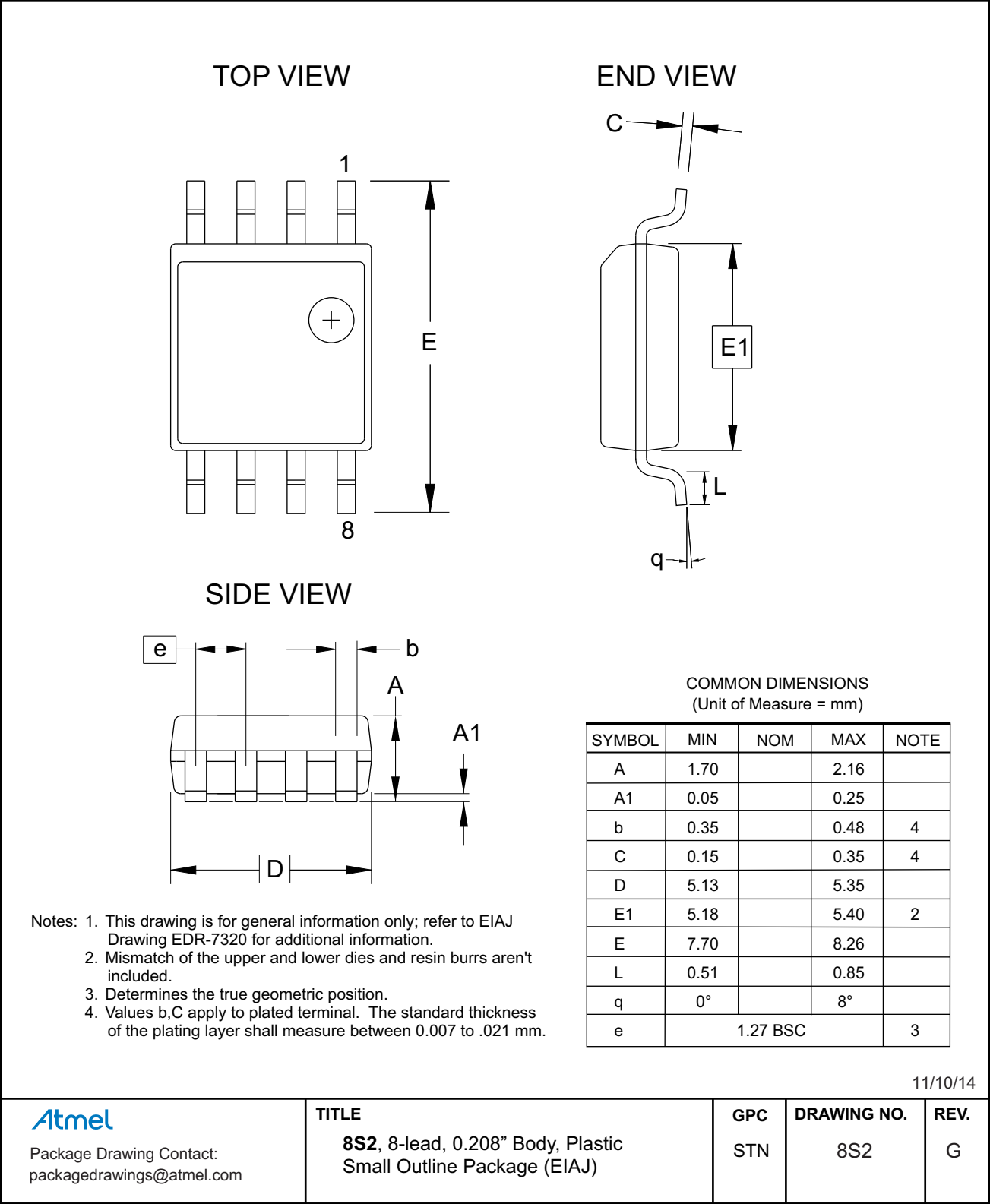
| Package Type | |
|--------------|---|
| 8S1 | 8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| 8S2 | 8-lead, 0.208" wide, Plastic Small Package Outline (EIAJ SOIC) |
| 8U-7 | 8-ball, Wafer Level Chip Scale Package (WLCSP) |

11. Packaging Information

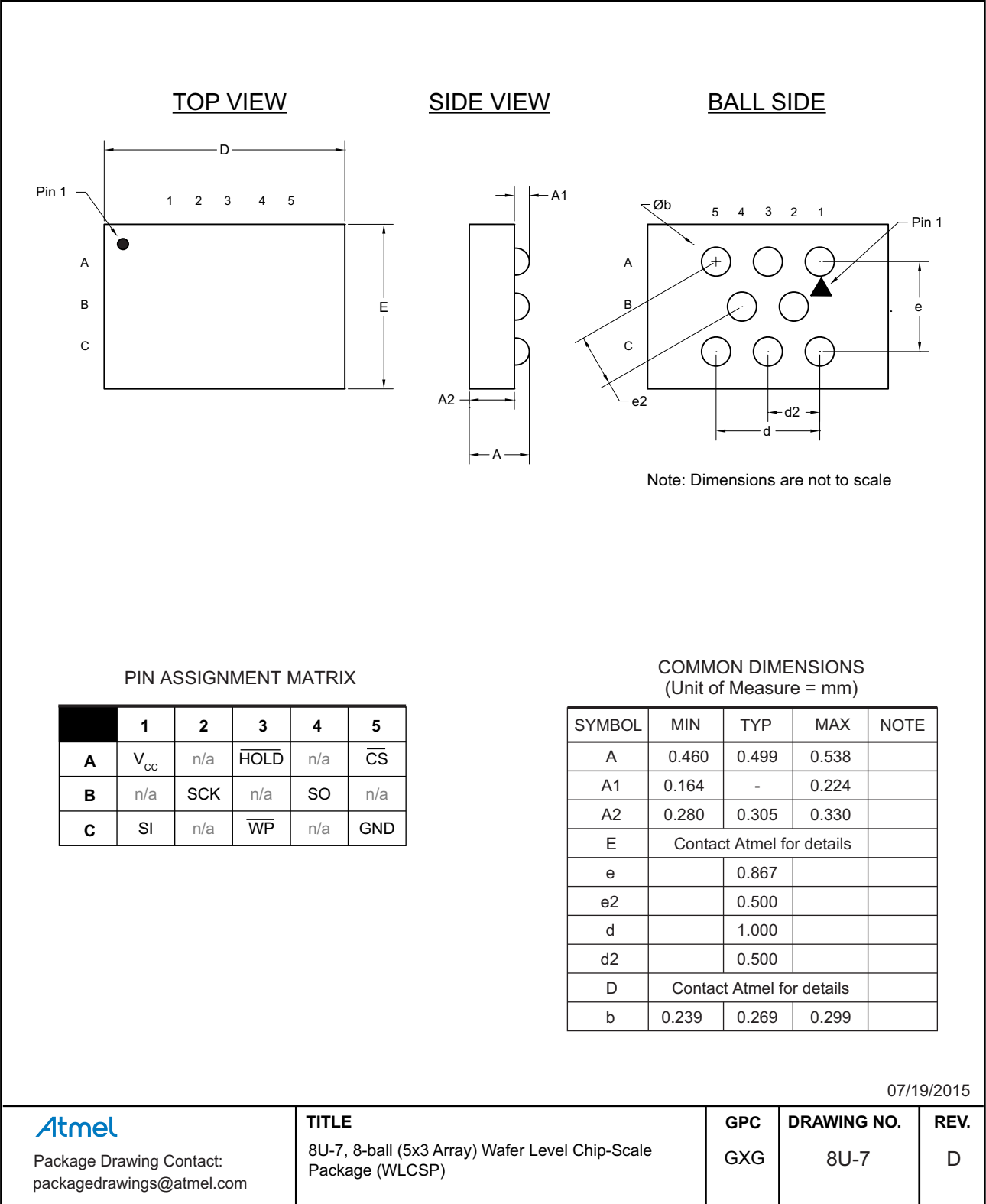
11.1 8S1 — 8-lead JEDEC SOIC



11.2 8S2 — 8-lead EIAJ SOIC



11.3 8U-7 — 8-ball WLCSP



Atmel

Package Drawing Contact:
packagedrawings@atmel.com

TITLE

8U-7, 8-ball (5x3 Array) Wafer Level Chip-Scale
Package (WLCSP)

GPC

GXG

DRAWING NO.

8U-7

REV.

D

07/19/2015

12. Revision History

| Doc. Rev. | Date | Comments |
|-----------|---------|--|
| 8823E | 05/2016 | Correct ordering information WLCSP note. |
| 8823D | 07/2015 | Update the t_{RI} and t_{FI} maximum values, part markings page, and the 8S1 and 8U-7 package drawings. |
| 8823C | 01/2015 | Correct the Write Timing figure. Update the 8S2 and 8U-7 package drawings, the ordering information section, and the disclaimer page. |
| 8823B | 03/2013 | Add part marking. Update datasheet status from advance to complete. Update footers and Atmel fax number. |
| 8823A | 12/2012 | Initial document release. |



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