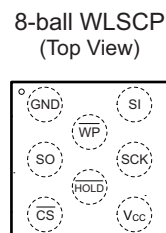
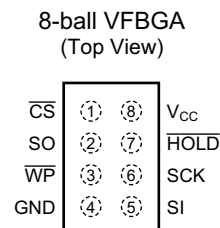
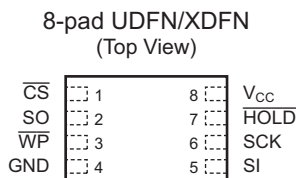
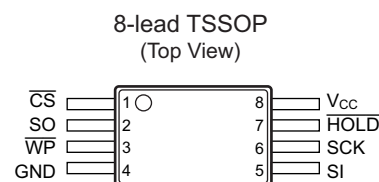
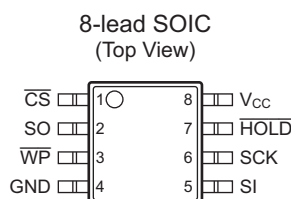


1. Pin Configurations and Pinouts

Table 1. Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
GND	Ground
$\overline{HOLD}$	Suspends Serial Input
SCK	Serial Data Clock
SO	Serial Data Output
SI	Serial Data Input
$\overline{WP}$	Write Protect
V_{CC}	Power Supply



Note: Drawings are not to scale.

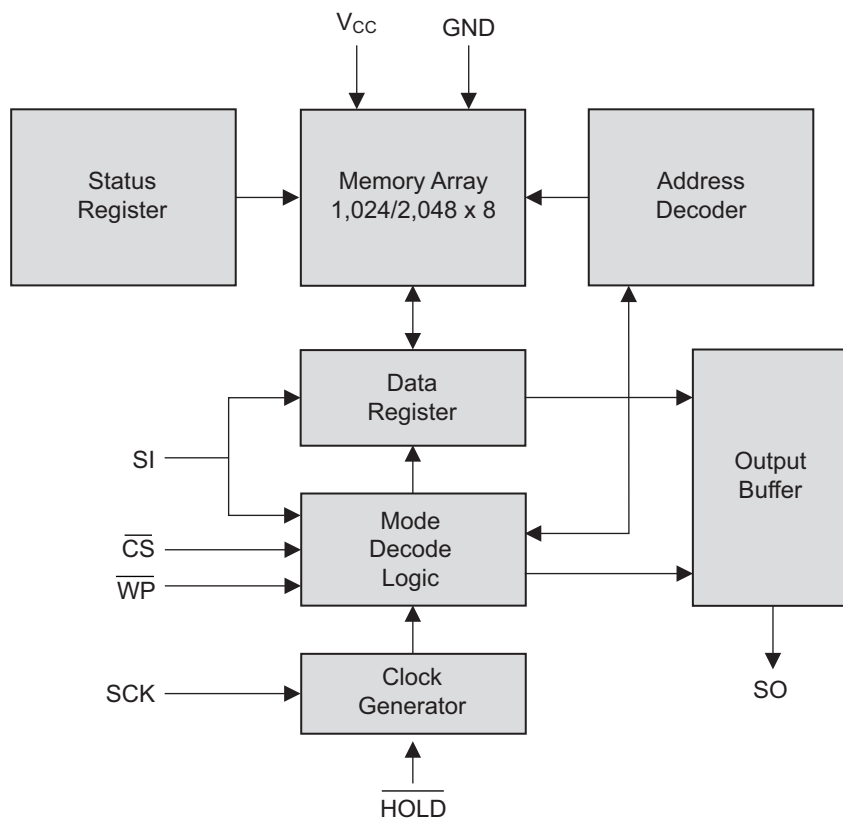
2. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	 -1.0V to +7.0V
Maximum Operating Voltage	 6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram

Figure 3-1. Block Diagram



4. Memory Organization

4.1 Pin Capacitance

Table 4-1. Pin Capacitance⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$, $V_{CC} = +5.0\text{V}$ (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	$V_{OUT} = 0\text{V}$
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

4.2 DC Characteristics

Table 4-2. DC Characteristics

Applicable over recommended operating range from $T_{AI} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 1.7\text{V}$ to 5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		4.5		5.5	V
I_{CC1}	Supply Current	$V_{CC} = 5.0\text{V}$ at 20MHz, SO = Open and Read		7.5	10.0	mA
I_{CC2}	Supply Current	$V_{CC} = 5.0\text{V}$ at 20MHz, SO = Open, Read, and Write		4.0	10.0	mA
I_{CC3}	Supply Current	$V_{CC} = 5.0\text{V}$ at 5MHz, SO = Open, Read, and Write		4.0	6.0	mA
I_{SB1}	Standby Current	$V_{CC} = 1.8\text{V}$, $\overline{CS} = V_{CC}$		< 0.1	6.0 ⁽²⁾	μA
I_{SB2}	Standby Current	$V_{CC} = 2.5\text{V}$, $\overline{CS} = V_{CC}$		0.3	7.0 ⁽²⁾	μA
I_{SB3}	Standby Current	$V_{CC} = 5.0\text{V}$, $\overline{CS} = V_{CC}$		2.0	10.0 ⁽²⁾	μA
I_{IL}	Input Leakage	$V_{IN} = 0\text{V}$ to V_{CC}	-3.0		3.0	μA
I_{OL}	Output Leakage	$V_{IN} = 0\text{V}$ to V_{CC} , $T_{AC} = 0^\circ\text{C}$ to 70°C	-3.0		3.0	μA
$V_{IL}^{(1)}$	Input Low-voltage		-0.6		$V_{CC} \times 0.3$	V
$V_{IH}^{(1)}$	Input High-voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL1}	Output Low-voltage	$3.6\text{V} \leq V_{CC} \leq 5.5\text{V}$	$I_{OL} = 3.0\text{mA}$		0.4	V
V_{OH1}	Output High-voltage		$I_{OH} = -1.6\text{mA}$	$V_{CC} - 0.8$		V
V_{OL2}	Output Low-voltage	$1.8\text{V} \leq V_{CC} \leq 3.6\text{V}$	$I_{OL} = 0.15\text{mA}$		0.2	V
V_{OH2}	Output High-voltage		$I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$		V

Notes: 1. V_{IL} min and V_{IH} max are reference only and are not tested.
2. Worst case measured at 85°C .

4.3 AC Characteristics

Table 4-3. AC Characteristics

Applicable over recommended operating range from $T_{AI} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} =$ as specified, $CL = 1$ TTL gate and 100pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5	0 0 0	20 10 5	MHz
t_{RI}	Input Rise Time	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5		2 2 2	μs
t_{FI}	Input Fall Time	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5		2 2 2	μs
t_{WH}	SCK High Time	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5	20 40 80		ns
t_{WL}	SCK Low Time	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5	20 40 80		ns
t_{CS}	$\overline{CS}$ High Time	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5	25 50 100		ns
t_{CSS}	$\overline{CS}$ Setup Time	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5	25 50 100		ns
t_{CSH}	$\overline{CS}$ Hold Time	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5	25 50 100		ns
t_{SU}	Data In Setup Time	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5	5 10 20		ns
t_H	Data In Hold Time	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5	5 10 20		ns
t_{HD}	$\overline{HOLD}$ Setup Time	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5	5 10 20		
t_{CD}	$\overline{HOLD}$ Hold Time	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5	5 10 20		ns
t_V	Output Valid	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5	0 0 0	20 40 80	ns

Table 4-3. AC Characteristics (Continued)

Applicable over recommended operating range from $T_{AI} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} =$ as specified, $CL = 1$ TTL gate and 100pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
t_{HO}	Output Hold Time	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5	0 0 0		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5	0 0 0	25 50 100	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5		40 80 200	ns
t_{DIS}	Output Disable Time	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5		40 80 200	ns
t_{WC}	Write Cycle Time	4.5 to 5.5 2.5 to 5.5 1.8 to 5.5		5 5 5	ms
Endurance ⁽¹⁾	3.3V, 25°C, Page Mode		1M		Write Cycles

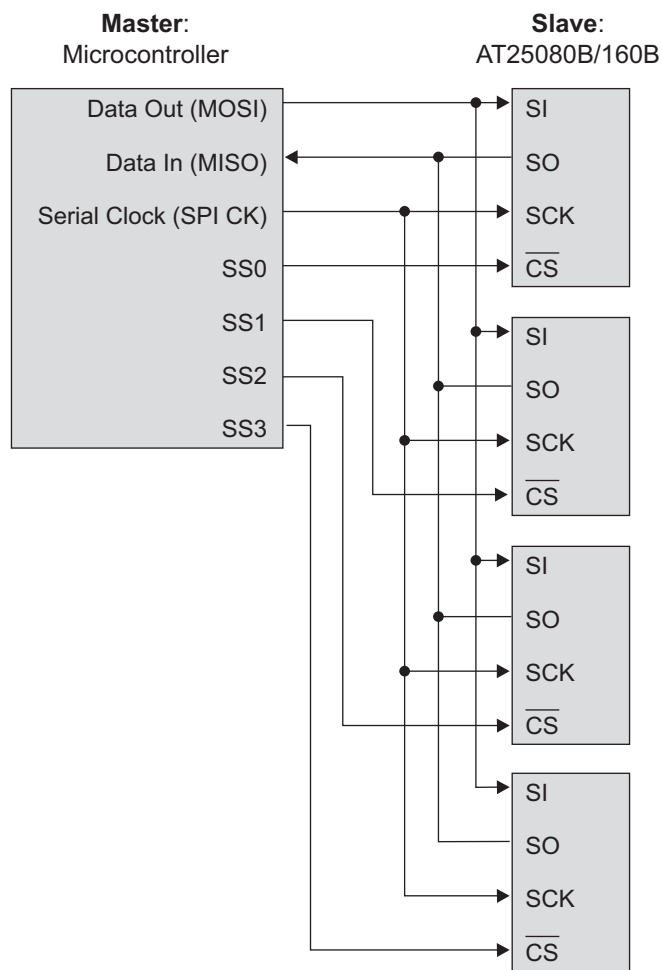
Note: 1. This parameter is characterized and is not 100% tested.

5. Serial Interface Description

Table 5-1. Serial Interface Description

Interface	Description
Master	The device that generates the Serial Clock.
Slave	Because the Serial Clock pin (SCK) is always an input, the AT25080B/160B always operates as a slave.
Transmitter/Receiver	The AT25080B/160B has separate pins designated for data transmission (SO) and reception (SI).
MSB	The Most Significant Bit (MSB) is the first bit transmitted and received.
Serial Opcode	After the device is selected with $\overline{CS}$ going low, the first byte will be received. This byte contains the opcode that defines the operations to be performed.
Invalid Opcode	If an invalid opcode is received, no data will be shifted into the AT25080B/160B, and the serial output pin (SO) will remain in a high-impedance state until the falling edge of $\overline{CS}$ is detected. This will reinitialize the serial communication.
Chip Select	The AT25080B/160B is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the Serial Output pin (SO) will remain in a high-impedance state.
Hold	The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select the AT25080B/160B. When the device is selected and a serial sequence is underway, Hold can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during Hold). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.
Write Protect	The Write Protect pin ($\overline{WP}$) allows normal Read and Write operations when held high. When the WP pin is brought low and WPEN bit is one, all write operations to the status register are inhibited. When the $\overline{WP}$ is low while $\overline{CS}$ is low, it will interrupt a Write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any Write operation to the status register. The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is zero. This will allow the user to install the AT25080B/160B in a system with the $\overline{WP}$ pin tied to ground, and it will be able to write to the status register. All $\overline{WP}$ pin functions are enabled when the WPEN bit is set to one.

Figure 5-1. SPI Serial Interface



6. Functional Description

The AT25080B/160B is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of the 6805 and 68HC11 microcontroller series.

The AT25080B/160B utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in the table below. All instructions, addresses, and data are transferred with the MSB first and starts with a high-to-low CS transition.

Table 6-1. Instruction Set for the AT25080B/160B

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
Read	0000 X011	Read Data from Memory Array
Write	0000 X010	Write Data to Memory Array

Write Enable (WREN): The device will power up in the Write Disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

Write Disable (WRDI): To protect the device against inadvertent writes, the WRDI instruction disables all programming modes. The WRDI instruction is independent of the status of the WP pin.

Read Status Register (RDSR): The RDSR instruction provides access to the status register. The Ready/Busy and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 6-2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	$\overline{\text{RDY}}$

Table 6-3. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{\text{RDY}}$)	If zero, it indicates the device is ready. If one, it indicates the write cycle is in progress.
Bit 1 (WEN)	If zero, it indicates the device is <i>not</i> write enabled. If one, it indicates the device is write enabled.
Bit 2 (BP0)	See Table 6-4 on page 10 .
Bit 3 (BP1)	See Table 6-4 .
Bits 4 to 6	These are zeros when device is not in an internal write cycle.
Bit 7 (WPEN)	See Table 6-5 on page 10
Bits 0 to 7	These are ones during an internal write cycle.

Write Status Register (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25080B/160B is divided into four array segments. One-quarter (1/4), one-half (1/2), or all of the memory segments can be protected. Any of the data within any selected segment will be read-only. The block write protection levels and corresponding status register control bits are shown in Table 6-4.

The three bits BP0, BP1, and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g., WREN, t_{WC} , RDSR).

Table 6-4. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected	
	BP1	BP0	AT25080B	AT25160B
0	0	0	None	None
1(1/4)	0	1	0300 – 03FF	0600 – 07FF
2(1/2)	1	0	0200 – 03FF	0400 – 07FF
3(All)	1	1	0000 – 03FF	0000 – 07FF

The WRSR instruction allows the user to enable or disable the Write Protect ($\overline{WP}$) pin through the use of the Write Protect Enable (WPEN) bit. Hardware Write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is one. Hardware Write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is zero. When the device is hardware write protected, writes to the status register, including the block protect bits and the WPEN bit, and the block-protected sections in the memory array are disabled. Writes are only allowed to sections of the memory that are not block-protected.

Note: When the WPEN bit is Hardware Write protected, it cannot be changed back to zero as long as the $\overline{WP}$ pin is held low.

Table 6-5. WPEN Operation

WPEN	$\overline{WP}$	WEN	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writeable	Writeable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writeable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writeable	Writeable

Read Sequence (Read): Reading the AT25080B/160B via the Serial Output (SO) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the read opcode is transmitted via the SI line followed by the byte address to be read (A15 to A0, see Table 6-6). Upon completion, any data on the SI line will be ignored. The data (D7 to D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll-over to the lowest address allowing the entire memory to be read in one continuous read cycle.

Write Sequence (Write): In order to program the AT25080B/160B, two separate instructions must be executed. First, the device **must be write enabled** via the WREN instruction, and then a Write instruction can be executed. The address of the memory location(s) to be programmed must be outside the protected address field location selected by the block write protection level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the Write opcode is transmitted via the SI line followed by the byte address (A15 to A0) and the data (D7 to D0) to be programmed (see Table 6-6). Programming will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low-time immediately after clocking in the D0 (LSB) data bit.

The Ready/Busy status of the device can be determined by initiating a RDSR instruction. If Bit 0 is one, the write cycle is still in progress. If Bit 0 is zero, the write cycle has ended. Only the RDSR instruction is enabled during the write programming cycle.

The AT25080B/160B is capable of a 32-byte Page Write operation. After each byte of data is received, the five low-order address bits are internally incremented by one; the high-order bits of the address will remain constant. If more than 32 bytes of data are transmitted, the address counter will roll-over and the previously written data will be overwritten. The AT25080B/160B is automatically returned to the write disable state at the completion of a write cycle.

Note: If the device is *not* write-enabled (WREN), the device will ignore the Write instruction and will return to the standby state when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to reinstate the serial communication.

Table 6-6. Address Key

Address	AT25080B	AT25160B
A_N	$A_9 - A_0$	$A_{10} - A_0$
Don't Care Bits	$A_{15} - A_{10}$	$A_{15} - A_{11}$

7. Timing Diagrams

Figure 7-1. Synchronous Data Timing (for Mode 0)

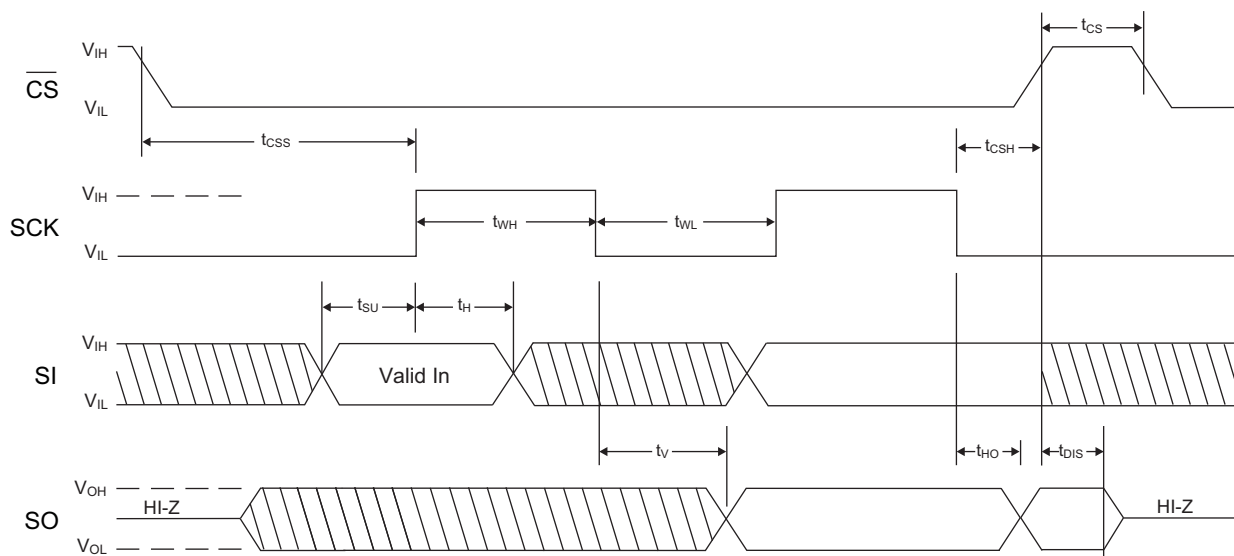


Figure 7-2. WREN Timing

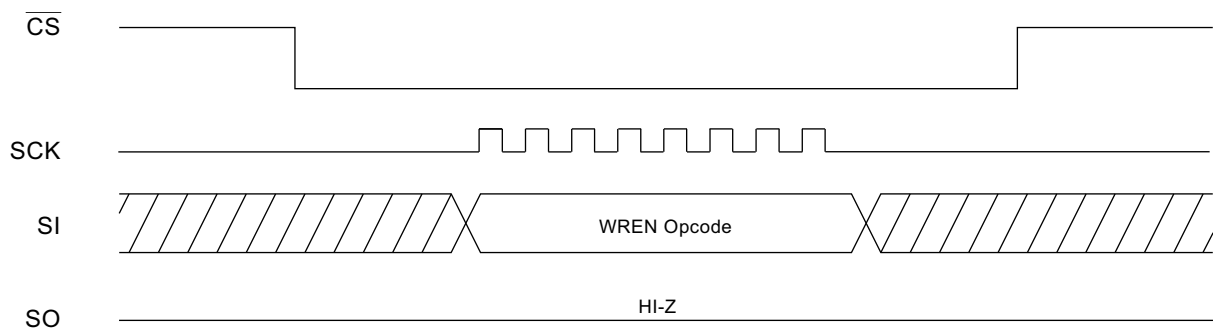


Figure 7-3. WRDI Timing

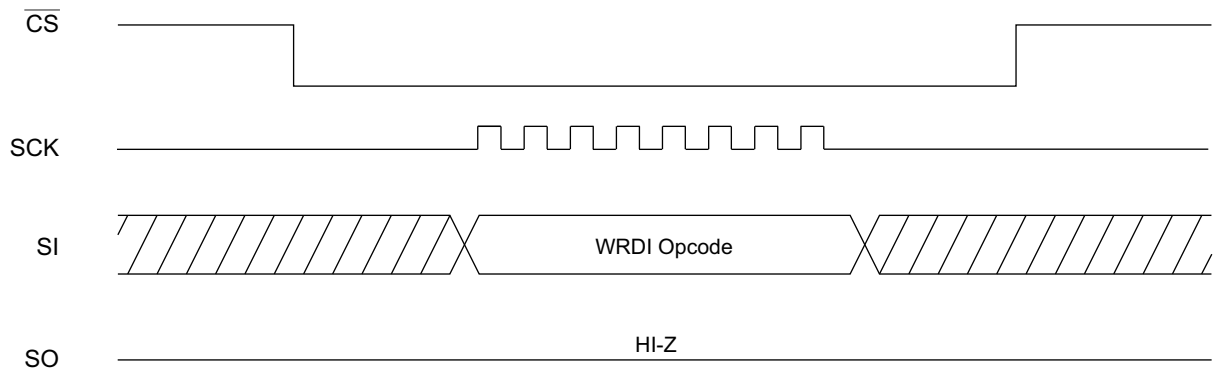


Figure 7-4. RDSR Timing

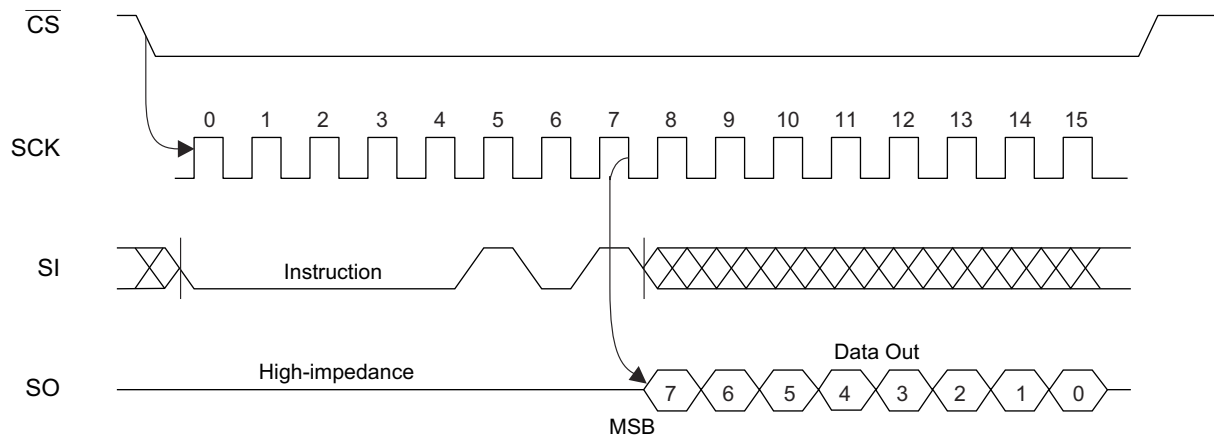


Figure 7-5. WRSR Timing

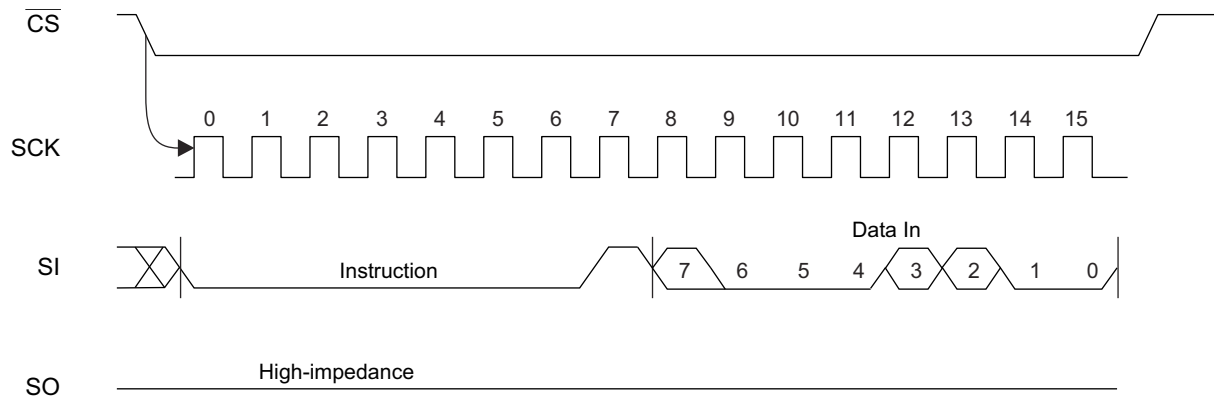


Figure 7-6. Read Timing

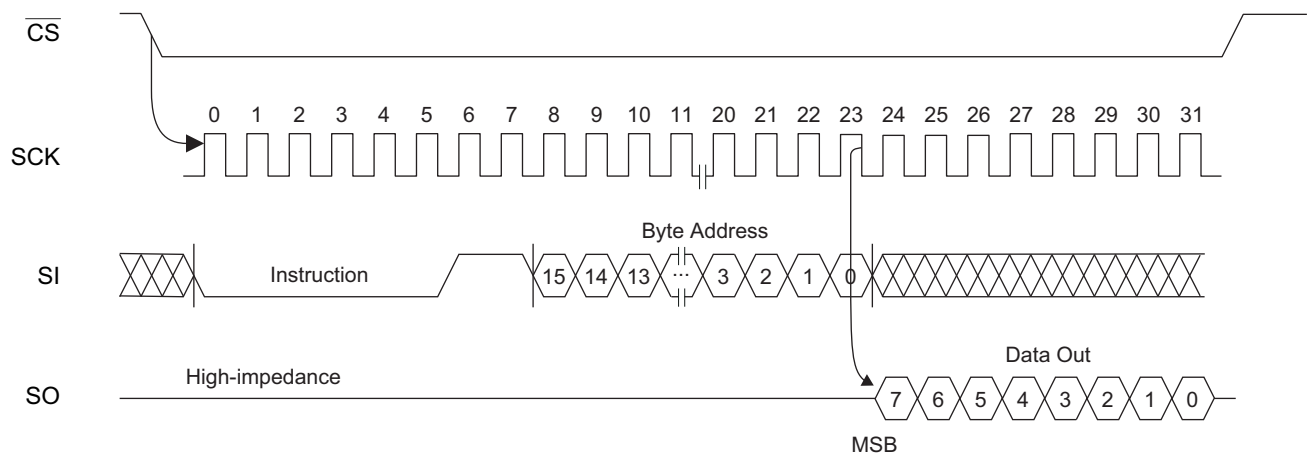


Figure 7-7. Write Timing

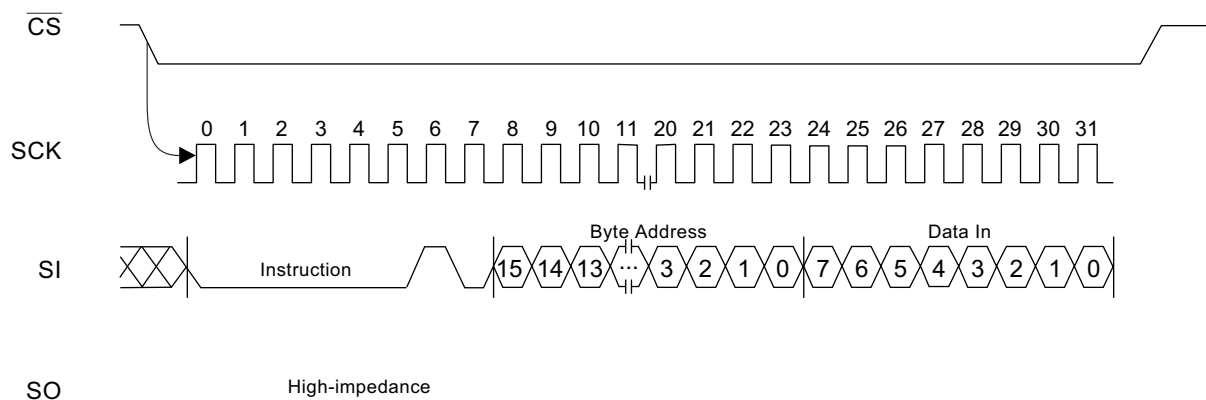
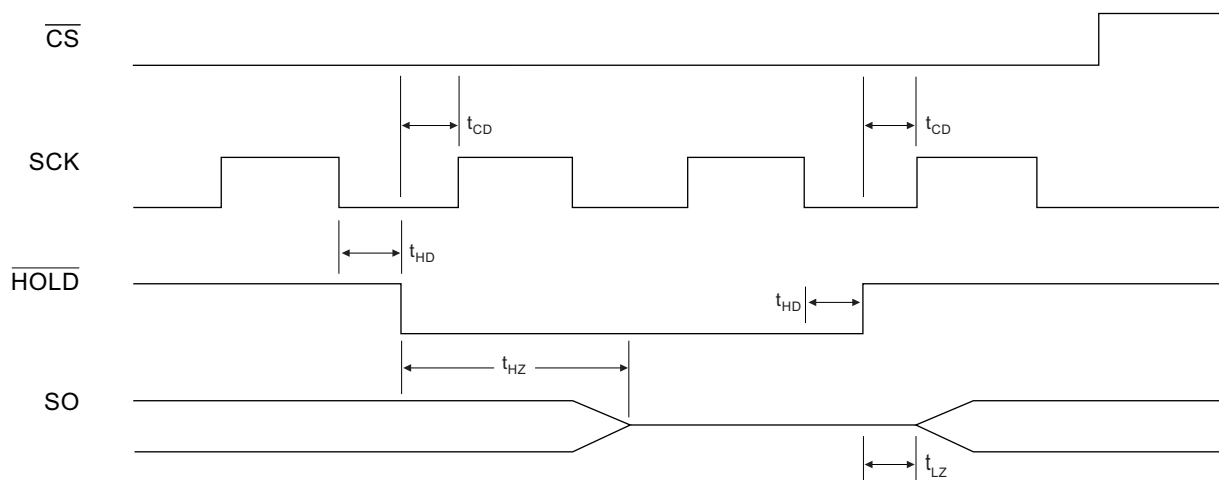
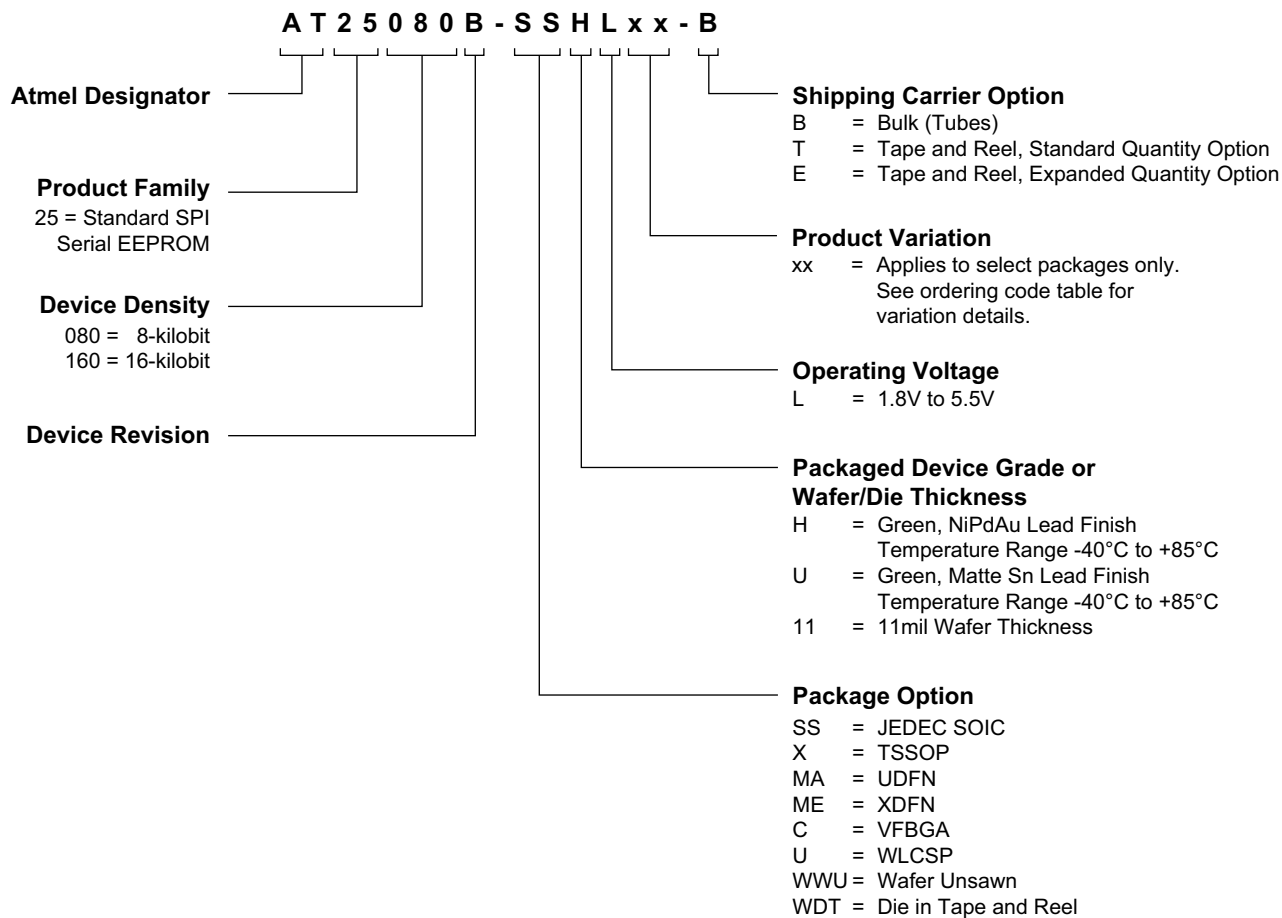


Figure 7-8. HOLD Timing

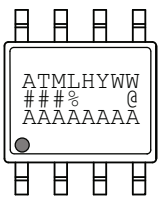


8. Ordering Code Detail



9. Part Markings

AT25080B and AT25160B: Package Marking Information

8-lead SOIC	8-lead TSSOP	8-pad UDFN
		2.0 x 3.0 mm Body 
8-pad XDFN	8-ball VFBGA	8-ball WLCSP
1.8 x 2.2 mm Body 	1.5 x 2.0 mm Body 	

Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT25080B		Truncation Code ###: 58B	
AT25160B		Truncation Code ###: 5AB	
Date Codes			Voltages
Y = Year	M = Month	WW = Work Week of Assembly	% = Minimum Voltage
4: 2014 8: 2018	A: January	02: Week 2	L: 1.8V min
5: 2015 9: 2019	B: February	04: Week 4	
6: 2016 0: 2020			
7: 2017 1: 2021	L: December	52: Week 52	
Country of Assembly		Lot Number	Grade/Lead Finish Material
@ = Country of Assembly		AAA...A = Atmel Wafer Lot Number	H: Industrial/NiPdAu
Trace Code			Atmel Truncation
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

6/10/14

 Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE 25080-160BSM , AT25080B and AT25160B Package Marking Information		DRAWING NO. 25080-160BSM	REV. B

10. Ordering Information

Atmel Ordering Code	Lead Finish	Package	Delivery Information		Operation Range
			Form	Quantity	
AT25080B-SSHL-B	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	Industrial Temperature (-40 to 85°C)
AT25080B-SSHL-T			Tape and Reel	4,000 per Reel	
AT25080B-XHL-B		8X	Bulk (Tubes)	100 per Tube	
AT25080B-XHL-T			Tape and Reel	5,000 per Reel	
AT25080B-MAHL-T		8MA2	Tape and Reel	5,000 per Reel	
AT25080B-MAHL-E			Tape and Reel	15,000 per Reel	
AT25080B-MEHL-T		8ME1	Tape and Reel	5,000 per Reel	
AT25080B-CUL-T	SnAgCu (Lead-free/Halogen-free)	8U3-1	Tape and Reel	5,000 per Reel	
AT25080B-UUL0B-T ⁽¹⁾		8U-12	Tape and Reel	5,000 per Reel	
AT25080B-WWU11L ⁽²⁾	N/A	Wafer Sale	Note 2		
AT25160B-SSHL-B	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	Industrial Temperature (-40 to 85°C)
AT25160B-SSHL-T			Tape and Reel	4,000 per Reel	
AT25160B-XHL-B		8X	Bulk (Tubes)	100 per Tube	
AT25160B-XHL-T			Tape and Reel	5,000 per Reel	
AT25160B-MAHL-T		8MA2	Tape and Reel	5,000 per Reel	
AT25160B-MAHL-E			Tape and Reel	15,000 per Reel	
AT25160B-MEHL-T		8ME1	Tape and Reel	5,000 per Reel	
AT25160B-CUL-T	SnAgCu (Lead-free/Halogen-free)	8U3-1	Tape and Reel	5,000 per Reel	
AT25160B-UUL0B-T ⁽¹⁾		8U-12	Tape and Reel	5,000 per Reel	
AT25160B-WWU11L ⁽²⁾	N/A	Wafer Sale	Note 2		

Notes: 1. WLCSP Package:

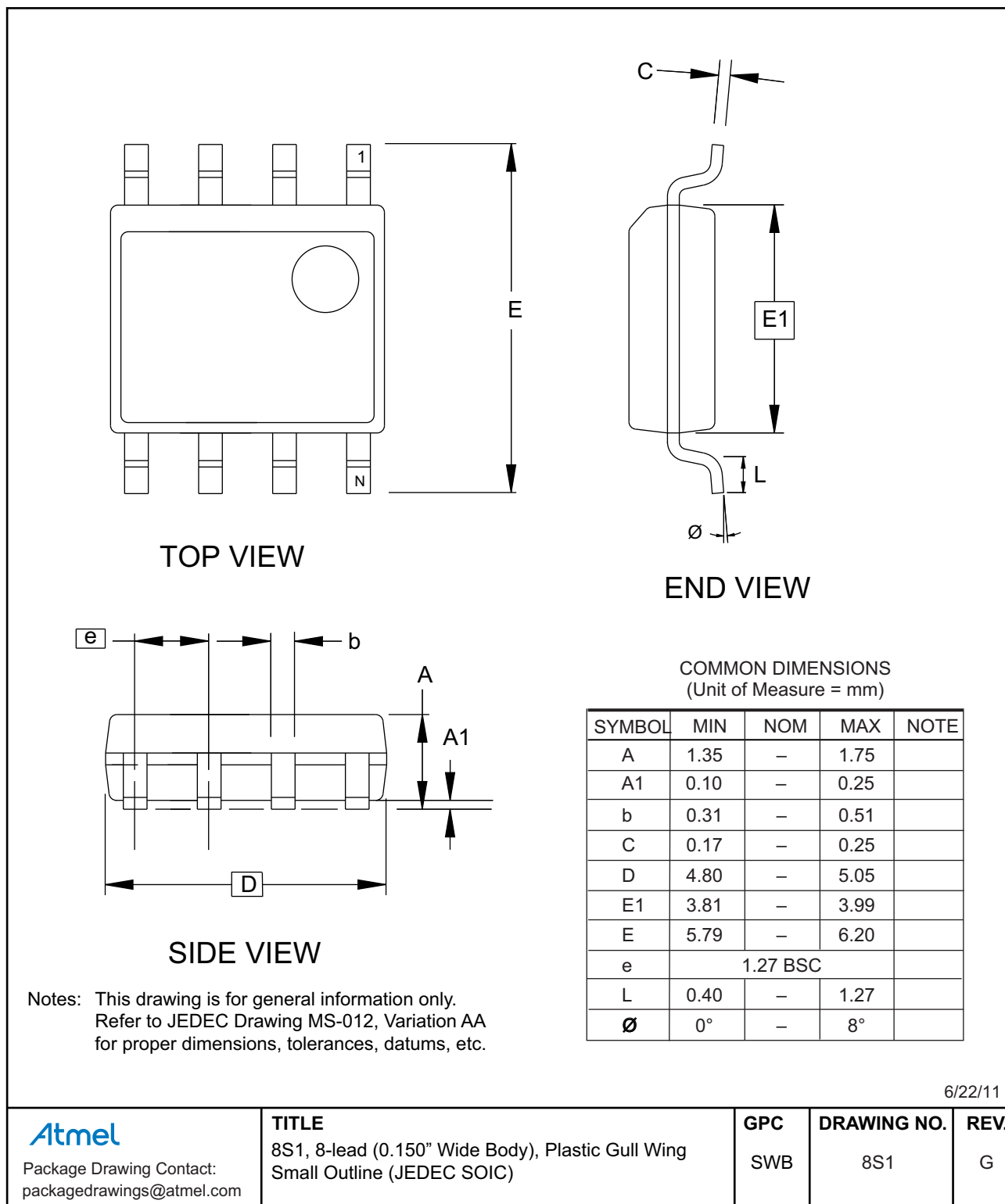
- This device includes a backside coating to increase product robustness.
- **CAUTION:** Exposure to ultraviolet (UV) light can degrade the data stored in the EEPROM cells. Therefore, customers who use a WLCSP product must ensure that exposure to ultraviolet light does **not** occur.

2. Contact Atmel Sales for Wafer sales.

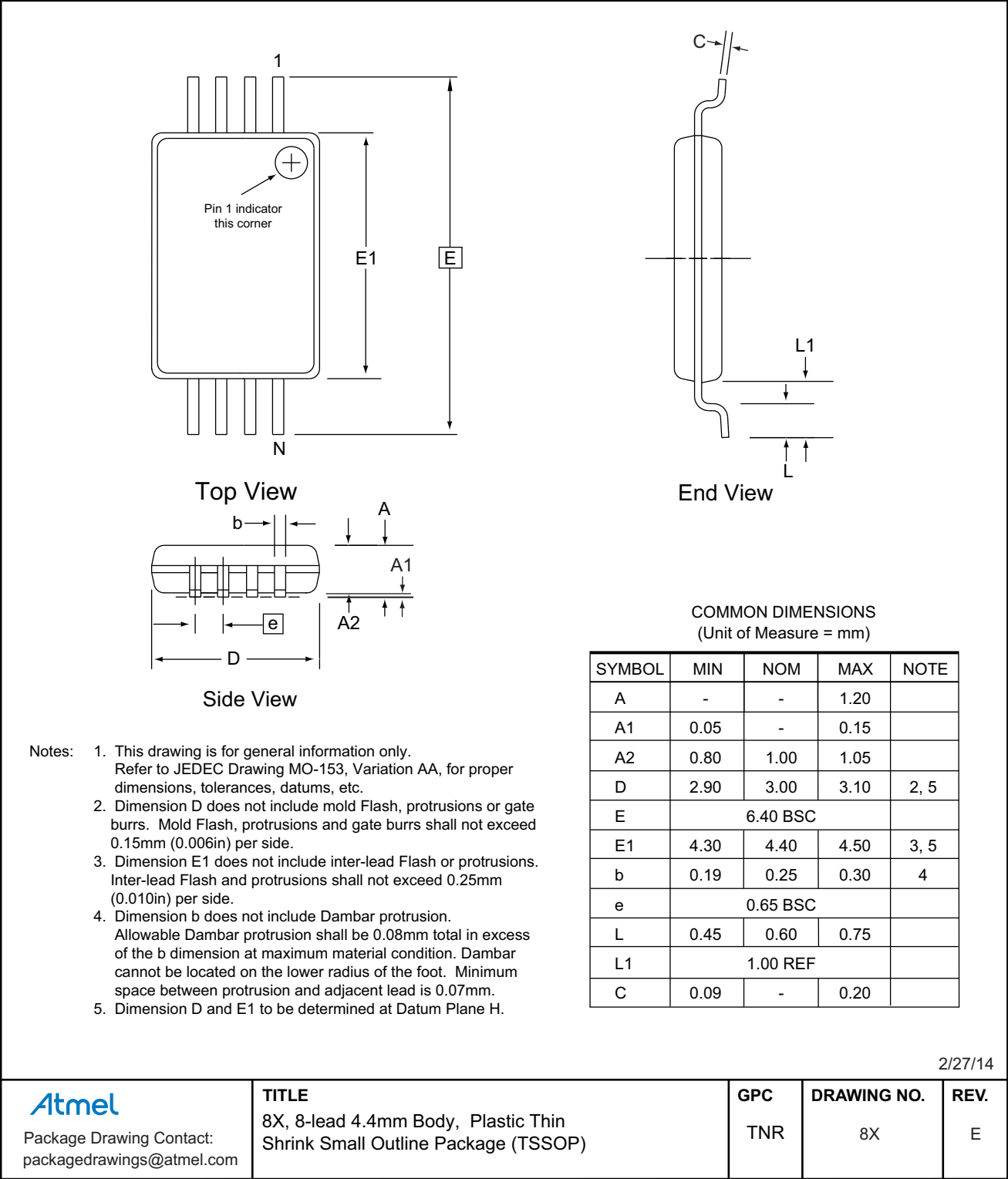
Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline Package (TSSOP)
8MA2	8-pad, 2.0mm x 3.0mm x 0.6mm body, Thermally Enhanced Plastic Ultra Thin Dual Flat Dual No Lead (UDFN)
8ME1	8-pad 1.8mm x 2.2mm body, Extra Thin DFN (XDFN)
8U3-1	8-ball, 1.50mm x 2.00mm body, 0.50mm pitch, Very Thin, Fine-Pitch Ball Grid Array (VFBGA)
8U-12	8-ball, 5 x 3 grid array, 0.40mm pitch, Wafer Level Chip Scale Package (WLCSP)

11. Packaging Information

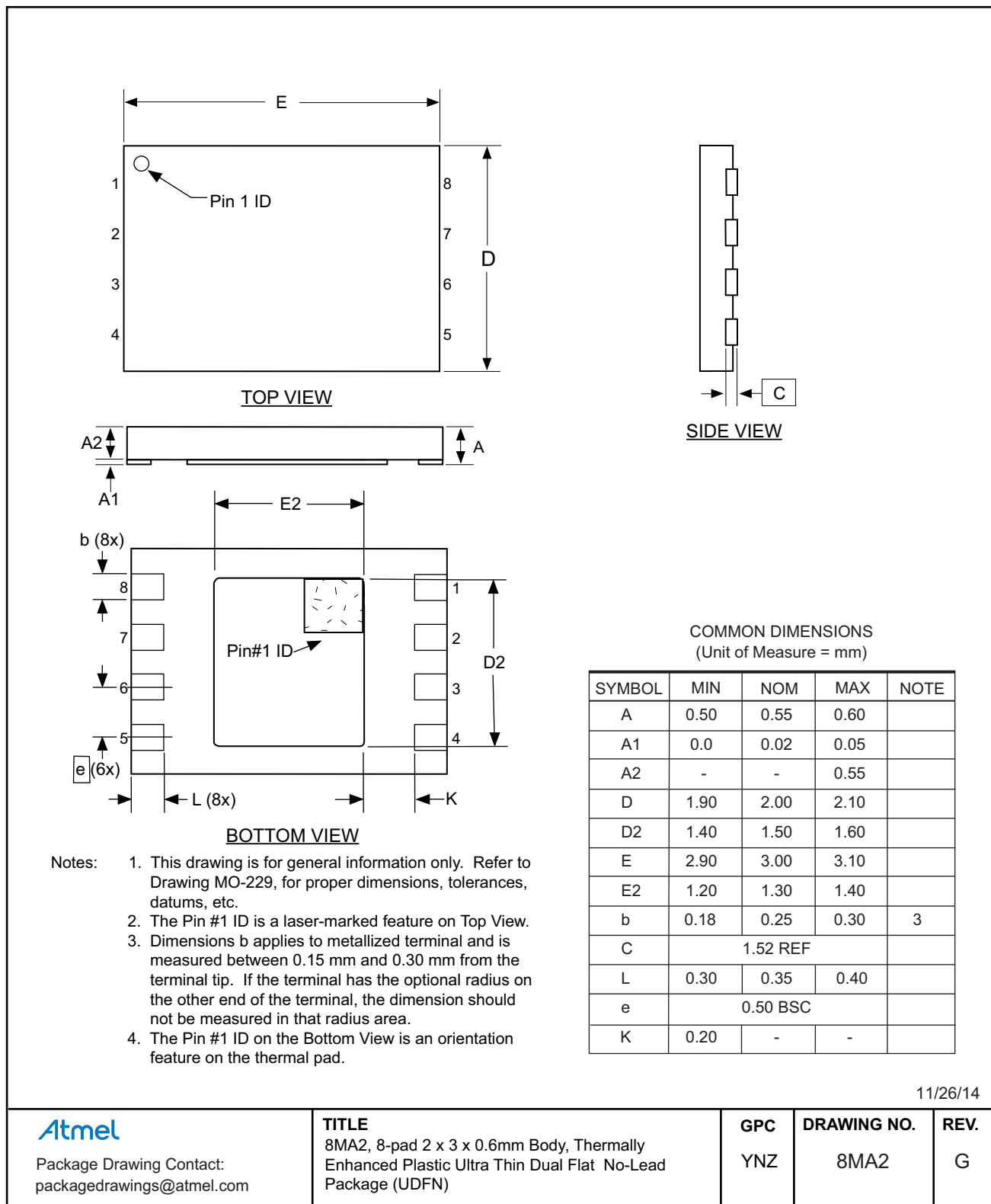
11.1 8S1 — 8-lead JEDEC SOIC



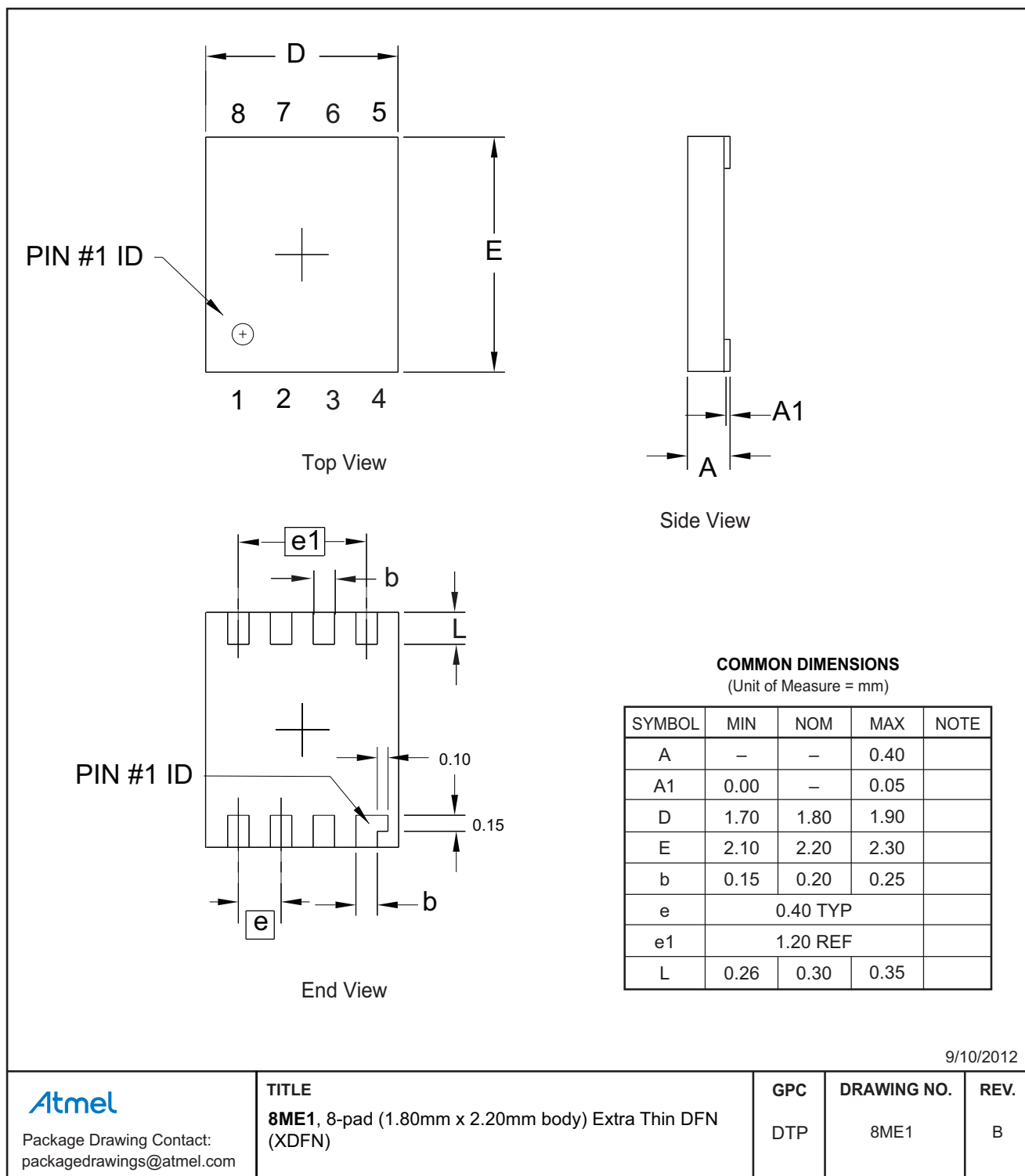
11.2 8X — 8-lead TSSOP



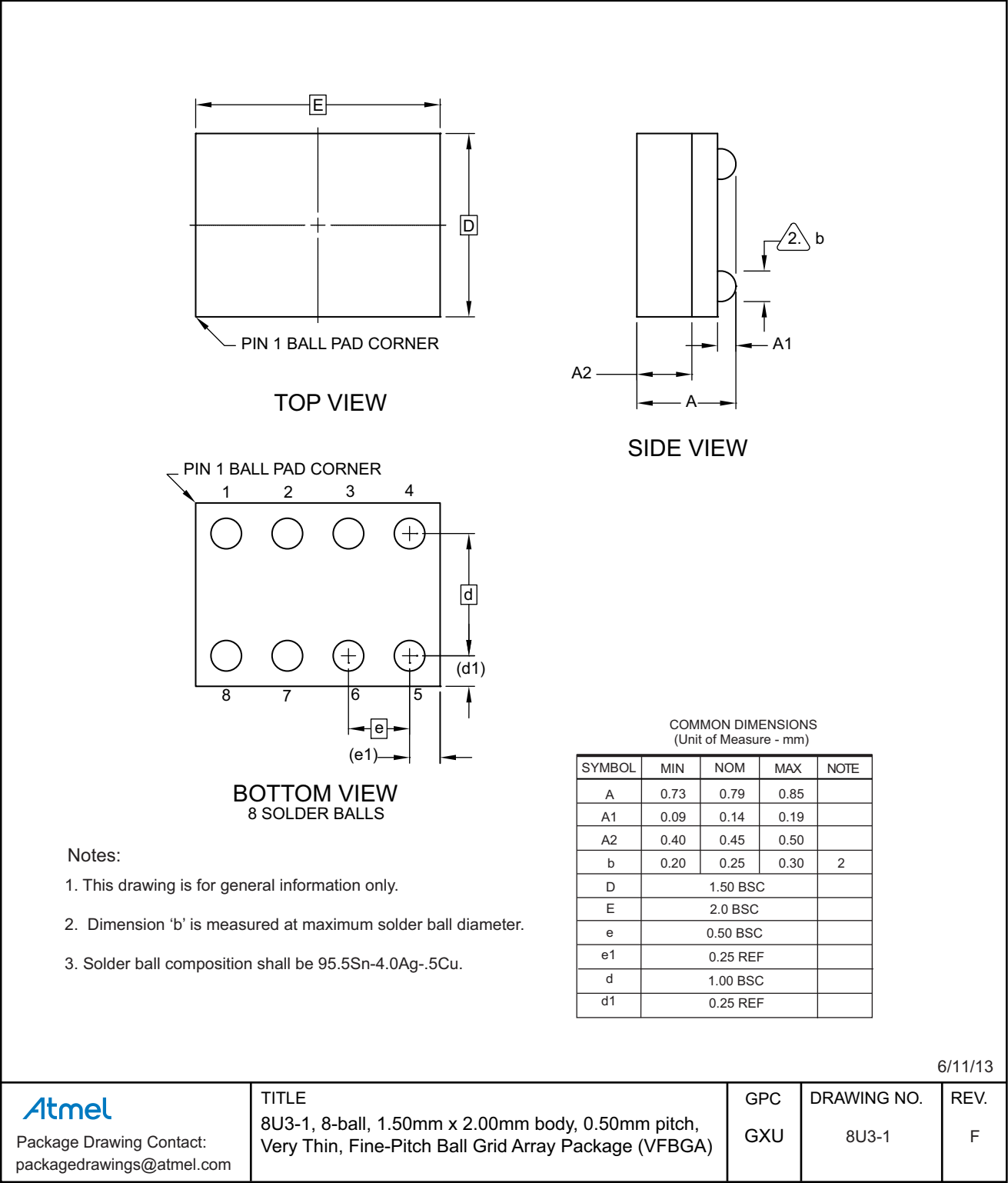
11.3 8MA2 — 8-pad UDFN



11.4 8ME1 — 8-pad XDFN



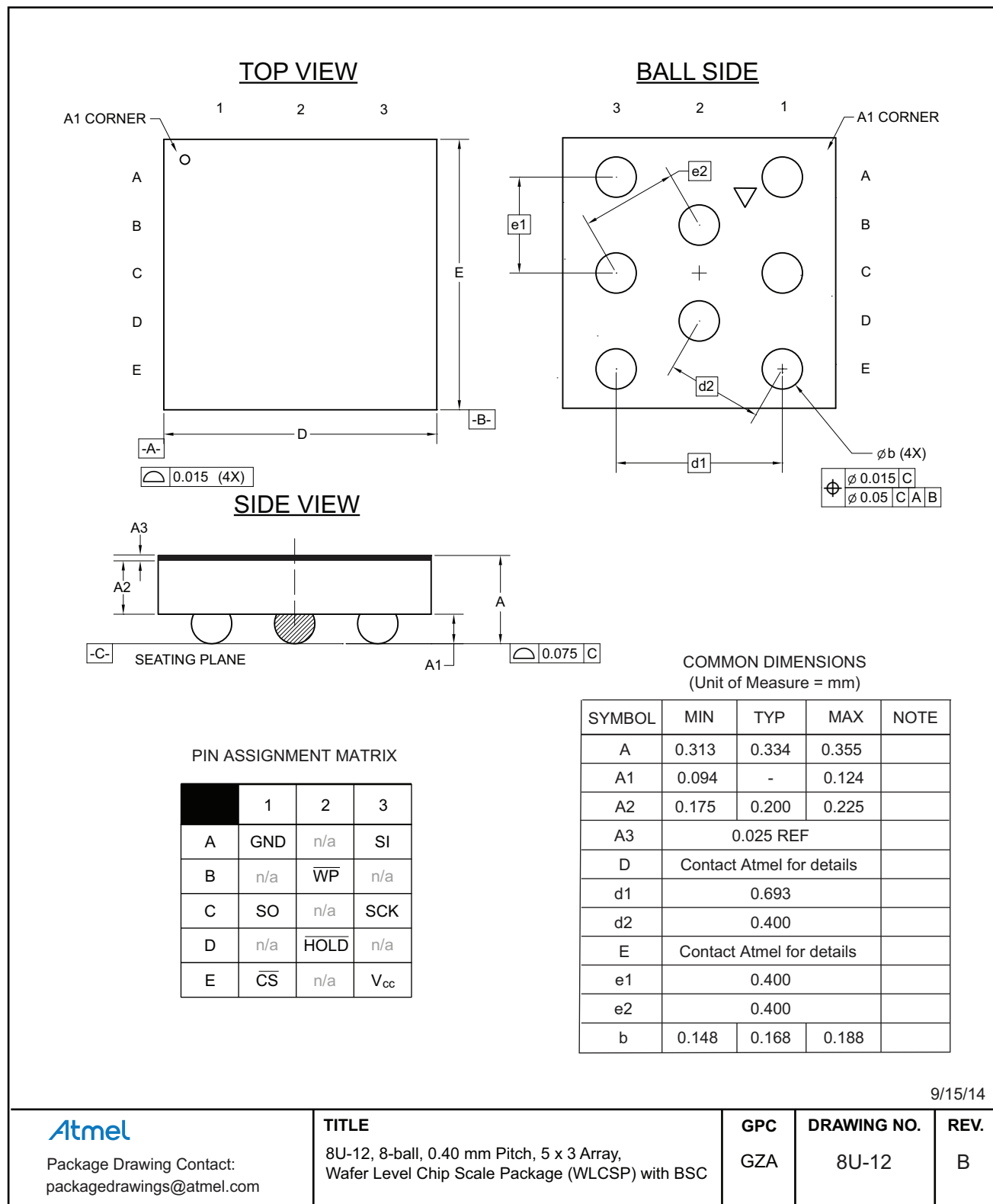
11.5 8U3-1 — 8-ball VFBGA



6/11/13

 Package Drawing Contact: packagedrawings@atmel.com	TITLE 8U3-1, 8-ball, 1.50mm x 2.00mm body, 0.50mm pitch, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)	GPC GXU	DRAWING NO. 8U3-1	REV. F
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11.6 8U-12 — 8-ball WLCSP



12. Revision History

Doc. Rev.	Date	Comments
5228G	01/2015	Add the AT25080B-MAHL-E and AT25160B-MAHL-E package options. Update the 8MA2 and 8U-12 package drawings and the ordering information.
5228F	07/2014	Add WLSCP package option. Update 8X, 8MA2, 8ME1, and 8U3-1 package drawings. Update template, Atmel logos, disclaimer page.
5228E	03/2012	Update 8A2 to 8X and 8S1, 8MA2, 8U3-1 package drawings.
5228D	04/2010	Update Ordering Code Detail and Ordering Information.
5228C	08/2009	Change Catalog Scheme and add Marking Details.
5228B	07/2008	Change 'Endurance' parameter on page 6.
5228A	09/2007	Initial document release.



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