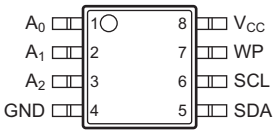
1. Pin Configurations and Pinouts

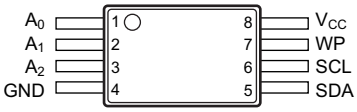
Table 1-1. Pin Configurations

Pin Name	Function
$A_0 - A_2$	Address Inputs
GND	Ground
V_{CC}	Power Supply
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

8-lead SOIC
(Top View)



8-lead TSSOP
(Top View)



Note: Drawings are not to scale.

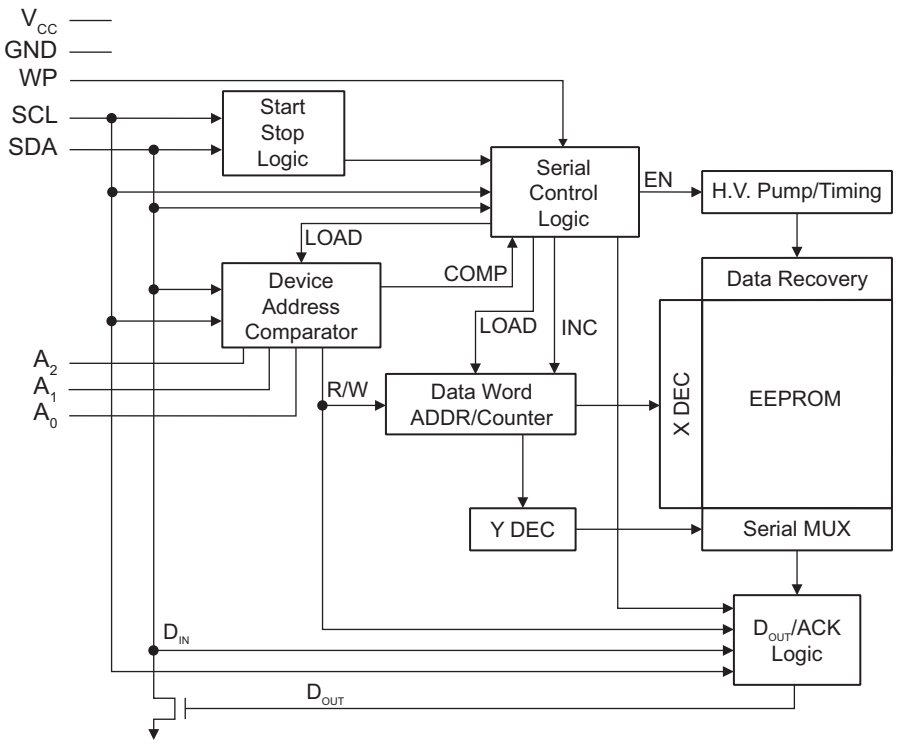
2. Absolute Maximum Ratings

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram

Figure 3-1. Block Diagram



4. Pin Descriptions

Serial Clock (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

Device/Page Addresses (A_2, A_1, and A_0): The A_2, A_1, and A_0 pins are device address inputs that are hard wired for the AT24HC02B. As many as eight 2K devices may be addressed on a single bus system (see Section 7., “Device Addressing”).

The AT24HC04B uses the A_2 and A_1 inputs for hardware addressing, and a total of four 4K devices may be addressed on a single bus system. The A_0 pin is a no connect.

Write Protect (WP): The AT24HC02B/04B have a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal Read/Write operations when connected to Ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

Table 4-1. Write Protect

WP Pin Status	Part of the Array Protected
At V_{CC}	Upper Half (1K/2K) Array
At GND	Normal Read/Write Operations

5. Memory Organization

AT24HC02B, 2K Serial EEPROM: Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.

AT24HC04B, 4K Serial EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires an 9-bit data word address for random word addressing.

5.1 Pin Capacitance

Table 5-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = +2.5V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

5.2 DC Characteristics

Table 5-2. DC Characteristics

Applicable over recommended operating range from: T_A = -40°C to +125°C, V_{CC} = +2.5V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		2.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	Read at 100kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	Write at 100kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB2}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]		–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Level V_{CC} = 2.5V	I_{OL} = 3.0mA			0.4	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

5.3 AC Characteristics

Table 5-3. AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +125°C, V_{CC} = +2.5V to +5.5V, CL = 1 TTL Gate and 100pF (unless otherwise noted).

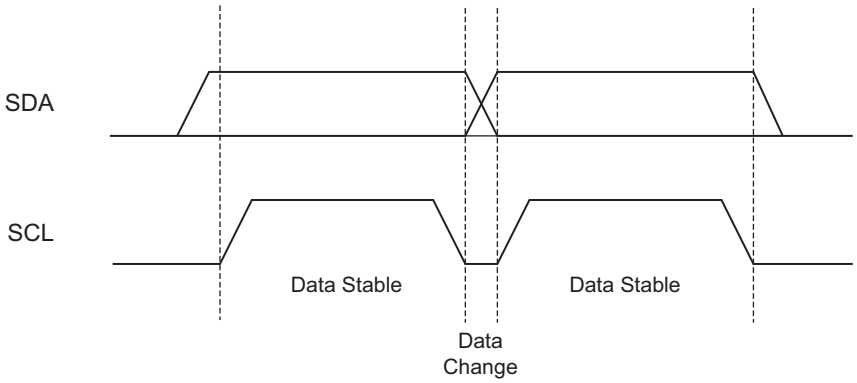
Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		400	kHz
t_{LOW}	Clock Pulse Width Low	1.2		µs
t_{HIGH}	Clock Pulse Width High	0.6		µs
t_I	Noise Suppression Time(1)		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start.(2)	1.2		µs
$t_{HD.STA}$	Start Hold Time	0.6		µs
$t_{SU.STA}$	Start Set-up Time	0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		ns
t_R	Inputs Rise Time(2)		300	ns
t_F	Inputs Fall Time(2)		300	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		µs
t_{DH}	Data Out Hold Time	50		ns
t_{WR}	Write Cycle Time		5	ms
Endurance(2)	5.0V, 25°C, Page Mode	1,000,000		Write Cycles

Notes: 1. This parameter is characterized and is not 100% tested (T_A = 25°C).
2. This parameter is ensured by characterization only.

6. Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

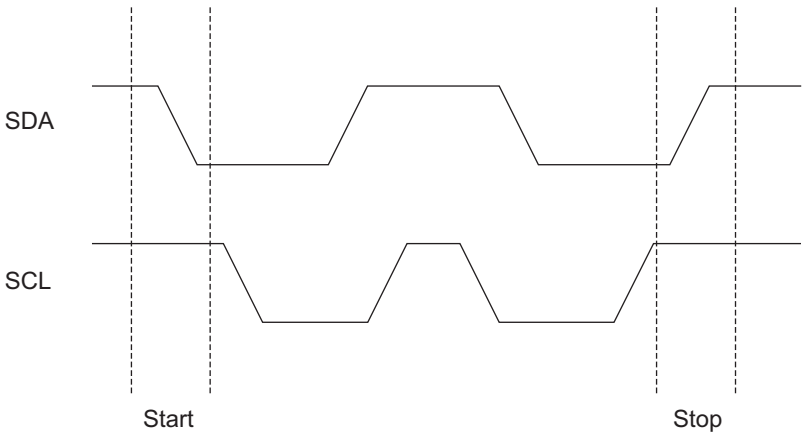
Figure 6-1. Data Validity



Start Condition: A high-to-low transition of SDA with SCL high is a Start condition which must precede any other command.

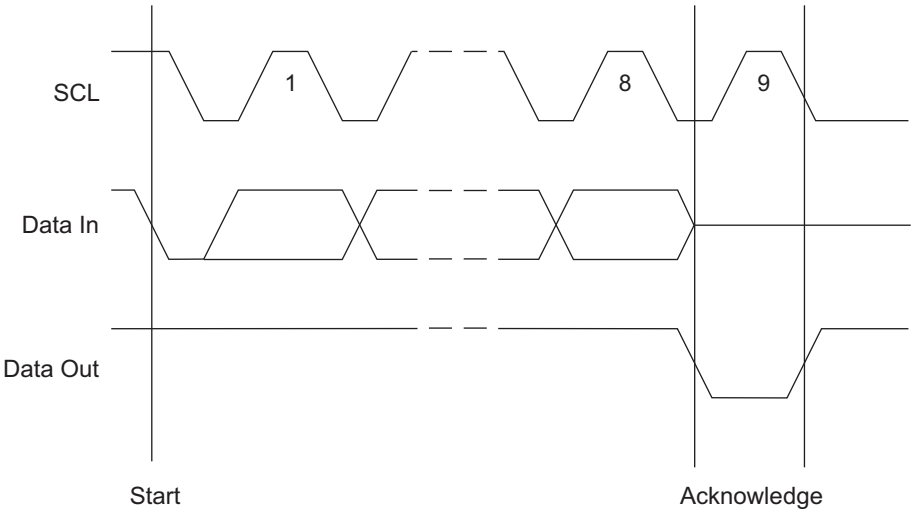
Stop Condition: A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the Stop command will place the EEPROM in a standby power mode.

Figure 6-2. Start and Stop Definition



Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Figure 6-3. Output Acknowledge



Standby Mode: The AT24HC02B/04B features a low-power standby mode which is enabled:

- Upon power-up.
- After the receipt of the Stop condition and the completion of any internal operations.

Software Reset: After an interruption in protocol, power loss or system reset, any 2-Wire part can be protocol reset by following these steps:

- Create a Start condition,
- Clock nine cycles, and
- Create another Start condition followed by Stop condition.

The device is ready for the next communication after above steps have been completed.

Figure 6-4. Software Reset Protocol

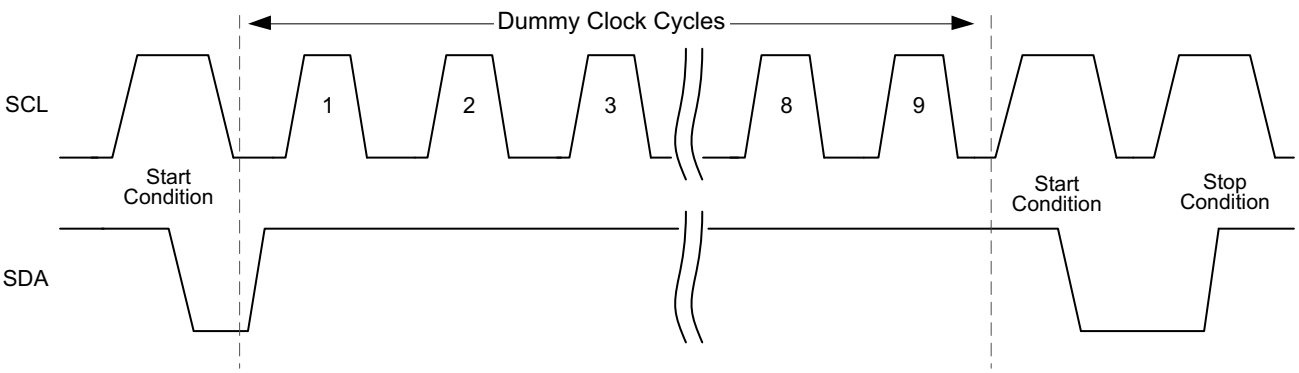


Figure 6-5. Bus Timing: SCL — Serial Clock, SDA: Serial Data I/O

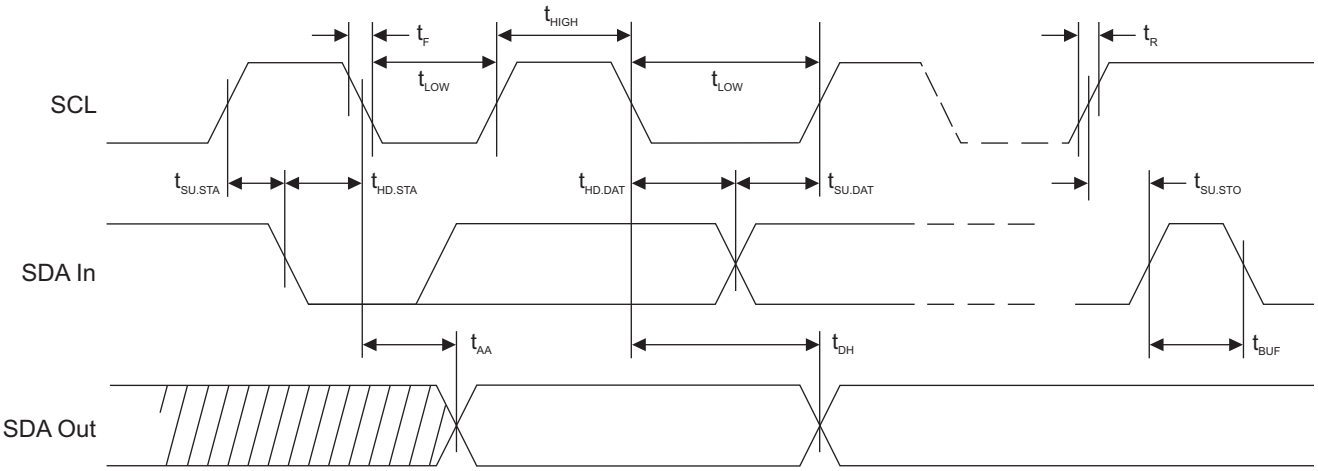
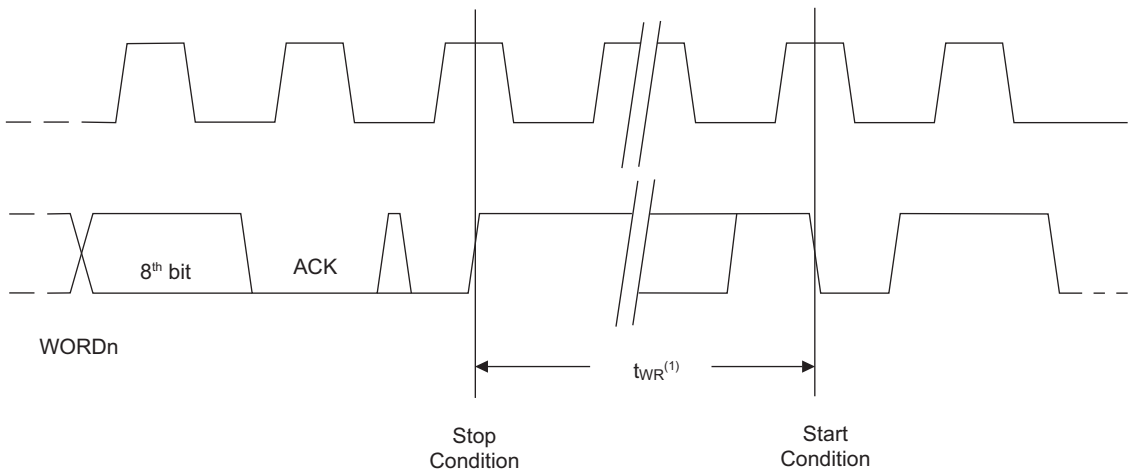


Figure 6-6. Write Cycle Timing: SCL – Serial Clock, SDA – Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid Stop condition of a write sequence to the end of the internal clear/write cycle.

7. Device Addressing

The 2Kand 4K EEPROM devices all require an 8-bit device address word following a Start condition to enable the device for a Read or Write operation.

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

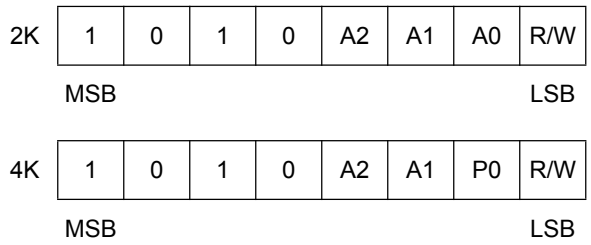
The next three bits are the A2, A1, and A0 device address bits for the 2K EEPROM. These three bits must compare to their corresponding hardwired input pins.

The 4K EEPROM only uses the A2 and A1 device address bits with the third bit being a memory address bit. The two device address bits must compare to their corresponding hardwired input pins. The A_0 pin is no connect.

The eighth bit of the device address is the Read/Write operation select bit. A Read operation is initiated if this bit is high and a Write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

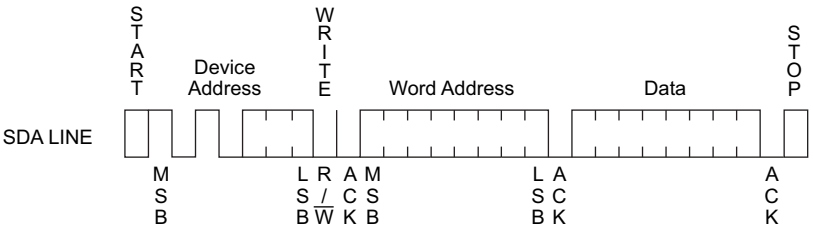
Figure 7-1. Device Address



8. Write Operations

Byte Write: A Write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the Write sequence with a Stop condition. At this time, the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the Write is complete.

Figure 8-1. Byte Write

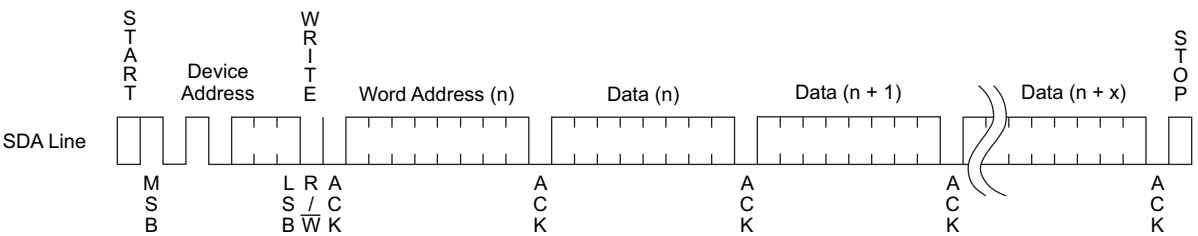


Page Write: The 2K EEPROM is capable of an 8-byte Page Write, and the 4K EEPROM device is capable of 16-byte Page Writes.

A Page Write is initiated the same as a Byte Write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven (2K) or fifteen (4K) more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the Page Write sequence with a Stop condition.

The data word address lower three bits (2K) or four (4K) are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight (2K) or sixteen (4K) data words are transmitted to the EEPROM, the data word address will roll-over and previous data will be overwritten.

Figure 8-2. Page Write



Acknowledge Polling: Once the internally timed write cycle has started and the EEPROM inputs are disabled, Acknowledge Polling can be initiated. This involves sending a Start condition followed by the device address word. The Read/Write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the Read or Write sequence to continue.

9. Read Operations

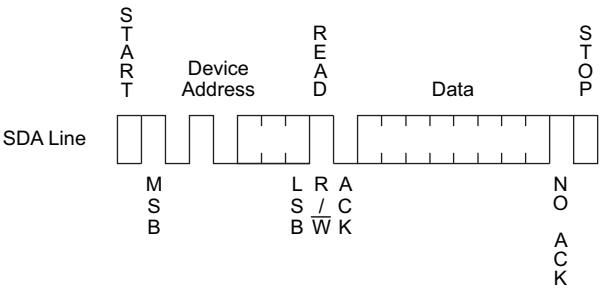
Read operations are initiated the same way as Write operations with the exception that the Read/Write select bit in the device address word is set to one. There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read

Current Address Read: The internal data word address counter maintains the last address accessed during the last Read or Write operation, incremented by one. This address stays valid between operations as long as the device power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

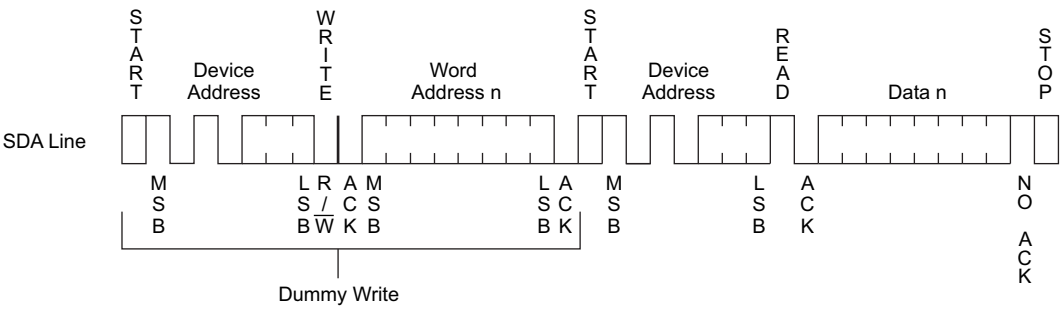
Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following Stop condition.

Figure 9-1. Current Address Read



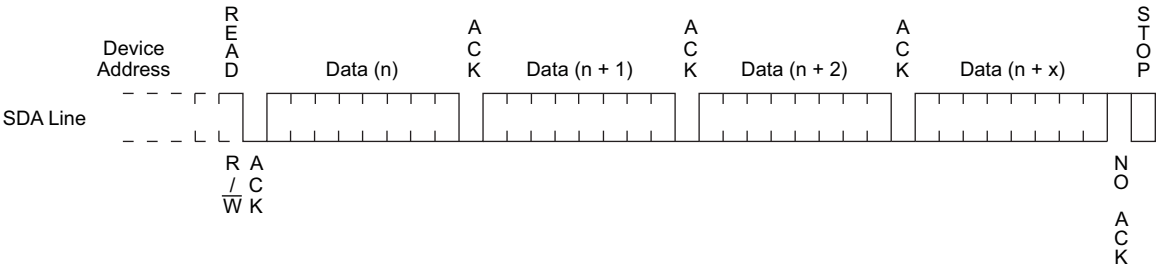
Random Read: A random Read requires a “dummy” Byte Write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another Start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following Stop condition.

Figure 9-2. Random Read



Sequential Read: Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a zero but does generate a following Stop condition.

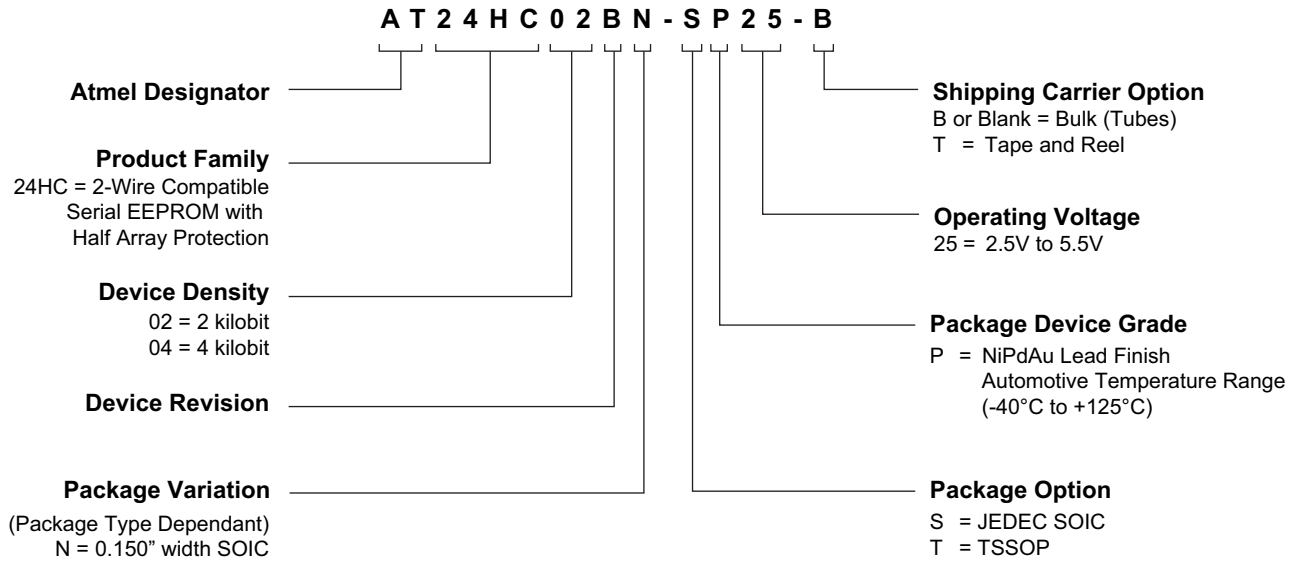
Figure 9-3. Sequential Read



10. Power Recommendation

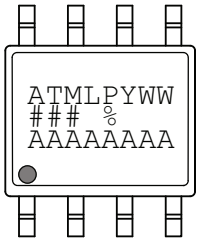
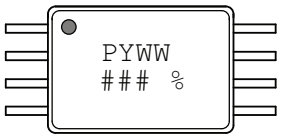
The device internal POR (Power-On Reset) threshold is just below the minimum operating voltage of the device. Power shall rise monotonically from 0.0Vdc to full V_{CC} in less than 1ms. Hold at full V_{CC} for at least 100µs before the first operation. Power shall drop from full V_{CC} to 0.0Vdc in less than 1ms. Power dropping to a non-zero level and then slowly going to zero is not recommended. Power shall remain off (0.0Vdc) for 0.5s minimum. Please consult Atmel if your power conditions do not meet the above recommendations.

11. Ordering Code Detail



12. Product Markings

AT24HC02B & AT24HC04B: Automotive Package Marking Information

8-lead SOIC	8-lead TSSOP
	

Note: Lot Number and location of assembly and on the bottom side of the package.

Note 1: ● designates pin 1
Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT24HC02B		Truncation Code ###: H2B	
AT24HC04B		Truncation Code ###: H4B	
Date Codes			**Voltages**
Y = Year		M = Month	WW = Work Week of Assembly	% = Minimum Voltage
4: 2014	8: 2018	A: January	02: Week 2	2: 2.5V min
5: 2015	9: 2019	B: February	04: Week 4	
6: 2016	0: 2020	...	...	
7: 2017	1: 2021	L: December	52: Week 52	
Country of Assembly		**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly		AAA...A = Atmel Wafer Lot Number		P: Automotive/NiPdAu
Trace Code				**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ				AT: Atmel ATM: Atmel ATML: Atmel

4/25/14

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	**TITLE** **24HC02-04BAM**, AT24HC02B & AT24HC04B Automotive Package Marking Information	**DRAWING NO.** 24HC02-04BAM	**REV.** A

13. Ordering Code Information

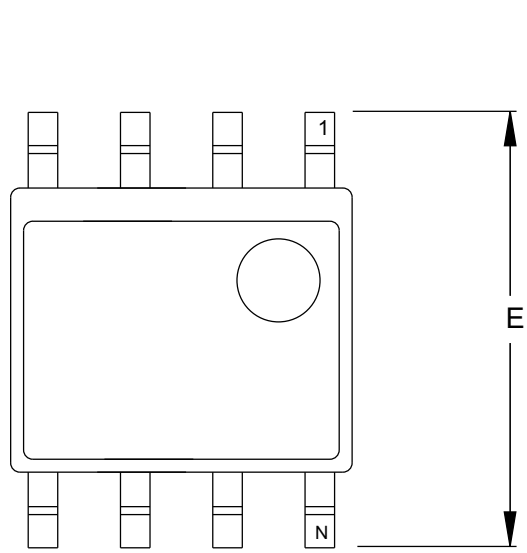
Atmel Ordering Code	Lead Finish	Package	Voltage	Operation Range
AT24HC02BN-SP25-B[1]	NiPdAu Lead Finish (Lead-free/Halogen-free)	8S1	2.5V to 5.5V	Automotive Temperature (–40°C to 125°C)
AT24HC02BN-SP25-T[2]				
AT24HC02B-TP25-B[1]		8X		
AT24HC02B-TP25-T[2]				
AT24HC04BN-SP25-B[1]	NiPdAu Lead Finish (Lead-free/Halogen-free)	8S1	2.5V to 5.5V	Automotive Temperature (–40°C to 125°C)
AT24HC04BN-SP25-T[2]				
AT24HC04B-TP25-B[1]		8X		
AT24HC04B-TP25-T[2]				

Notes: 1. B = Bulk.
2. T = Tape and reel:
   - SOIC = 4,000 per reel.
   - TSSOP = 5,000 per reel.

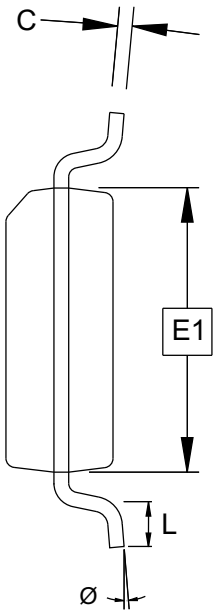
Package Type	
8S1	8-lead, 0.150" wide body, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline Package (TSSOP)

14. Packaging Information

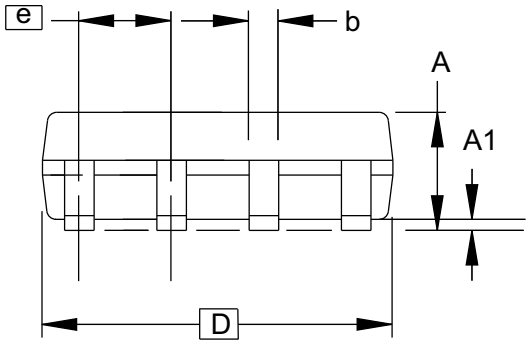
14.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

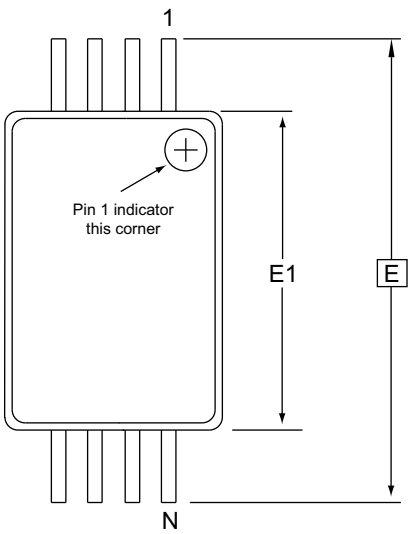
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

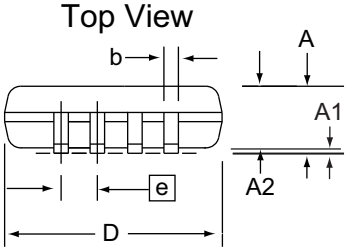
6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	GPC SWB	DRAWING NO. 8S1	REV. G

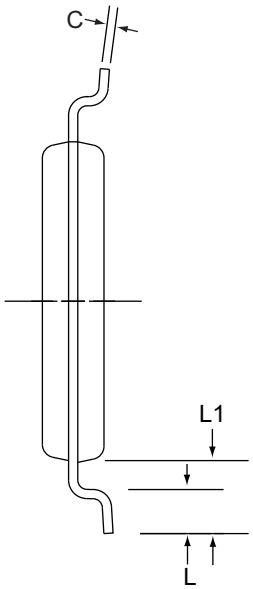
14.2 8X — 8-lead TSSOP



Top View



Side View



End View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	0.25	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

2/27/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	**GPC** TNR	**DRAWING NO.** 8X	**REV.** E

15. Revision History

Doc. Rev.	Date	Comments
5192D	08/2014	Added power recommendation, part markings, and ordering code detail. Updated template, logos, and disclaimer page. No changes to functional specification.
5192C	01/2009	Removed Preliminary status.
5192B	03/2008	Added information for AT24HC04B. Updated to new template.
5192A	01/2007	Initial document release.

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