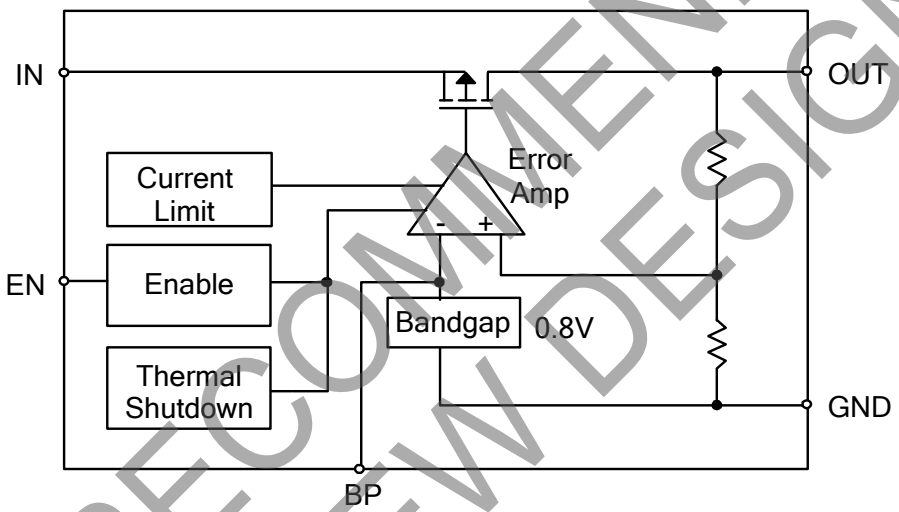
Pin Descriptions

Pin Number	Pin Name	Description
1	IN	Voltage Input
2	GND	Ground
3	EN	Chip Enable Control
4	BP	Band-Gap Bypass
5	OUT	Voltage Output

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	3.5	kV
ESD MM	Machine Model ESD Protection	400	V
V_{IN}	Input Voltage	-0.3 to 5.5	V
V_{EN}	EN Pin Voltage	-0.3 to 5.5	V
V_{OUT}	Output Voltage	-0.3 to V_{IN}+0.3	V
V_{BP}	Band Gap Bypass Pin Voltage	-0.3 to 5.5	V
P_D	Power Dissipation	500	mW
T_J	Operating Junction Temperature Range	-40 to +125	°C
T_{ST}	Storage Temperature Range	-65 to +150	°C

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

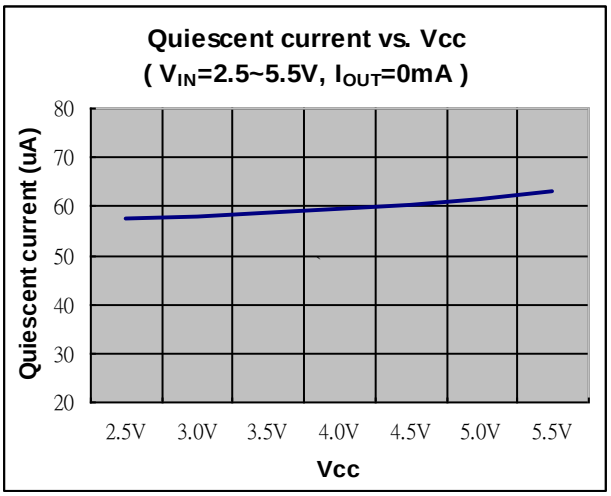
Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	2.5	5.5	V
I_{OUT}	Output Current	—	150	mA
T_A	Operating Ambient Temperature	-40	+85	°C

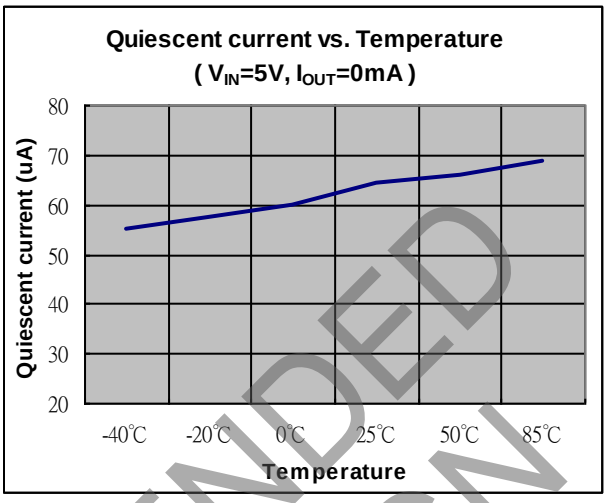
Electrical Characteristics (@V_{CC} = 3.3V, I_L = 30mA, C_{IN} = 1µF, C_{OUT} = 1µF, T_A = +25°C)

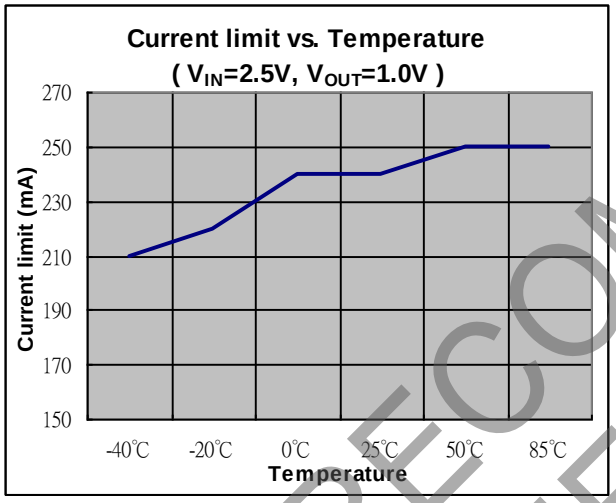
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
System Supply Input						
V_{IN}	Operating Input Voltage	I_L = 0 to 150mA	2.5	—	5.5	V
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Accuracy	$V_{IN} = V_{OUT}$ + 1V where 1mA ≤ I_{OUT} ≤ 50mA	-2	—	2	%
V_{DO}	Dropout Voltage	I_L = 150mA	—	200	300	mV
I_{OUT}	Output Current	$V_{IN} - V_{OUT}$ = 1V	150	—	—	mA
I_Q	Quiescent Current	$V_{IN} = V_{OUT}$ + 1V where I_{OUT} = 0 and $V_{EN} = V_{IN}$	—	50	80	µA
$I_{SHUTDOWN}$	Shutdown Current	$V_{IN} = V_{OUT}$ + 1V where I_{OUT} = 0 and V_{EN} = 0	—	0.1	1	µA
PSRR	Power Supply Rejection Ratio	I_{OUT} = 30mA, f = 1kHz	—	70	—	dB
I_{LIMIT}	Current Limit	—	200	250	—	mA
Thermal Management						
$T_{SHUTDOWN}$	Thermal Shutdown	—	—	+150	—	°C
Reference Voltage						
$\Delta V_{REF}/\Delta T$	Tempco of Bandgap Reference	—	—	30	50	ppm/°C
$\Delta V_{OUT}/\Delta T$	Tempco of Output Voltage	I_{OUT} = 30mA, -40°C ≤ T_A ≤ +85°C	—	50	100	ppm/°C
Control and Protection						
$V_{IH,EN}$	—	—	2.0	—	—	V
$V_{IL,EN}$	—	—	—	—	0.7	V
I_{EN}	EN Pin Leakage Current	$V_{EN} = V_{IN}$ @V_{IN} = 5.0V and V_{SS} = 0V	—	0.01	0.1	µA
		$V_{EN} = V_{SS}$ @V_{IN} = 5.0V and V_{SS} = 0V	—	0.01	0.1	µA
Regulation						
$\Delta V_O/\Delta V_{IN}$	Line Regulation	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V where V_{OUT} > 2.0V, I_{OUT} = 30mA	—	0.02	0.1	%/V
ΔV_{LOAD}	Load Regulation	1mA ≤ I_L ≤ 150mA where $V_{IN} = V_{OUT}$ + 1V	—	0.003	0.006	%/mA
Noise						
e_n	Output Noise	BW = 10Hz to 100kHz	—	50	—	μV_{rms}
Thermal Resistance						
θ_{JA}	Thermal Resistance Junction-to-Ambient	SOT25 (Note 4)	—	200	—	°C/W
		SOT353 (Note 4)	—	337	—	°C/W
θ_{JC}	Thermal Resistance Junction-to-Case	SOT25 (Note 4)	—	52	—	°C/W
		SOT353 (Note 4)	—	121	—	°C/W

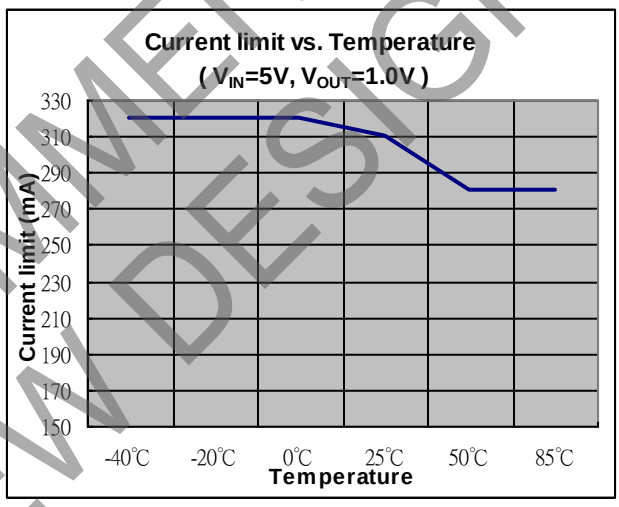
Note: 4. Test condition for SOT25 and SOT353: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

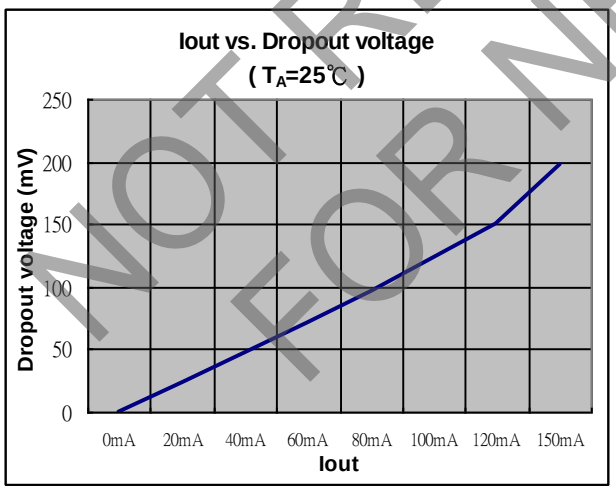
Typical Operating Characteristics

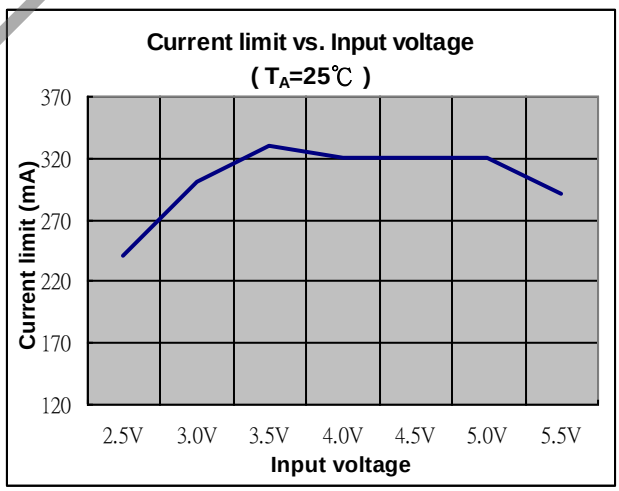




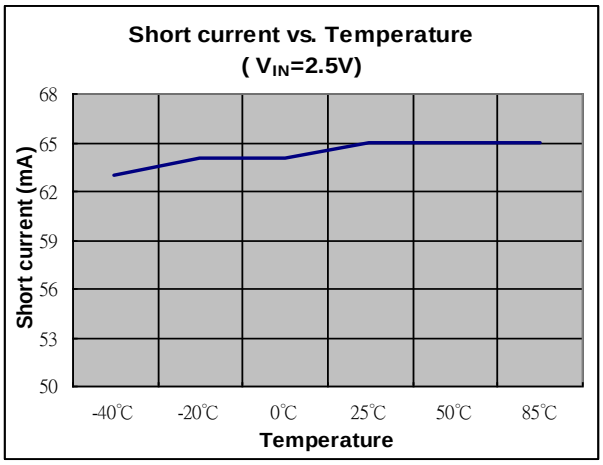


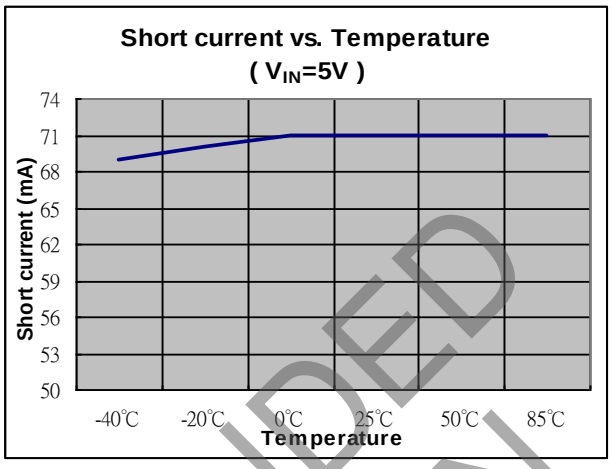


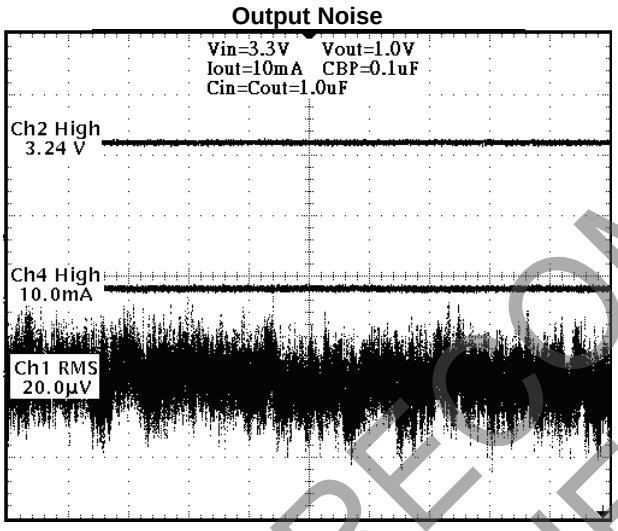


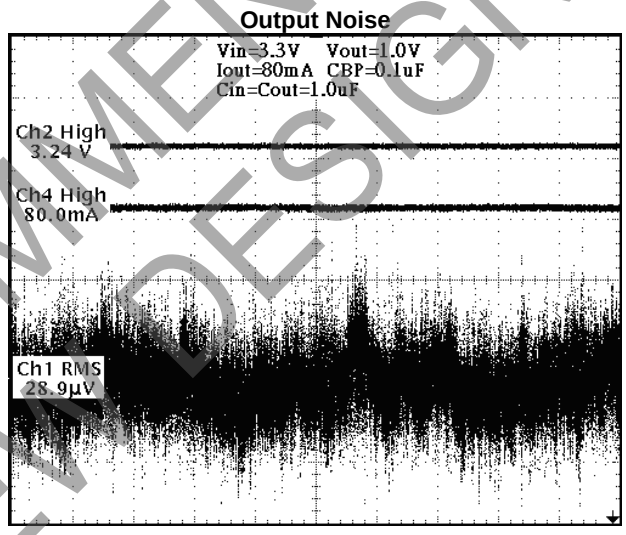


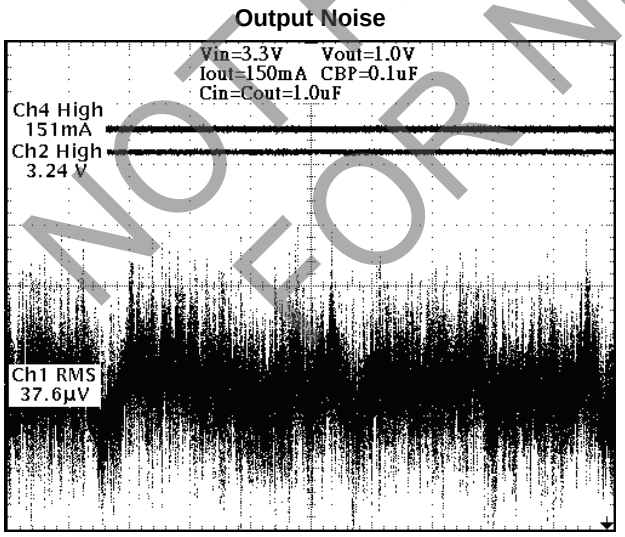
Typical Operating Characteristics (Cont.)





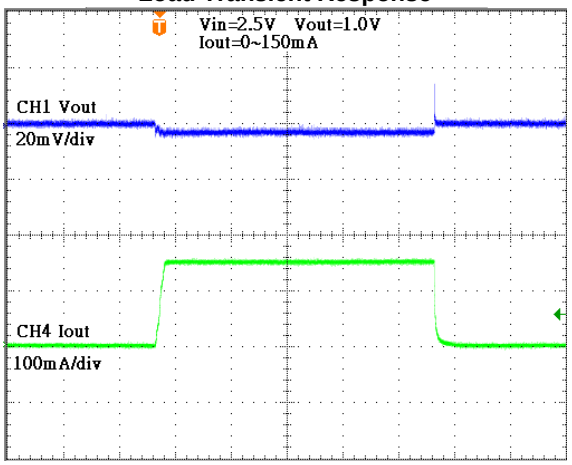




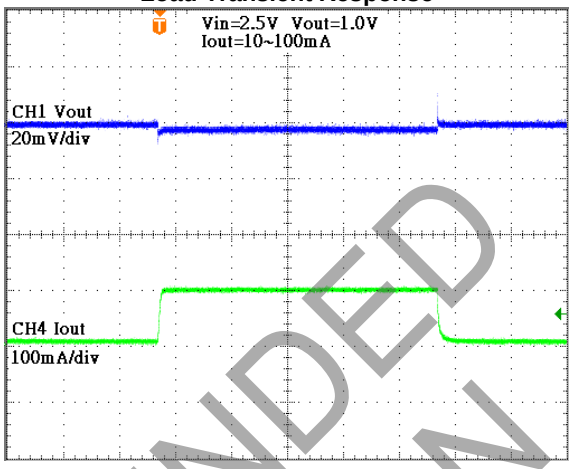


Typical Operating Characteristics (Cont.)

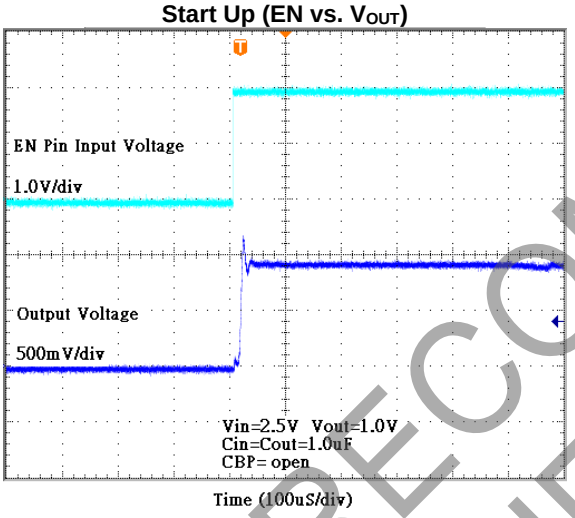
Load Transient Response



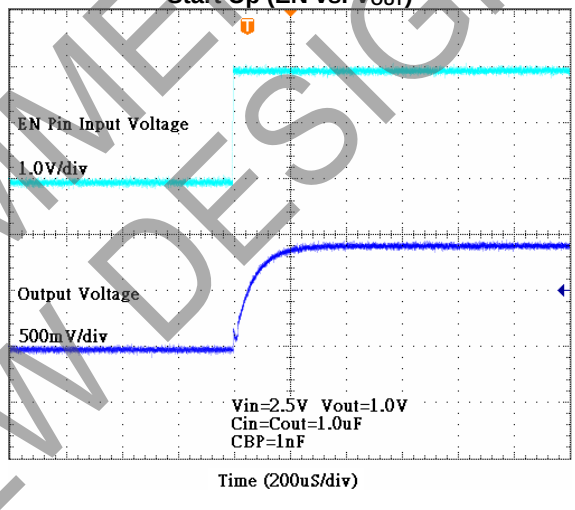
Load Transient Response



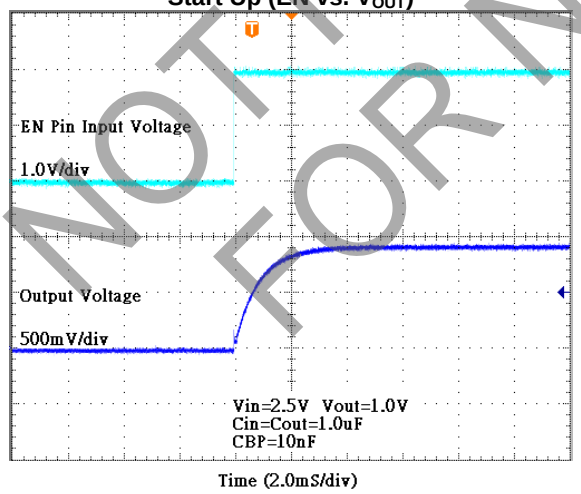
Start Up (EN vs. V_{OUT})



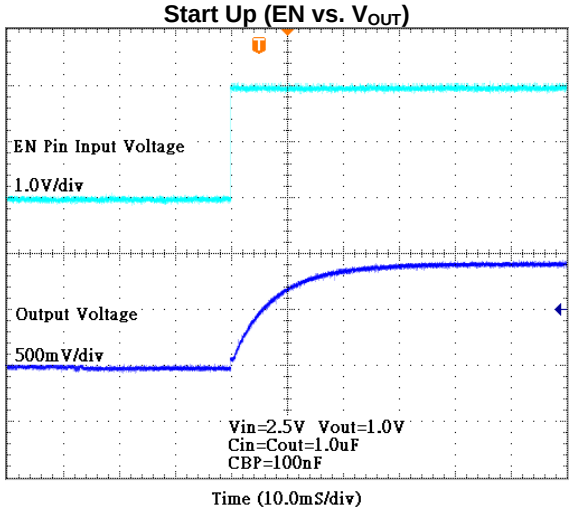
Start Up (EN vs. V_{OUT})



Start Up (EN vs. V_{OUT})



Start Up (EN vs. V_{OUT})



Application Note

Input Capacitor

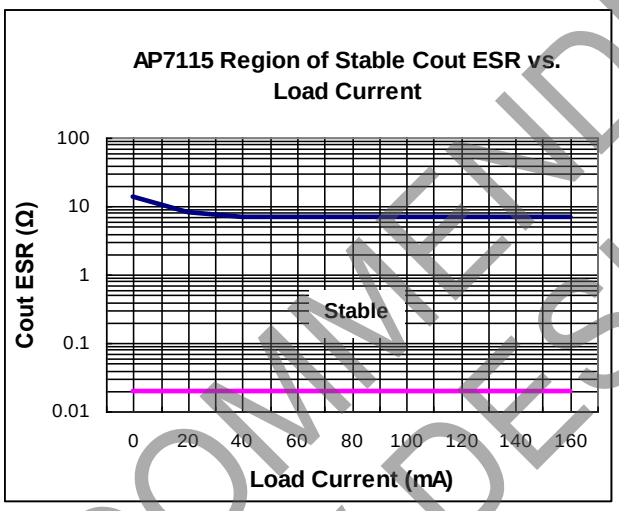
A 1µF input capacitor is required between the AP7115 input pin and GND.

There are no requirements for the ESR on input capacitor, but tolerance and temperature coefficient must be considered.

Output Capacitor

The AP7115 can work with very small ceramic output capacitors (1µF or greater). Higher capacitance values help to improve transient. The output capacitor's ESR is critical because it from a zero to provide phase lead which is required for loop stability.

Figure below is Cout ESR vs. Load Current.



Band-Gap Bypass Capacitor

0.1µF bypass capacitor Between BP pin and GND can reduce output voltage noise.

Shutdown Input Operation

The AP7115 is shutdown by pulling the EN pin low, and turned on by driving the input high. If the shutdown feature is not required, the EN pin should be tied to VIN to keep the regulator on at all time.

Dropout Voltage

$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$

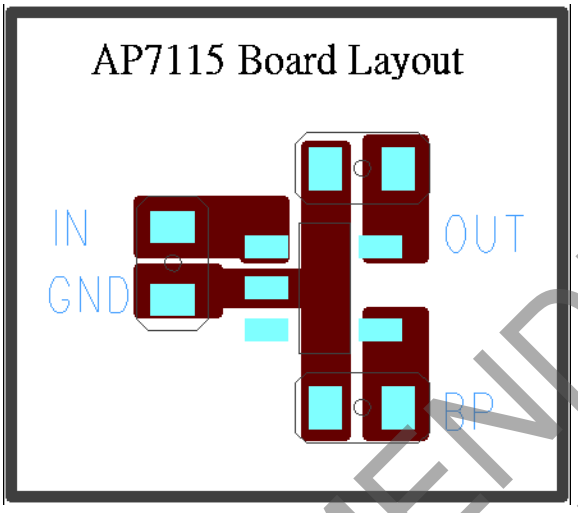
Current Limit

The AP7115 monitors and controls the PMOS' gate voltage, limiting the output current to 250mA (typ.). The output can be shorted to ground for an indefinite period of time without damaging the part.

Application Note (Cont.)

PCB Layout

Optimum performance can only be achieved when the device is mounted on a PC board according to the diagram below:



Thermal Considerations

Thermal Shutdown Protection limits power dissipation in AP7115. When the operation junction temperature exceeds +155°C, the Over Temperature Protection circuit starts the thermal shutdown function and turns the pass element off. The pass element turns on again after the junction temperature cools by +30°C. For continuous operation, do not exceed absolute maximum operation junction temperature +125°C. The power dissipation definition in device is:

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature +125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

Ordering Information

AP7115 - XX XX G - 7

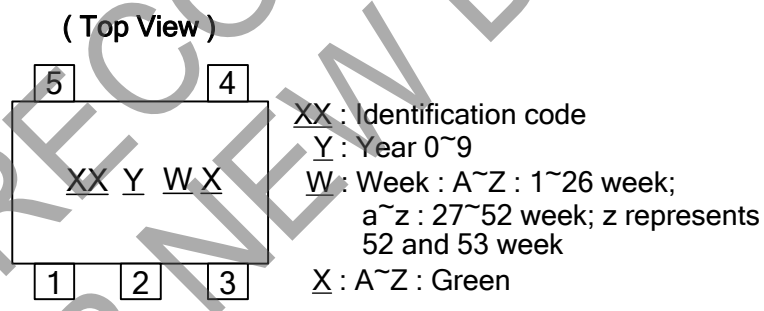
Output Voltage	Package	Green	Packing
10 : 1.0V 12 : 1.2V 15 : 1.5V 18 : 1.8V 25 : 2.5V 28 : 2.8V 29 : 2.9V 30 : 3.0V 33 : 3.3V 35 : 3.5V	W : SOT25 SE : SOT353	G : Green	7 : Tape & Reel

Part Number	Package Code	Packaging (Note 5)	7" Tape and Reel	
			Quantity	Part Number Suffix
AP7115-XXWG-7	W	SOT25	3000/Tape & Reel	-7
AP7115-XXSEG-7	SE	SOT353	3000/Tape & Reel	-7

Notes: 5. Pad layout as shown in Diodes Incorporated's package outline PDFs, which can be found on our website at http://www.diodes.com/package-outlines.html.

Marking Information

SOT25/SOT353

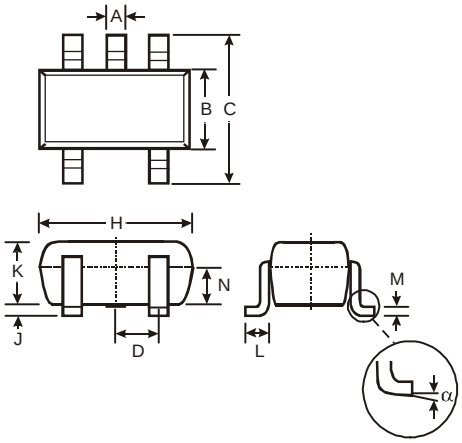


Part Number SOT25	Identification Code	Part Number SOT353	Identification Code
AP7115-10WG-7	FO	AP7115-10SEG-7	GO
AP7115-12WG-7	FP	AP7115-12SEG-7	GP
AP7115-15WG-7	FQ	AP7115-15SEG-7	GQ
AP7115-18WG-7	FR	AP7115-18SEG-7	GR
AP7115-25WG-7	FS	AP7115-25SEG-7	GS
AP7115-28WG-7	FT	AP7115-28SEG-7	GT
AP7115-29WG-7	FU	AP7115-29SEG-7	GU
AP7115-30WG-7	FV	AP7115-30SEG-7	GV
AP7115-33WG-7	FW	AP7115-33SEG-7	GW
AP7115-35WG-7	FX	AP7115-35SEG-7	GX

Package Outline Dimensions

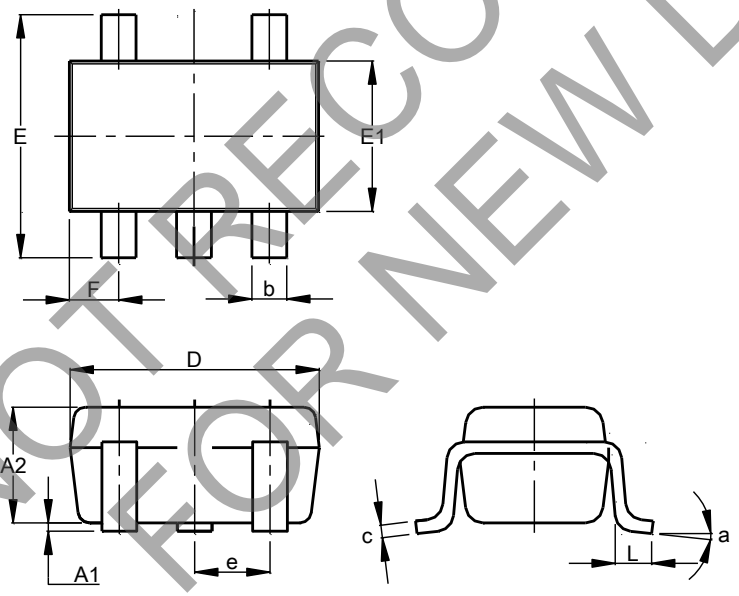
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: SOT25



SOT25			
Dim	**Min**	**Max**	**Typ**
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	-	-	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
N	0.70	0.80	0.75
α	0°	8°	-
All Dimensions in mm			

(2) Package Type: SOT353

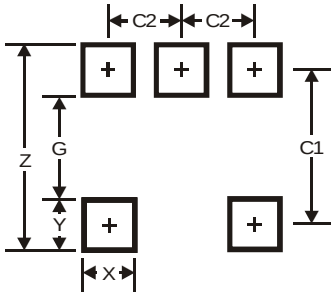


SOT353			
Dim	**Min**	**Max**	**Typ**
A1	0.00	0.10	0.05
A2	0.90	1.00	1.00
b	0.10	0.30	0.25
c	0.10	0.22	0.11
D	1.80	2.20	2.15
E	2.00	2.20	2.10
E1	1.15	1.35	1.30
e	0.650 BSC		
F	0.40	0.45	0.425
L	0.25	0.40	0.30
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

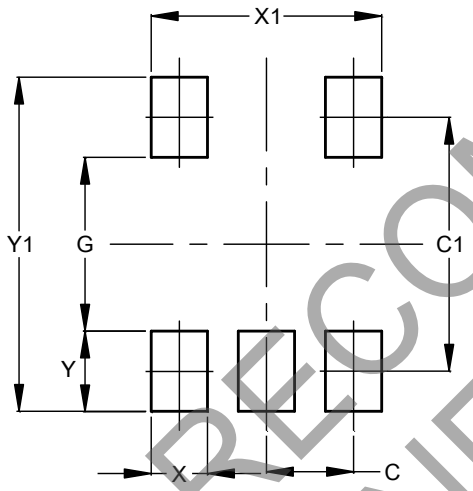
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: SOT25



Dimensions	Value
Z	3.20
G	1.60
X	0.55
Y	0.80
C1	2.40
C2	0.95

(2) Package Type: SOT353



Dimensions	Value (in mm)
C	0.650
C1	1.900
G	1.300
X	0.420
X1	1.720
Y	0.600
Y1	2.500

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