TABLE OF CONTENTS

REVISION HISTORY

12/11—Rev. B to Rev. C

Deleted Endnote 1 from Leakage Currents Parameter, Table 1 . 3
Deleted Endnote 1 from Leakage Currents Parameter, Table 2 . 4

10/09—Rev. A to Rev. B

Updated Format ... Universal
Added Pb-Free Information to Table 3 ... 5
Added Table 4 ... 6
Updated Outline Dimensions ... 12
Changes to Ordering Guide ... 12

7/02—Rev. 0 to Rev. A.

Changes to Features ... 1
Additions to Product Highlights ... 1
Changes to Specifications ... 2
Edits to Absolute Maximum Ratings ... 4
Changes to Terminology ... 4
Edits to Ordering Guide ... 4
Added new TPCs 4 and 5 ... 5
Added TPC 10 ... 6
Test Circuits 6, 7, and 8 replaced ... 7
Updated KS-6 Package Drawing ... 9

1/01—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5 V ± 10% and GND = 0 V; T_A = −40°C to +125°C unless otherwise stated.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	2.5			Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA;
	5	6	7	Ω max	see Figure 13
On Resistance Match Between Channels (ΔR_{ON})		0.1		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		0.8	0.8	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.75			Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		1.2	1.5	Ω max	
LEAKAGE CURRENTS					V_{DD} = 5.5 V
Source Off Leakage I_S (Off)	±0.01			nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V;
	±0.25	±0.35	1	nA max	see Figure 14
Channel On Leakage I_D, I_S (On)	±0.01			nA typ	V_S = V_D = 1 V or V_S = V_D = 4.5 V;
	±0.25	±0.35	5	nA max	see Figure 15
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	7			ns typ	R_L = 300 Ω, C_L = 35 pF
			12	ns max	V_S = 3 V; see Figure 16
t_{OFF}	3			ns typ	R_L = 300 Ω, C_L = 35 pF
			6	ns max	V_S = 3 V; see Figure 16
Break-Before-Make Time Delay, t_D	8			ns typ	R_L = 300 Ω, C_L = 35 pF,
			1	ns min	V_{S1} = V_{S2} = 3 V; see Figure 17
Off Isolation	−67			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−87			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 18
Channel-to-Channel Crosstalk	−62			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−82			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 19
Bandwidth −3 dB	200			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 20
C_S (Off)	7			pF typ	
C_D, C_S (On)	27			pF typ	
POWER REQUIREMENTS					V_{DD} = 5.5 V
					Digital inputs = 0 V or 5.5 V
I_{DD}	0.001			μA typ	
			1.0	μA max	

[1] Guaranteed by design, not subject to production test.

V_{DD} = 3 V ± 10% and GND = 0 V; T_A= −40°C to +125°C unless otherwise stated

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	6	7		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA;
		10	12	Ω max	see Figure 13
On Resistance Match Between Channels (ΔR_{ON})		0.1		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		0.8	0.8	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)		2.5		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
LEAKAGE CURRENTS					V_{DD} = 3.3 V
Source Off Leakage IS (Off)	±0.01			nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.25	±0.35	1	nA max	see Figure 14
Channel On Leakage I_D, I_S (On)	±0.01			nA typ	V_S = V_D = 1 V or V_S = V_D = 3 V;
	±0.25	±0.35	5	nA max	see Figure 15
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2.0		V min	
Input Low Voltage, V_{INL}		0.8		V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	10			ns typ	R_L = 300 Ω, C_L = 35 pF
			15	ns max	V_S = 2 V; see Figure 16
t_{OFF}	4			ns typ	R_L = 300 Ω, C_L = 35 pF
			8	ns max	V_S = 2 V; see Figure 16
Break-Before-Make Time Delay, t_D	8			ns typ	R_L = 300 Ω, C_L = 35 pF
			1	ns min	V_{S1} = V_{S2} = 2 V; see Figure 17
Off Isolation	−67			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−87			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 18
Channel-to-Channel Crosstalk	−62			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−82			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 19
Bandwidth −3 dB	200			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 20
C_S (Off)	7			pF typ	
C_D, C_S (On)	27			pF typ	
POWER REQUIREMENTS					V_{DD} = 3.3 V
					Digital inputs = 0 V or 3.3 V
I_{DD}	0.001			μA typ	
			1.0	μA max	

[1] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 3.

Parameter	Ratings
V_{DD} to GND	−0.3 V to +7 V
Analog, Digital Input[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	30 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SC70 Package, Power Dissipation	315 mW
θ_{JA} Thermal Impedance	332°C/W
θ_{JC} Thermal Impedance	120°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Pb-free Reflow Soldering	
Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	10 sec to 40 sec

[1] Overvoltage at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

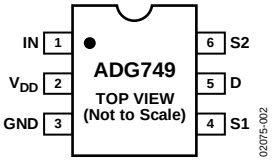

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	IN	Digital control input pin.
2	V_{DD}	Most positive power supply pin.
3	GND	Ground (0 V) reference pin.
4	S1	Source terminal of the multiplexer. Can be used as input or output.
5	D	Drain terminal of the multiplexer. Can be used as input or output.
6	S2	Source terminal of the multiplexer. Can be used as input or output.

Table 5. Truth Table

ADG749 IN	Switch S1	Switch S2
0	ON	OFF
1	OFF	ON

TERMINOLOGY

R_{ON}
Ohmic resistance between D and S.

ΔR_{ON}
On resistance match between any two channels, such as: R_{ON} max − R_{ON} min.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (Off)
Source leakage current with the switch off.

I_D, I_S (On)
Channel leakage current with the switch on.

V_D (V_S)
Analog voltage on Terminals D and S.

C_S (Off)
Off switch source capacitance.

C_D, C_S (On)
On switch capacitance.

Insertion Loss
Loss due to on resistance of the switch.

t_{ON}
Delay between applying the digital control input and the output switching on.

t_{OFF}
Delay between applying the digital control input and the output switching off.

t_D
Off time or on time measured between the 90% points of both switches, when switching from one address state to another.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Bandwidth
The frequency at which the output is attenuated by −3 dBs.

On Response
The frequency response of the on switch.

TYPICAL PERFORMANCE CHARACTERISTICS

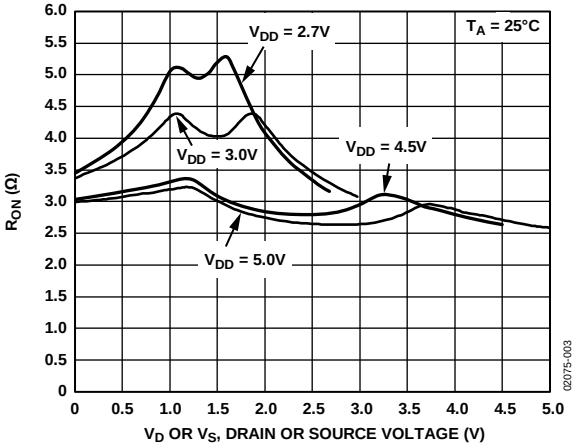

Figure 3. On Resistance vs. V_D (V_S) Single Supplies

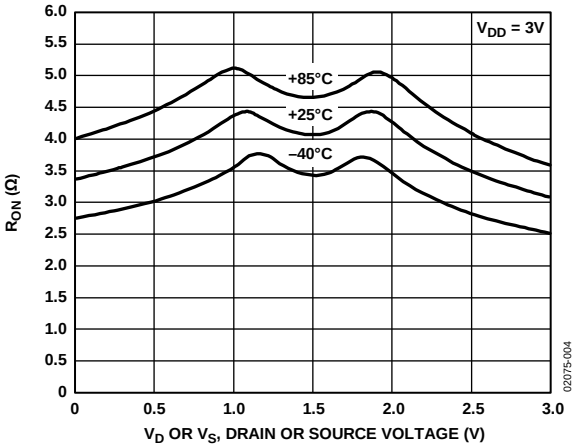

Figure 4. On Resistance vs. V_D (V_S) for Different Temperature, V_{DD} = 3 V

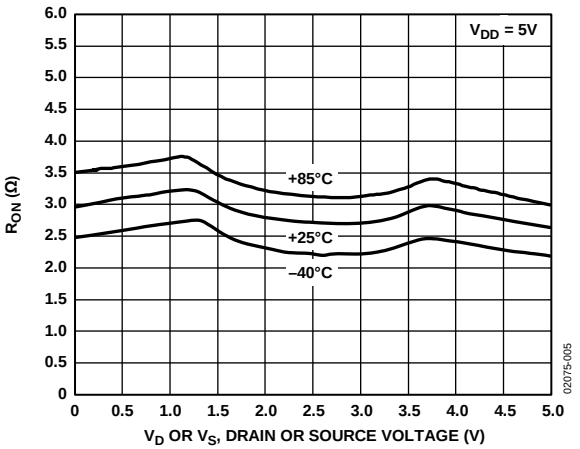

Figure 5. On Resistance vs. V_D (V_S) for Different Temperatures, V_{DD} = 5 V

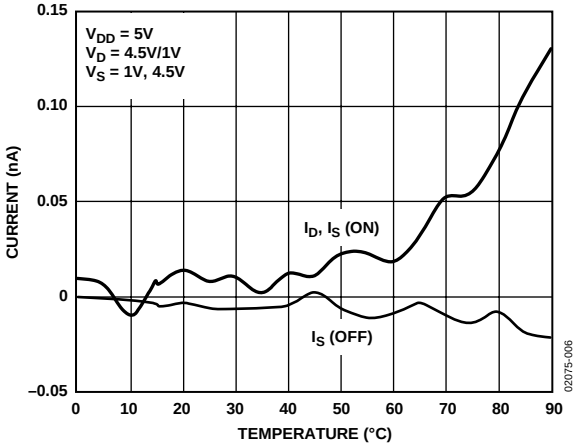

Figure 6. Leakage Currents vs. Temperature

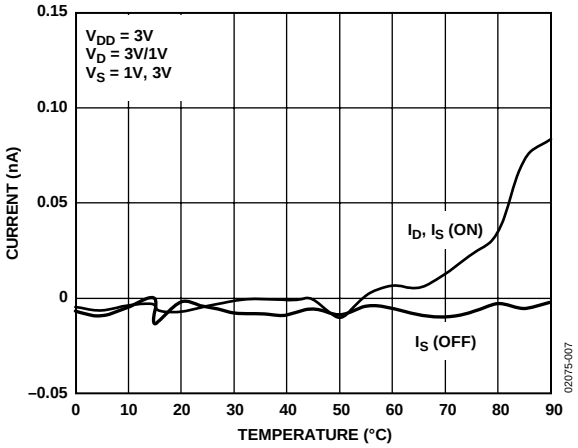

Figure 7. Leakage Currents vs. Temperature

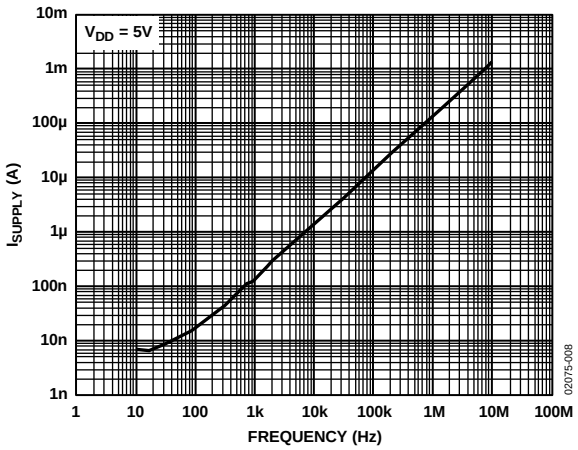

Figure 8. Supply Current vs. Input Switching Frequency

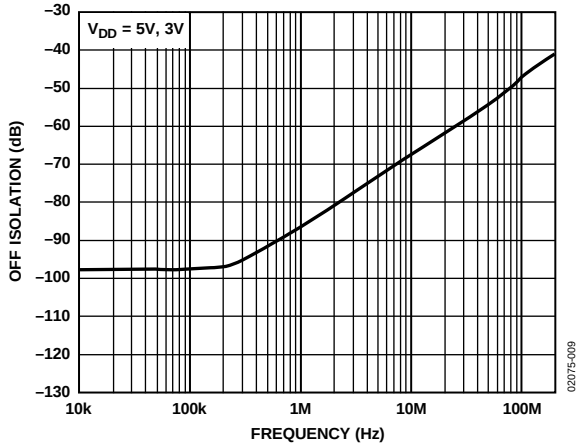

Figure 9. Off Isolation vs. Frequency

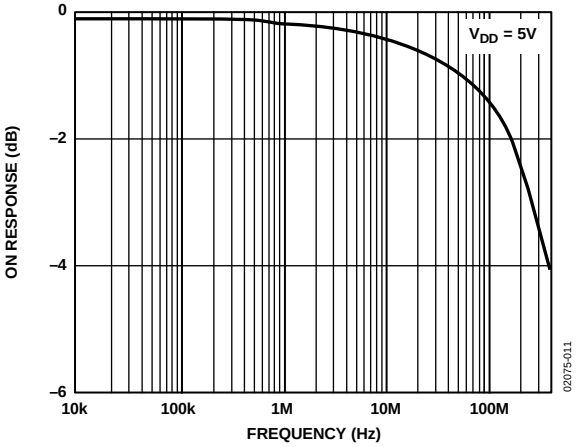

Figure 11. On Response vs. Frequency

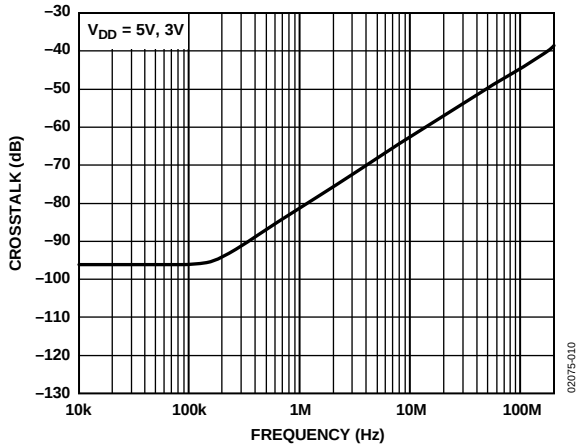

Figure 10. Crosstalk vs. Frequency

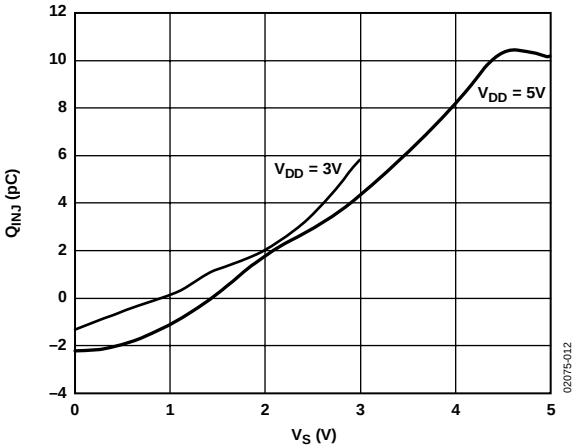

Figure 12. Charge Injection vs. Source Voltage

TEST CIRCUITS

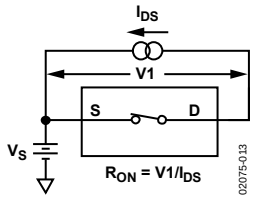

Figure 13. On Resistance

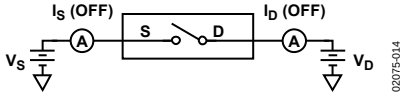

Figure 14. Off Leakage

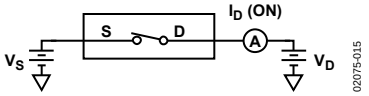

Figure 15. On Leakage

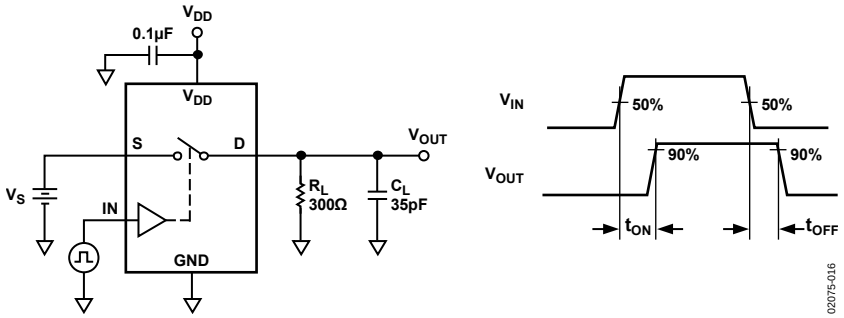

Figure 16. Switching Times

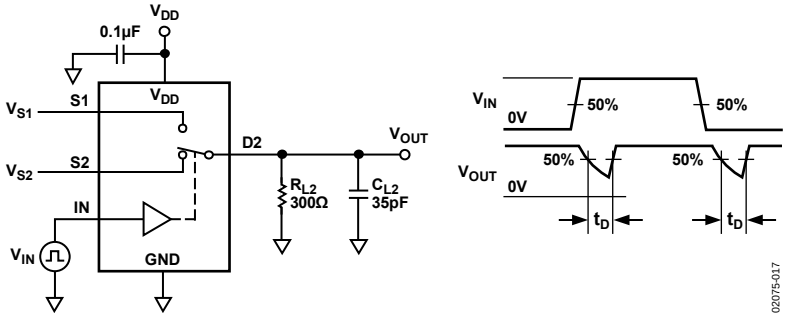

Figure 17. Break-Before-Make Time Delay, t_D

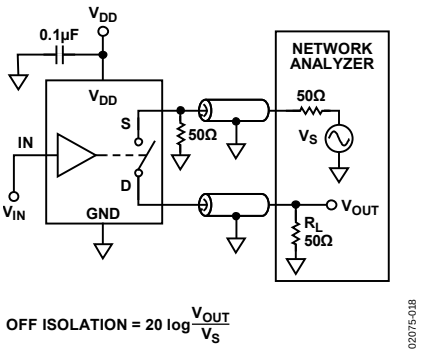

Figure 18. Off Isolation

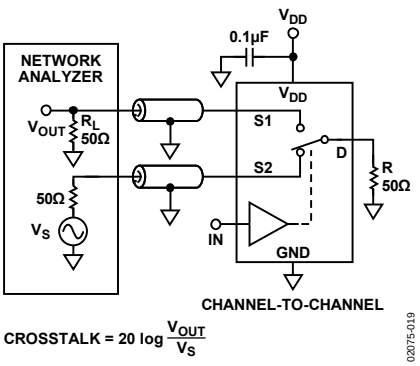

Figure 19. Channel-to-Channel Crosstalk

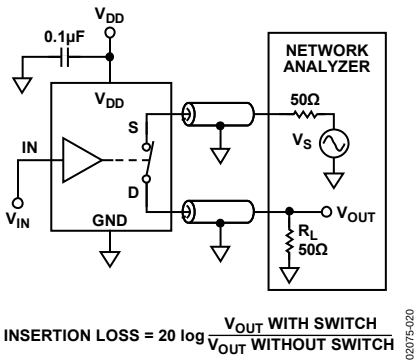

Figure 20. Bandwidth

APPLICATIONS INFORMATION

The ADG749 belongs to Analog Devices' new family of CMOS switches. This series of general-purpose switches has improved switching times, offering lower on resistance, higher bandwidths, low power consumption, and low leakage currents.

ADG749 SUPPLY VOLTAGES

Functionality of the ADG749 extends from 1.8 V to 5.5 V single supply, which makes it ideal for battery-powered instruments, where power efficiency and performance are important design parameters.

It is important to note that the supply voltage affects the input signal range, the on resistance, and the switching times of the part. By taking a look at the typical performance characteristics and the specifications, the effects of the power supplies can be clearly seen.

For V_{DD} = 1.8 V operation, R_{ON} is typically 40 Ω over the temperature range.

ON RESPONSE VS. FREQUENCY

Figure 21 illustrates the parasitic components that affect the ac performance of CMOS switches (the switch is shown surrounded by a box). Additional external capacitances will further degrade some performance. These capacitances affect feedthrough, crosstalk, and system bandwidth.

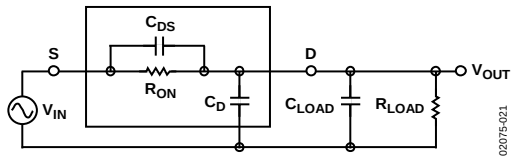

Figure 21. Switch Represented by Equivalent Parasitic Components

The transfer function that describes the equivalent diagram of the switch (Figure 21) is of the form *A(s)* shown below.

$$A(s) = R_T\left[\frac{s(R_{ON}\ C_{DS})+1}{s(R_T\ R_{ON}\ C_{DS})+1}\right]$$

where:

$R_T = R_{LOAD}/(R_{LOAD} + R_{ON})$

$C_T = C_{LOAD} + C_D + C_{DS}$

The signal transfer characteristic is dependent on the switch channel capacitance, C_{DS}. This capacitance creates a frequency zero in the numerator of the transfer function *A(s)*. Because the switch on resistance is small, this zero usually occurs at high frequencies. The bandwidth is a function of the switch output capacitance combined with C_{DS} and the load capacitance. The frequency pole corresponding to these capacitances appears in the denominator of *A(s)*.

The dominant effect of the output capacitance, C_D, causes the pole breakpoint frequency to occur first. Therefore, in order to maximize bandwidth, a switch must have a low input and output capacitance and low on resistance. The on response vs. frequency plot for the ADG749 is shown in Figure 11.

OFF ISOLATION

Off isolation is a measure of the input signal coupled through an off switch to the switch output. The capacitance, C_{DS}, couples the input signal to the output load when the switch is off, as shown in Figure 22.

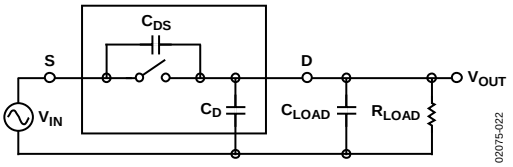

Figure 22. Off Isolation is Affected by External Load Resistance and Capacitance

The larger the value of CDS, the larger the values of feedthrough that will be produced. The typical performance characteristic graph of Figure 9 illustrates the drop in off isolation as a function of frequency. From dc to roughly 200 kHz, the switch shows better than −95 dB isolation. Up to frequencies of 10 MHz, the off isolation remains better than −67 dB. As the frequency increases, more and more of the input signal is coupled through to the output. Off isolation can be maximized by choosing a switch with the smallest C_{DS} possible. The values of load resistance and capacitance also affect off isolation, since they contribute to the coefficients of the poles and zeros in the transfer function of the switch when open.

$$A(s) = \left[\frac{s(R_{LOAD}\ C_{DS})}{s(R_{LOAD})(C_{LOAD} + C_D + C_{DS})+1}\right]$$

OUTLINE DIMENSIONS

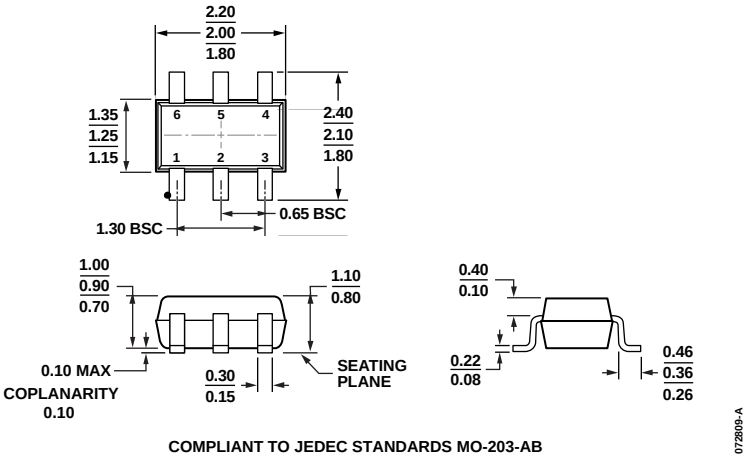

Figure 23. 6-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature range	Package Description	Package Option	Branding[2]
ADG749BKSZ-R2	−40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	S1M
ADG749BKSZ-REEL	−40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	S1M
ADG749BKSZ-REEL7	−40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	S1M

[1] Z= RoHS Compliant Part.
[2] Branding on this package is limited to three characters due to space constraints.

D02075-0-12/11(C)