

ADG528A—SPECIFICATIONS

DUAL SUPPLY ($V_{DD} = +10.8\text{ V}$ to $+16.5\text{ V}$, $V_{SS} = -10.8\text{ V}$ to -16.5 V , unless otherwise noted.)

	ADG528A ADG529A K Version −40°C to		ADG528A ADG529A B Version −40°C to		ADG528A ADG529A T Version −55°C to			
Parameter	+25°C	+85°C	+25°C	+85°C	+25°C	+125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V min	
R _{ON}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V max	
	280		280		280		Ω typ	−10 V ≤ V _S ≤ +10 V, I _{DS} = 1 mA; Test Circuit 1
	450	600	450	600	450	600	Ω max	
	300	400	300	400	300	400	Ω max	V _{DD} = 15 V (±10%), V _{SS} = −15 V (±10%)
R _{ON} Drift	0.6		0.6		0.6		Ω max	V _{DD} = 15 V (±5%), V _{SS} = −15 V (±5%)
R _{ON} Match	5		5		5		%/°C typ	−10 V ≤ V _S ≤ +10 V, I _{DS} = 1 mA
I _S (OFF), Off Input Leakage	0.02		0.02		0.02		% typ	−10 V ≤ V _S ≤ +10 V, I _{DS} = 1 mA
	1	50	1	50	1	50	nA typ	V1 = ±10 V, V2 = ∓10 V; Test Circuit 2
I _D (OFF), Off Input Leakage	0.04		0.04		0.04		nA max	
ADG528A	1	100	1	100	1	100	nA typ	V1 = ±10 V, V2 = ∓10 V; Test Circuit 3
ADG529A	1	50	1	50	1	50	nA max	
I _D (ON), On Channel Leakage	0.04		0.04		0.04		nA max	
ADG528A	1	100	1	100	1	100	nA typ	V1 = ±10 V, V2 = ∓10 V; Test Circuit 4
ADG529A	1	50	1	50	1	50	nA max	
I _{DIFF} , Differential Off Output Leakage (ADG529A only)		25		25		25	nA max	V1 = ±10 V, V2 = ∓10 V; Test Circuit 5
DIGITAL CONTROL								
V _{INH} , Input High Voltage		2.4		2.4		2.4	V min	
V _{INL} , Input Low Voltage		0.8		0.8		0.8	V max	
I _{INL} or I _{INH}		1		1		1	μA max	V _{IN} = 0 to V _{DD}
C _{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS ¹								
t _{TRANSITION}	200		200		200		ns typ	V1 = ±10 V, V2 = ∓10 V; Test Circuit 6
	300	400	300	400	300	400	ns max	
t _{OPEN}	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t _{ON} (EN, $\overline{WR}$)	200		200		200		ns typ	Test Circuits 8 and 9
	300	400	300	400	300	400	ns max	
t _{OFF} (EN, $\overline{RS}$)	200		200		200		ns typ	Test Circuits 8 and 10
	300	400	300	400	300	400	ns max	
t _W Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 1
t _S Address, Enable Setup Time		100		100		100	ns min	See Figure 1
t _H , Address, Enable Hold Time		10		10		10	ns min	See Figure 1
t _{RS} Reset Pulse Width		100		100		100	ns min	See Figure 2
OFF Isolation	68		68		68		dB typ	V _{EN} = 0.8 V, R _L = 1 kΩ, C _L = 15 pF,
	50		50		50		dB min	V _S = 7 V rms, f = 100 kHz
C _S (OFF)	5		5		5		pF typ	V _{EN} = 0.8 V
C _D (OFF)								
ADG528A	22		22		22		pF typ	V _{EN} = 0.8 V
ADG529A	11		11		11		pF typ	
Q _{INJ} , Charge Injection	4		4		4		pC typ	R _S = 0 Ω, V _S = 0 V; Test Circuit 11

Parameter	ADG528A ADG529A K Version –40°C to +25°C +85°C		ADG528A ADG529A B Version –40°C to +25°C +85°C		ADG528A ADG529A T Version –55°C to +25°C +125°C		Units	Comments
POWER SUPPLY								
I _{DD}	0.6		0.6		0.6		mA typ	V _{IN} = V _{INL} or V _{INH}
		1.5		1.5		1.5	mA max	
I _{SS}	20		20		20		μA typ	V _{IN} = V _{INL} or V _{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		2.8		2.8		2.8	mW max	

NOTE

¹Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

SINGLE SUPPLY (V_{DD} = +10.8 V to +16.5 V, V_{SS} = GND = 0 V, unless otherwise noted.)

Parameter	ADG528A ADG529A K Version –40°C to +25°C +85°C		ADG528A ADG529A B Version –40°C to +25°C +85°C		ADG528A ADG529A T Version –55°C to +25°C +125°C		Units	Comments
ANALOG SWITCH								
Analog Signal Range	GND	GND	GND	GND	GND	GND	V min V max	
	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}		
R _{ON}	500		500		500		Ω typ	GND ≤ V _S ≤ +10 V, I _{DS} = 0.5 mA; Test Circuit 1
	700	1000	700	1000	700	1000	Ω max	
R _{ON} Drift	0.6		0.6		0.6		%/°C typ	GND ≤ V _S ≤ +10 V, I _{DS} = 0.5 mA
R _{ON} Match	5		5		5		% typ	GND ≤ V _S ≤ +10 V, I _{DS} = 0.5 mA
I _S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = +10 V/GND, V2 = GND/+10 V; Test Circuit 2
	1	50	1	50	1	50	nA max	
I _D (OFF), Off Input Leakage	0.04		0.04		0.04		nA typ	V1 = +10 V/GND, V2 = GND/+10 V; Test Circuit 3
ADG528A	1	100	1	100	1	100	nA max	
ADG529A	1	50	1	50	1	50	nA max	
I _D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = +10 V/GND, V2 = GND/+10 V; Test Circuit 4
ADG528A	1	100	1	100	1	100	nA max	
ADG529A	1	50	1	50	1	50	nA max	
I _{DIFF} , Differential Off Output Leakage (ADG529A only)		25		25		25	nA max	V1 = +10 V/GND, V2 = GND/+10 V; Test Circuit 5
DIGITAL CONTROL								
V _{INH} , Input High Voltage		2.4		2.4		2.4	V min	
V _{INL} , Input Low Voltage		0.8		0.8		0.8	V max	
I _{INL} or I _{INH}		1		1		1	μA max	V _{IN} = 0 to V _{DD}
C _{IN} , Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS ¹								
t _{TRANSITION}	300		300		300		ns typ	V1 = +10 V/GND, V2 = GND/+10 V; Test Circuit 6
	450	600	450	600	450	600	ns max	
t _{OPEN}	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t _{ON} (EN, $\overline{\text{WR}}$)	250		250		250		ns typ	Test Circuits 8 and 9
	450	600	450	600	450	600	ns max	
t _{OFF} (EN, $\overline{\text{RS}}$)	250		250		250		ns typ	Test Circuits 8 and 10
	450	600	450	600	450	600	ns max	
t _W Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 1

ADG528A

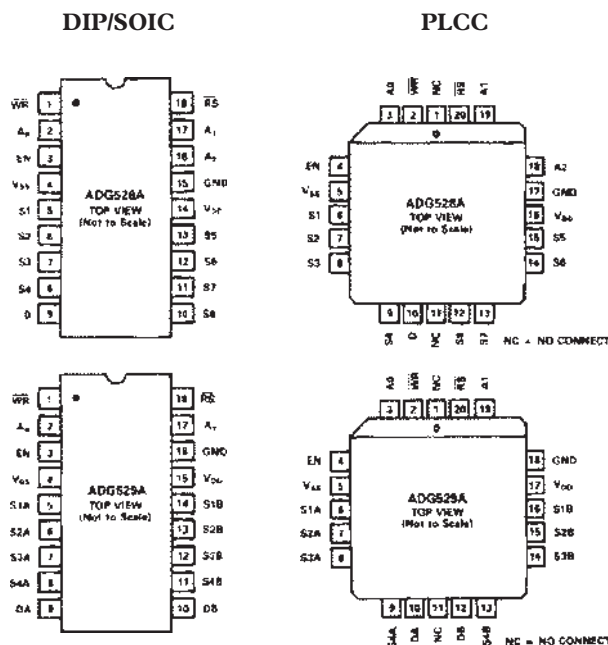
Parameter	ADG528A ADG529A K Version –40°C to +25°C +85°C	ADG528A ADG529A B Version –40°C to +25°C +85°C	ADG528A ADG529A T Version –55°C to +25°C +125°C	Units	Comments
DYNAMIC CHARACTERISTICS ¹ (Cont'd)					
t _S Address, Enable Setup Time	100	100	100	ns min	See Figure 1
t _H Address, Enable Hold Time	10	10	10	ns min	See Figure 1
t _{RS} Reset Pulse Width	100	100	100	ns min	See Figure 2
OFF Isolation	68	68	68	dB typ	V _{EN} = 0.8 V, R _L = 1 kΩ, C _L = 15 pF,
	50	50	50	dB min	V _S = 3.5 V rms, f = 100 kHz
C _S (OFF)	5	5	5	pF typ	V _{EN} = 0.8 V
C _D (OFF)					
ADG528A	22	22	22	pF typ	V _{EN} = 0.8 V
ADG529A	11	11	11	pF typ	
Q _{INJ} , Charge Injection	4	4	4	pC typ	R _S = 0 Ω, V _S = 0 V; Test Circuit 11
POWER SUPPLY					
I _{DD}	0.6	0.6	0.6	mA typ	V _{IN} = V _{INL} or V _{INH}
	1.5	1.5	1.5	mA max	
Power Dissipation	11	10	10	mW typ	
	25	25	25	mW max	

NOTE

¹Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS¹

($T_A = +25^\circ\text{C}$, unless otherwise noted)

V_{DD} to V_{SS} 44 V

V_{DD} to GND 25 V

V_{SS} to GND -25 V

Analog Inputs²

Voltage at S, D $V_{SS} - 2\text{ V}$ to $V_{DD} + 2\text{ V}$ or 20 mA, whichever Occurs First

Continuous Current, S or D 20 mA

Pulsed Current, S or D

1 ms duration, 10% Duty Cycle 40 mA

Digital Inputs¹

Voltage at A, EN, $\overline{WR}$, $\overline{RS}$ $V_{SS} - 4\text{ V}$ to $V_{DD} + 4\text{ V}$ or 20 mA, whichever Occurs First

Power Dissipation (Any Package)

Up to $+75^\circ\text{C}$ 470 mW

Derates above $+75^\circ\text{C}$ 6 mW/ $^\circ\text{C}$

Operating Temperature

Commercial (K Version) -40°C to $+85^\circ\text{C}$

Industrial (B Version) -40°C to $+85^\circ\text{C}$

Extended (T Version) -55°C to $+125^\circ\text{C}$

Storage Temperature Range -65°C to $+150^\circ\text{C}$

Lead Temperature (Soldering, 10 sec) $+300^\circ\text{C}$

NOTES

¹Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Overvoltage at A, EN, $\overline{WR}$, $\overline{RS}$, S or D will be clamped by diodes. Current should be limited to the maximum rating above.

ADG528A

TRUTH TABLES

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	X	$\overline{\text{L}}^{\text{H}}$	1	Retains Previous Switch Condition
X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

X = Don't Care

ADG528A

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	$\overline{\text{L}}^{\text{H}}$	1	Retains Previous Switch Condition
X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

X = Don't Care

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TIMING DIAGRAMS

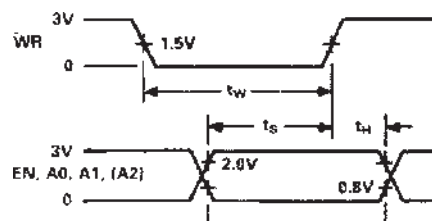


Figure 1.

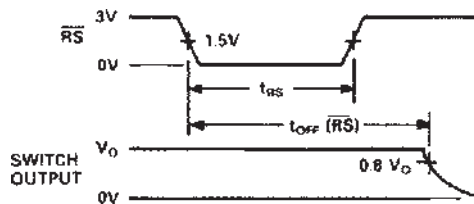


Figure 2.

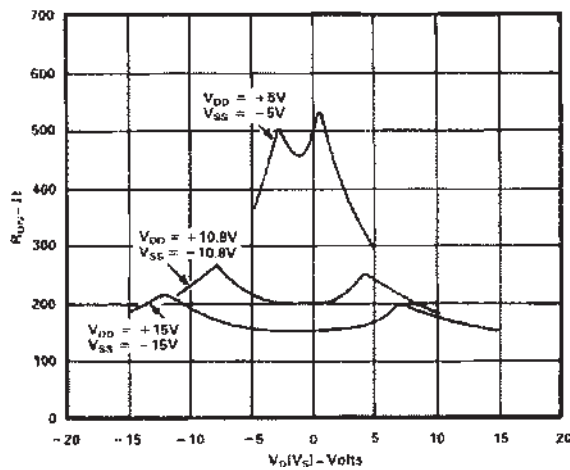
Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{WR}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{WR}$.

Figure 2 shows the Reset Pulse Width, t_{RS} , and Reset Turn-off Time, $t_{OFF}(\overline{RS})$.

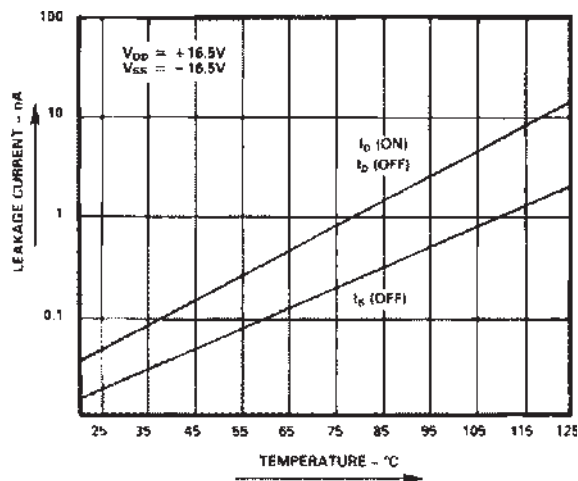
Note: All digital input signals rise and fall times measured from 10% to 90% of 3 V. $t_R = t_F = 20$ ns.

Typical Performance Characteristics—ADG528A

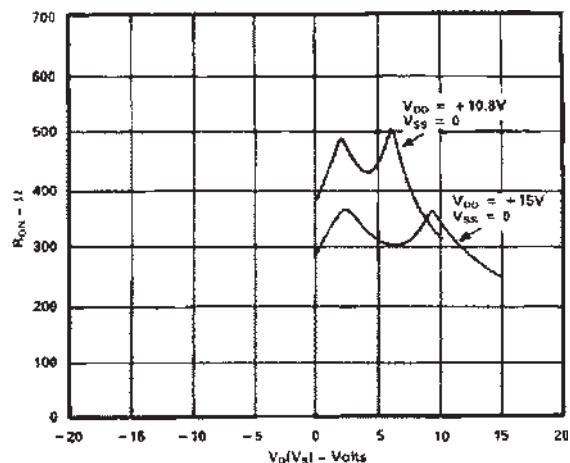
The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5 V.



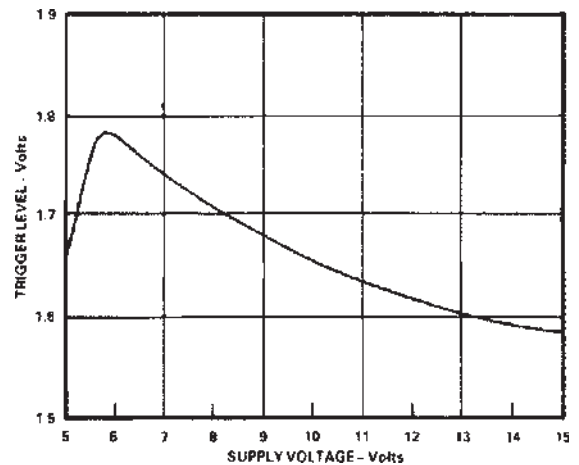
TPC 1. R_{ON} as a Function of $V_D(V_S)$: Dual Supply Voltage, $T_A = +25^\circ\text{C}$



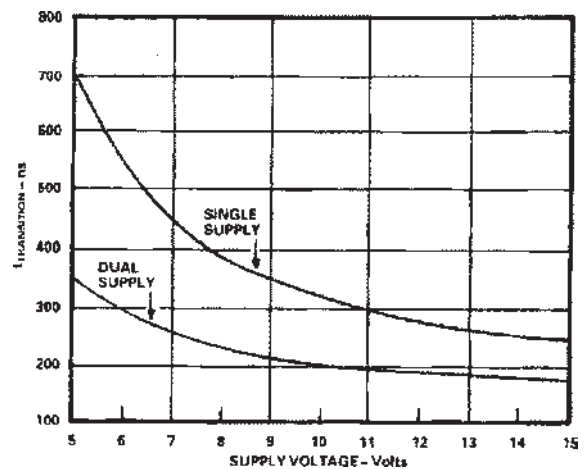
TPC 2. Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



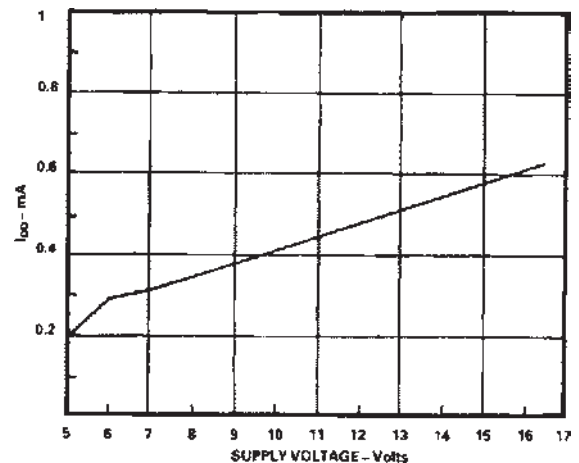
TPC 3. R_{ON} as a Function of $V_D(V_S)$: Single Supply Voltage, $T_A = +25^\circ\text{C}$



TPC 4. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, $T_A = +25^\circ\text{C}$



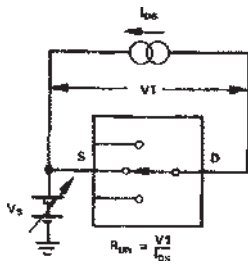
TPC 5. $t_{\text{TRANSITION}}$ vs. Supply Voltage: Dual and Single Supplies, $T_A = +25^\circ\text{C}$ (Note: For V_{DD} and $|V_{SS}| < 10\text{ V}$; $V_1 = V_{DD}/V_{SS}$, $V_2 = V_{SS}/V_{DD}$. See Test Circuit 6)



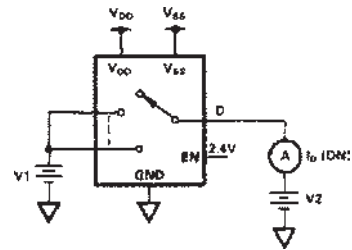
TPC 6. I_{DD} vs. Supply Voltage: Dual or Single Supply, $T_A = +25^\circ\text{C}$

ADG528A

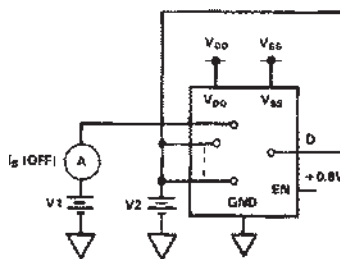
Test Circuits



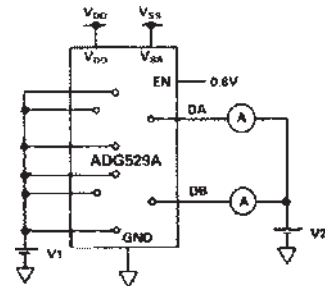
Test Circuit 1. R_{ON}



Test Circuit 4. I_D (ON)

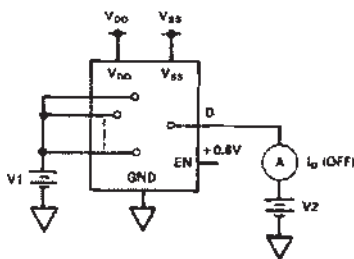


Test Circuit 2. I_S (OFF)

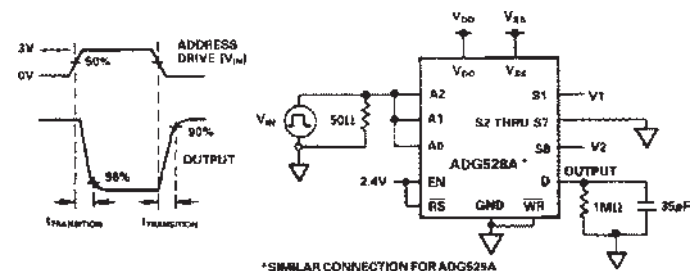


$$I_{DIFF} = I_{DA} (OFF) - I_{DB} (OFF)$$

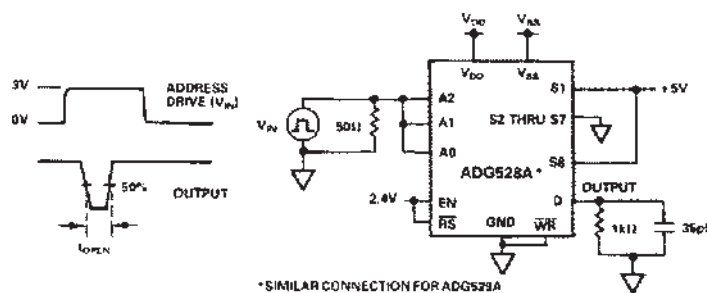
Test Circuit 5. I_{DIFF}



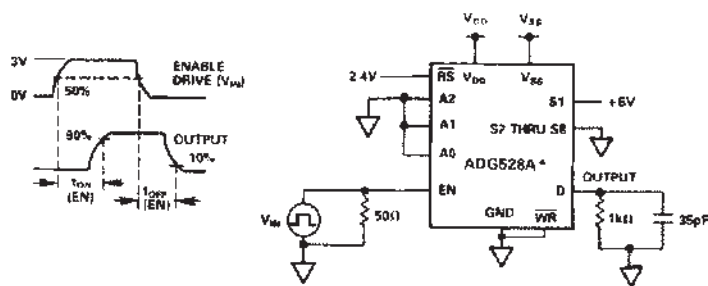
Test Circuit 3. I_D (OFF)



Test Circuit 6. Switching Time of Multiplexer, $t_{TRANSITION}$

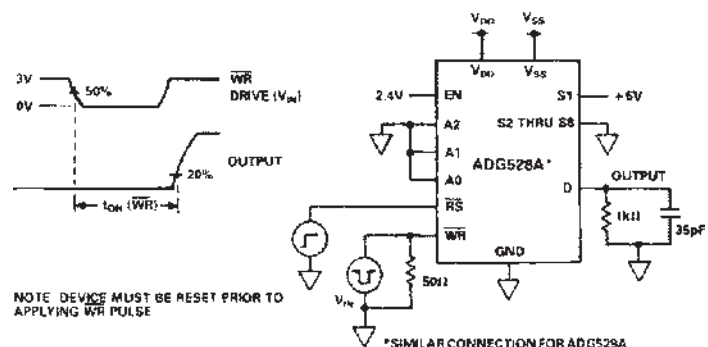


Test Circuit 7. Break-Before-Make Delay, t_{OPEN}



*SIMILAR CONNECTION FOR ADG528A

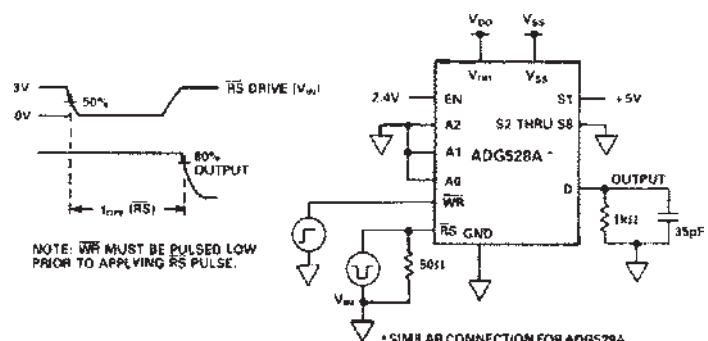
Test Circuit 8. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$



NOTE: DEVICE MUST BE RESET PRIOR TO APPLYING WR PULSE

*SIMILAR CONNECTION FOR ADG528A

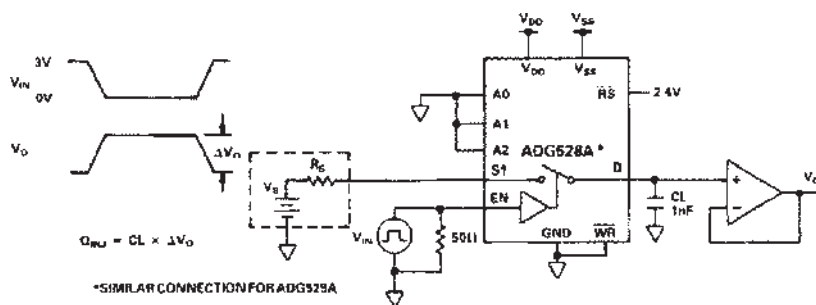
Test Circuit 9. Write Turn-On Time, $t_{ON}(\overline{WR})$



NOTE: WR MUST BE PULSED LOW PRIOR TO APPLYING RS PULSE.

*SIMILAR CONNECTION FOR ADG528A

Test Circuit 10. Reset Turn-Off Time, $t_{OFF}(\overline{RS})$



*SIMILAR CONNECTION FOR ADG528A

Test Circuit 11. Charge Injection

ADG528A

TERMINOLOGY

R_{ON}	Ohmic resistance between terminals D and S	$t_{OFF} (EN)$	Delay time between the 50% and 10% points of the digital input and switch “OFF” condition
$R_{ON} Match$	Difference between the R_{ON} of any two channels	$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and switch “ON” condition when switching from one address state to another.
$R_{ON} Drift$	Change in R_{ON} versus temperature	t_{OPEN}	“OFF” time measured between 50% points of both switches when switching from one address state to another
$I_S (OFF)$	Source terminal leakage current when the switch is off.	V_{INL}	Maximum input voltage for Logic “0”
$I_D (OFF)$	Drain terminal leakage current when the switch is off.	V_{INH}	Minimum input voltage for Logic “1”
$I_D (ON)$	Leakage current that flows from the closed switch into the body.	$I_{INL} (I_{INH})$	Input current of the digital input
$V_S (V_D)$	Analog voltage on terminal S or D	V_{DD}	Most positive voltage supply
$C_S (OFF)$	Channel input capacitance for “OFF” condition	V_{SS}	Most negative voltage supply
$C_D (OFF)$	Channel output capacitance for “OFF” condition	I_{DD}	Positive supply current
C_{IN}	Digital input capacitance	I_{SS}	Negative supply current
$t_{ON} (EN)$	Delay time between the 50% and 90% points of the digital input and switch “ON” condition.		

Technical drawings of the 18-pin connector showing dimensions in inches and millimeters.

Top View:

- Overall width: 0.920 (23.37)
- Width between pin centers: 0.900 (22.86)
- Width between mounting holes: 0.880 (22.35)
- Pin pitch: 0.100 (2.54) BSC
- Pin diameter: 0.210 (5.33) MAX
- Pin height: 0.150 (3.81)
- Pin base diameter: 0.130 (3.30)
- Pin base thickness: 0.115 (2.92)
- Pin base width: 0.022 (0.56)
- Pin base thickness: 0.018 (0.46)
- Pin base width: 0.014 (0.36)
- Pin base thickness: 0.070 (1.78)
- Pin base thickness: 0.060 (1.52)
- Pin base thickness: 0.045 (1.14)

Side View:

- Pin height: 0.280 (7.11)
- Pin base thickness: 0.250 (6.35)
- Pin base width: 0.240 (6.10)

Cross-sectional View:

- Pin height: 0.325 (8.26)
- Pin base thickness: 0.310 (7.87)
- Pin base width: 0.300 (7.62)
- Pin base thickness: 0.060 (1.52) MAX
- Pin base thickness: 0.015 (0.38) MIN
- Pin base thickness: 0.015 (0.38) GAUGE PLANE
- Pin base thickness: 0.015 (0.38) SEATING PLANE
- Pin base thickness: 0.005 (0.13) MIN
- Pin base thickness: 0.195 (4.95)
- Pin base thickness: 0.130 (3.30)
- Pin base thickness: 0.115 (2.92)
- Pin base thickness: 0.014 (0.36)
- Pin base thickness: 0.010 (0.25)
- Pin base thickness: 0.008 (0.20)
- Pin base thickness: 0.430 (10.92) MAX

• **COLE**

Dimensions Shown in inches and (millimeters)

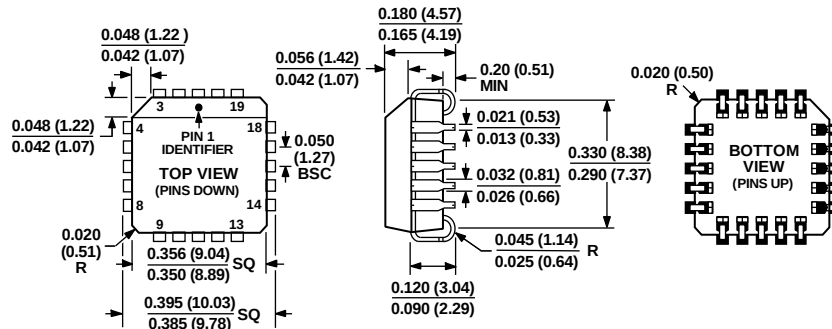
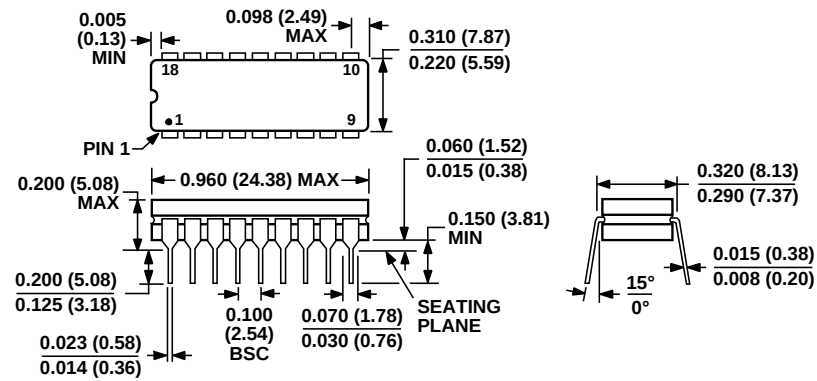


Figure 2. 20-Lead Plastic Leaded Chip Carrier [PLCC]
(P-20)

Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 3. 18-Lead Ceramic Dual In-Line Package [CERDIP] (Q-18)

Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG528AKN	–40°C to +85°C	18-Lead Plastic Dual In-Line Package [PDIP]	N–18
ADG528AKNZ	–40°C to +85°C	18-Lead Plastic Dual In-Line Package [PDIP]	N–18
ADG528AKP	–40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P–20
ADG528AKP-REEL	–40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P–20
ADG528AKPZ	–40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P–20
ADG528AKPZ-REEL	–40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P–20
ADG528ATQ	–55°C to +125°C	18-Lead Ceramic Dual In-Line Package [CERDIP]	Q–18
ADG528ABCHIPS	–55°C to +125°C	DIE	

¹ Z = RoHS Compliant Part.

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10/2004—Rev. A to Rev. B

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