## **TABLE OF CONTENTS**

Features	Absolute Maximum Ratings6
Applications1	ESD Caution6
Functional Block Diagram1	Pin Configurations and Function Descriptions7
General Description1	Typical Performance Characteristics8
Product Highlights1	Terminology12
Revision History2	Test Circuits
Specifications	Outline Dimensions
±15 V Dual Supply3	Ordering Guide
+12 V Single Supply4	Automotive Products
±5 V Dual Supply5	
REVISION HISTORY	
1/2020—Rev. C to Rev. D	3/2011—Rev. A to Rev. B
Change to Features Section	Changes to Features Section1
Changes to Leakage Currents Parameter, Table 1 3	Changes to Table 5, Added Exposed Pad Notation3
Changes to Leakage Currents Parameter, Table 2	Updated Outline Dimensions
Changes to Leakage Currents Parameter, Table 35	Changes to Ordering Guide40
Updated Outline Dimensions	Added Automotive Products Section40
3/2016—Rev. B to Rev. C	3/2009—Rev. 0 to Rev. A
Changed CP-16-13 to CP-16-26Throughout	Changes to Power Requirements, IDD, Digital Inputs = 5 V
Changes to Figure 2, Figure 3, and Table 5	Parameter, Table 13
Updated Outline Dimensions	Changes to Power Requirements, IDD, Digital Inputs = 5 V
Changes to Ordering Guide	Parameter Table 24

5/2008—Revision 0: Initial Version

## SPECIFICATIONS ±15 V DUAL SUPPLY

 $V_{\text{DD}}$  = 15 V  $\pm$  10%,  $V_{\text{SS}}$  = –15 V  $\pm$  10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance, R <sub>ON</sub>	1.5			Ωtyp	$V_S = \pm 10 \text{ V}, I_S = -10 \text{ mA}; \text{ see Figure 23}$
	1.8	2.3	2.6	Ω max	$V_{DD} = +13.5 \text{ V}, V_{SS} = -13.5 \text{ V}$
On-Resistance Match Between	0.1			Ωtyp	$V_S = \pm 10 \text{ V}$ , $I_S = -10 \text{ mA}$
Channels, ΔR <sub>ON</sub>				1	
	0.18	0.19	0.21	Ω max	
On-Resistance Flatness, RFLAT(ON)	0.3			Ωtyp	$V_S = \pm 10 \text{ V}, I_S = -10 \text{ mA}$
	0.36	0.4	0.45	Ω max	
LEAKAGE CURRENTS					$V_{DD} = +16.5 \text{ V}, V_{SS} = -16.5 \text{ V}$
Source Off Leakage, I <sub>s</sub> (Off)	±0.03			nA typ	$V_S = \pm 10 \text{ V}, V_D = \mp 10 \text{ V}$ ; see Figure 24
	±0.55	±2	±12.5	nA max	-
ADG1411WBCPZ-REEL Only	±3		±40	nA max	
Drain Off Leakage, I <sub>D</sub> (Off)	±0.03			nA typ	$V_S = \pm 10 \text{ V}, V_D = \mp 10 \text{ V}$ ; see Figure 24
	±0.55	±2	±12.5	nA max	13 = 10 1, 15   10 1, 300 1 1 guile 2 1
ADG1411WBCPZ-REEL Only	±3	<u></u>	±40	nA max	
Channel On Leakage, I <sub>D</sub> , I <sub>S</sub> (On)	±0.15			nA typ	$V_S = V_D = \pm 10 \text{ V}$ ; see Figure 25
Chairner On Leakage, ID, IS (On)			. 20	,,	VS = VD = ±10 V, see Figure 25
ADC1411MDCD7.DEFL.O.	±2	±4	±30	nA max	
ADG1411WBCPZ-REEL Only	±3		±40	nA max	
DIGITAL INPUTS					
Input High Voltage, V <sub>INH</sub>			2.0	V min	
Input Low Voltage, V <sub>INL</sub>			0.8	V max	
Input Current, I <sub>INL</sub> or I <sub>INH</sub>	0.005			μA typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			±0.1	μA max	
Digital Input Capacitance, C <sub>IN</sub>	3.5			pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>					
ton	100			ns typ	$R_L = 300 \Omega,  C_L = 35  pF$
	150	170	190	ns max	$V_S = 10 \text{ V}$ ; see Figure 30
toff	90			ns typ	$R_L = 300 \Omega$ , $C_L = 35 pF$
	120	140	160	ns max	V <sub>s</sub> = 10 V; see Figure 30
Break-Before-Make Time Delay, t <sub>D</sub>	25			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
(ADG1413 Only)					, ,
			10	ns min	$V_{S1} = V_{S2} = 10 \text{ V}$ ; see Figure 31
Charge Injection, Q <sub>INJ</sub>	-20			pC typ	$V_S = 0 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ ; see Figure 32
Off Isolation	-80			dB typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 100 kHz$ ; see Figure 26
Channel-to-Channel Crosstalk	-100			dB typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 1 MHz$ ; see Figure 27
Total Harmonic Distortion + Noise	0.014			% typ	$R_L = 110 \Omega$ , 15 V p-p, $f = 20 \text{ Hz to } 20 \text{ kHz}$ ;
					see Figure 29
–3 dB Bandwidth	170			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ ; see Figure 28
Insertion Loss	-0.35			dB typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 1 MHz$ ; see Figure 28
C <sub>s</sub> (Off)	23			pF typ	$V_S = 0 \text{ V, } f = 1 \text{ MHz}$
C <sub>D</sub> (Off)	23			pF typ	$V_S = 0 \text{ V, } f = 1 \text{ MHz}$
C <sub>D</sub> , C <sub>S</sub> (On)	116			pF typ	$V_S = 0 V, f = 1 MHz$
POWER REQUIREMENTS				<del>                                     </del>	$V_{DD} = +16.5 \text{ V}, V_{SS} = -16.5 \text{ V}$
IDD	0.001			μA typ	Digital inputs = 0 V or V <sub>DD</sub>
	3.001		1	μA max	
l <sub>DD</sub>	220			μΑ typ	Digital inputs = 5 V
עטו	220		380	μΑ typ μΑ max	Digital ilipats – 5 v
L	0.001		200		Digital inputs = 0 V c · V
Iss	0.001		1	μA typ	Digital inputs = $0 \text{ V or V}_{DD}$
V 0/			1	μA max	CND OV
$V_{DD}/V_{SS}$			±4.5/±16.5	V min/V max	GND = 0 V

 $<sup>^{\</sup>rm 1}\,\mbox{Guaranteed}$  by design; not subject to production test.

#### +12 V SINGLE SUPPLY

 $V_{DD}$  = 12 V ± 10%,  $V_{SS}$  = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V <sub>DD</sub>	V	
On Resistance, Ron	2.8			Ωtyp	$V_s = 0 \text{ V to } 10 \text{ V}, I_s = -10 \text{ mA}; \text{ see Figure } 23$
on nesistance, non	3.5	4.3	4.8	Ω max	$V_{DD} = 10.8 \text{ V}, V_{SS} = 0 \text{ V}$
On-Resistance Match	0.13	1.5	1.0	Ωtyp	$V_{S} = 0 \text{ V to } 10 \text{ V}, V_{SS} = 0 \text{ V}$
Between Channels, ΔR <sub>ON</sub>	0.13			12 (yp	VS = 0 V to 10 V, IS = -10 IIIA
	0.21	0.23	0.25	Ω max	
On-Resistance Flatness, R <sub>FLAT(ON)</sub>	0.6	5.25	0.25	Ωtyp	$V_S = 0 \text{ V to } 10 \text{ V}, I_S = -10 \text{ mA}$
on nearest names, menton	1.1	1.2	1.3	Ω max	
LEAKAGE CURRENTS	1	1.2	1.5	1211107	$V_{DD} = 10.8 \text{ V}, V_{SS} = 0 \text{ V}$
Source Off Leakage, Is (Off)	±0.02			nA typ	$V_{S} = 1 \text{ V}/10 \text{ V}, V_{S} = 0 \text{ V}$ $V_{S} = 1 \text{ V}/10 \text{ V}, V_{D} = 10 \text{ V}/0 \text{ V}; \text{ see Figure 24}$
Jource on Leakage, is (Oil)	±0.55	±2	±12.5	nA max	vs = 1 v/10 v, vb = 10 v/0 v, see rigule 24
ADG1411WBCPZ-REEL Only	±3	12	±40	nA max	
Drain Off Leakage, I <sub>D</sub> (Off)	±0.02		40		$V_S = 1 \text{ V}/10 \text{ V}, V_D = 10 \text{ V}/0 \text{ V}; \text{ see Figure 24}$
Diain On Leakage, ib (Oil)			.425	nA typ	$v_S = 1 \text{ V/ 10 V, } v_D = 10 \text{ V/0 V, see Figure 24}$
100111110000000000000000000000000000000	±0.55	±2	±12.5	nA max	
ADG1411WBCPZ-REEL Only	±3		±40	nA max	
Channel On Leakage, ID, Is (On)	±0.15			nA typ	$V_S = V_D = 1 \text{ V}/10 \text{ V}$ ; see Figure 25
	±1.5	±4	±30	nA max	
ADG1411WBCPZ-REEL Only	±3		±40	nA max	
DIGITAL INPUTS					
Input High Voltage, V <sub>INH</sub>			2.0	V min	
Input Low Voltage, V <sub>INL</sub>			0.8	V max	
Input Current, I <sub>INL</sub> or I <sub>INH</sub>	0.001			μA typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			±0.1	μA max	
Digital Input Capacitance, C <sub>IN</sub>	3.5			pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>					
ton	170			ns typ	$R_L = 300 \Omega$ , $C_L = 35 pF$
	250	295	330	ns max	$V_s = 8 \text{ V}$ ; see Figure 30
t <sub>off</sub>	75			ns typ	$R_L = 300 \Omega$ , $C_L = 35 pF$
	135	165	190	ns max	$V_s = 8 \text{ V}$ ; see Figure 30
Break-Before-Make Time Delay, t <sub>D</sub>	100			ns typ	$R_L = 300 \Omega$ , $C_L = 35 pF$
(ADG1413 Only)					
			40	ns min	$V_{S1} = V_{S2} = 8 \text{ V}$ ; see Figure 31
Charge Injection, Q <sub>INJ</sub>	30			pC typ	$V_s = 6 \text{ V}$ , $R_s = 0 \Omega$ , $C_L = 1 \text{ nF}$ ; see Figure 32
Off Isolation	-80			dB typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 100 kHz$ ; see Figure 26
Channel-to-Channel Crosstalk	-100			dB typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 1 MHz$ ; see Figure 27
−3 dB Bandwidth	130			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ ; see Figure 28
Insertion Loss	-0.5			dB typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 1 MHz$ ; see Figure 28
C <sub>s</sub> (Off)	38			pF typ	$V_s = 6 \text{ V}, f = 1 \text{ MHz}$
C <sub>D</sub> (Off)	40			pF typ	$V_s = 6 \text{ V}, f = 1 \text{ MHz}$
C <sub>D</sub> , C <sub>s</sub> (On)	104			pF typ	$V_S = 6 \text{ V}, f = 1 \text{ MHz}$
POWER REQUIREMENTS				7 71	$V_{DD} = 13.2 \text{ V}$
I <sub>DD</sub>	0.001			μA typ	Digital inputs = $0 \text{ V or V}_{DD}$
00	0.001		1	μΑ typ μΑ max	Digital inpats = 0 v oi voo
	220		'	μΑτιιαχ μΑ typ	Digital inputs = 5 V
	220		380	μΑ typ μΑ max	Digital Inputs – 5 v
V					$GND = 0 \text{ V}, \text{ V}_{SS} = 0 \text{ V}$
$V_{DD}$			5/16.5	V min/V max	GIND = U V, VSS = U V

 $<sup>^{\</sup>rm 1}\,\mbox{Guaranteed}$  by design; not subject to production test.

#### ±5 V DUAL SUPPLY

 $V_{\text{DD}}$  = 5 V  $\pm$  10%,  $V_{\text{SS}}$  = -5 V  $\pm$  10%, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V <sub>DD</sub> to V <sub>SS</sub>	V	
On Resistance, Ron	3.3			Ω typ	$V_s = \pm 4.5 \text{ V}, I_s = -10 \text{ mA}$ ; see Figure 23
	4	4.9	5.4	Ω max	$V_{DD} = +4.5 \text{ V}, V_{SS} = -4.5 \text{ V}$
On-Resistance Match	0.13			Ωtyp	$V_s = \pm 4.5 \text{ V, } I_s = -10 \text{ mA}$
Between Channels, ΔR <sub>ON</sub>				,,	
	0.22	0.23	0.25	Ω max	
On-Resistance Flatness, R <sub>FLAT(ON)</sub>	0.9			Ω typ	$V_S = \pm 4.5 \text{ V; } I_S = -10 \text{ mA}$
	1.1	1.24	1.31	Ω max	
LEAKAGE CURRENTS					$V_{DD} = +5.5 \text{ V}, V_{SS} = -5.5 \text{ V}$
Source Off Leakage, Is (Off)	±0.03			nA typ	$V_S = \pm 4.5 \text{ V}, V_D = \mp 4.5 \text{ V}; \text{ see Figure 24}$
	±0.55	±2	±12.5	nA max	
ADG1411WBCPZ-REEL Only	±3		±40	nA max	
Drain Off Leakage, I <sub>D</sub> (Off)	±0.03			nA typ	$V_S = \pm 4.5 \text{ V}, V_D = \mp 4.5 \text{ V}; \text{ see Figure 24}$
3,75,7	±0.55	±2	±12.5	nA max	13 = 13 1, 15 1 13 1, 300 1 1ga 10 2 1
ADG1411WBCPZ-REEL Only	±3		±40	nA max	
Channel On Leakage, I <sub>D</sub> , I <sub>S</sub> (On)	±0.05		±40	nA typ	$V_S = V_D = \pm 4.5 \text{ V}$ ; see Figure 25
Charmer on Leakage, ID, IS (OH)			. 20		V5 = VD = ±4.5 V, see rigure 25
ADC1411WDCD7 DEEL O. I. 1	±1.0	±4	±30	nA max	
ADG1411WBCPZ-REEL Only1	±3		±40	nA max	
DIGITAL INPUTS				., .	
Input High Voltage, V <sub>INH</sub>			2.0	V min	
Input Low Voltage, V <sub>INL</sub>			0.8	V max	
Input Current, I <sub>INL</sub> or I <sub>INH</sub>	0.001			μA typ	$V_{IN} = V_{GND} \text{ or } V_{DD}$
			±0.1	μA max	
Digital Input Capacitance, C <sub>IN</sub>	3.5			pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>					
t <sub>on</sub>	275			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	400	465	510	ns max	$V_s = 3 \text{ V}$ ; see Figure 30
t <sub>OFF</sub>	175			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	290	320	380	ns max	$V_s = 3 \text{ V}$ ; see Figure 30
Break-Before-Make Time Delay,	100			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
t <sub>D</sub> (ADG1413 Only)					
			50	ns min	$V_{S1} = V_{S2} = 3 \text{ V; see Figure 31}$
Charge Injection, Q <sub>INJ</sub>	30			pC typ	$V_S = 0 \text{ V}, R_S = 0 \Omega, C_L = 1 \text{ nF}; \text{ see Figure 32}$
Off Isolation	-80			dB typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 100 kHz$ ; see Figure 26
Channel-to-Channel Crosstalk	-100			dB typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 1 MHz$ ; see Figure 27
Total Harmonic Distortion + Noise	0.03			% typ	$R_L$ = 110 Ω, 5 V p-p, f = 20 Hz to 20 kHz; see Figure 29
–3 dB Bandwidth	130			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ ; see Figure 28
Insertion Loss	-0.5			dB typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 1 MHz$ ; see Figure 28
C <sub>s</sub> (Off)	32			pF typ	$V_s = 0 \text{ V, } f = 1 \text{ MHz}$
C <sub>D</sub> (Off)	33			pF typ	$V_s = 0 \text{ V, } f = 1 \text{ MHz}$
C <sub>D</sub> , C <sub>S</sub> (On)	116			pF typ	$V_S = 0 \text{ V, } f = 1 \text{ MHz}$
POWER REQUIREMENTS				71	$V_{DD} = +5.5 \text{ V}, V_{SS} = -5.5 \text{ V}$
I <sub>DD</sub>	0.001			μA typ	Digital inputs = 0 V or V <sub>DD</sub>
			1.0	μA max	
Iss	0.001		1.0	μA typ	Digital inputs = 0 V or V <sub>DD</sub>
133	0.001	1	1.0	μΑ typ μΑ max	Signal inputs – o v oi voi
			1.0	I IIA max	

 $<sup>^{\</sup>rm 1}$  Guaranteed by design; not subject to production test.

### **ABSOLUTE MAXIMUM RATINGS**

 $T_A = 25$ °C, unless otherwise noted.

Table 4.

Table 4.	
Parameter	Rating
V <sub>DD</sub> to V <sub>SS</sub>	35 V
V <sub>DD</sub> to GND	−0.3 V to +25 V
V <sub>SS</sub> to GND	+0.3 V to −25 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3 \text{ V to } V_{DD} + 0.3 \text{ V or}$ 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	GND $- 0.3 \text{ V}$ to $V_{DD} + 0.3 \text{ V}$ or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	500 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current per Channel at 25°C	
16-Lead TSSOP	190 mA
16-Lead LFCSP	250 mA
Continuous Current per Channel at 125°C	
16-Lead TSSOP	90 mA
16-Lead LFCSP	100 mA
Operating Temperature Range	
Automotive (Y Version)	-40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
$\theta_{JA}$ Thermal Impedance	
16-Lead TSSOP (4-Layer Board)	112°C/W
16-Lead LFCSP	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/-5)°C

<sup>&</sup>lt;sup>1</sup> Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

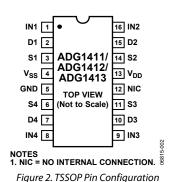
Only one absolute maximum rating may be applied at any one time.

#### **ESD CAUTION**



**ESD** (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



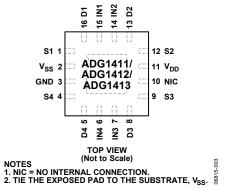


Figure 3. LFCSP Pin Configuration

**Table 5. Pin Function Descriptions** 

F	Pin No.		
TSSOP	LFCSP	Mnemonic	Description
1	15	IN1	Logic Control Input.
2	16	D1	Drain Terminal. This pin can be an input or output.
3	1	S1	Source Terminal. This pin can be an input or output.
4	2	Vss	Most Negative Power Supply Potential.
5	3	GND	Ground (0 V) Reference.
6	4	S4	Source Terminal. This pin can be an input or output.
7	5	D4	Drain Terminal. This pin can be an input or output.
8	6	IN4	Logic Control Input.
9	7	IN3	Logic Control Input.
10	8	D3	Drain Terminal. This pin can be an input or output.
11	9	S3	Source Terminal. This pin can be an input or output.
12	10	NIC	No Internal Connection.
13	11	$V_{DD}$	Most Positive Power Supply Potential.
14	12	S2	Source Terminal. This pin can be an input or output.
15	13	D2	Drain Terminal. This pin can be an input or output.
16	14	IN2	Logic Control Input.
$N/A^1$	0	EPAD	Exposed Pad. Tie the exposed pad to the substrate, Vss.

<sup>&</sup>lt;sup>1</sup> N/A means not applicable.

#### Table 6. ADG1411/ADG1412 Truth Table

140.4 01.12 01.11 1.40.1				
ADG1411 INx	ADG1412 INx	Switch Condition		
0	1	On		
1	0	Off		

#### Table 7. ADG1413 Truth Table

ADG1413 INx	S1, S4	S2, S3
0	Off	On
1	On	Off

### TYPICAL PERFORMANCE CHARACTERISTICS

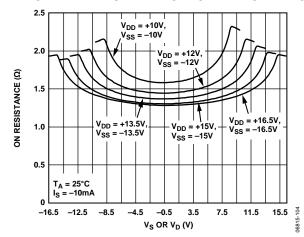


Figure 4. On Resistance vs. V<sub>D</sub> or V<sub>S</sub>, Dual Supply

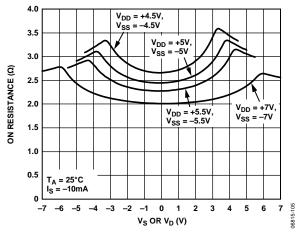


Figure 5. On Resistance vs.  $V_D$  or  $V_S$ , Dual Supply

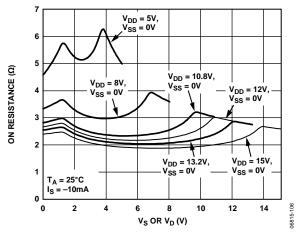


Figure 6. On Resistance vs.  $V_D$  or  $V_S$ , Single Supply

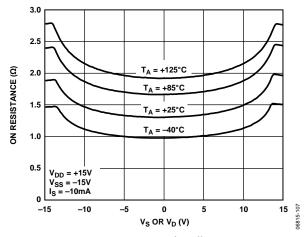


Figure 7. On Resistance vs. V<sub>D</sub> or V<sub>S</sub> for Different Temperatures, ±15 V Dual Supply

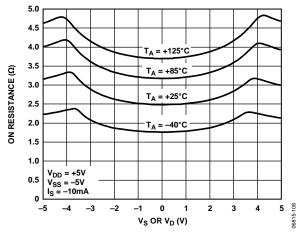


Figure 8. On Resistance vs.  $V_D$  or  $V_S$  for Different Temperatures,  $\pm 5$  V Dual Supply

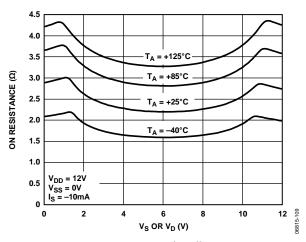


Figure 9. On Resistance vs.  $V_D$  or  $V_S$  for Different Temperatures, +12 V Single Supply

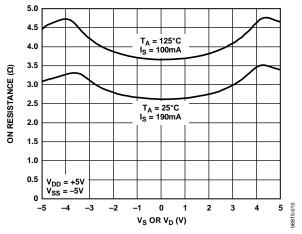


Figure 10. On Resistance vs.  $V_D$  or  $V_S$  for Different Current Levels,  $\pm 5 V$  Dual Supply

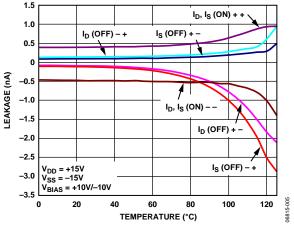


Figure 11. Leakage Currents vs. Temperature, ±15 V Dual Supply

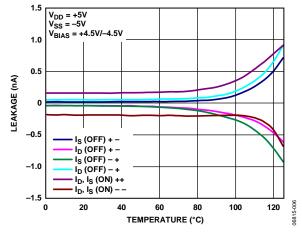


Figure 12. Leakage Currents vs. Temperature, ±5 V Dual Supply

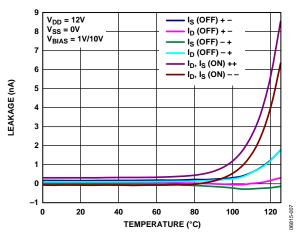


Figure 13. Leakage Currents vs. Temperature, +12 V Single Supply

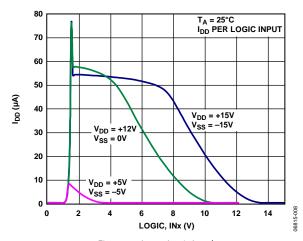


Figure 14. IDD vs. Logic Level

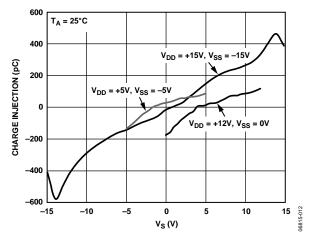


Figure 15. Charge Injection vs. Source Voltage

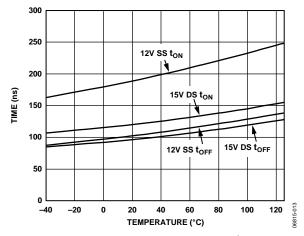


Figure 16. t<sub>ON</sub>/t<sub>OFF</sub> Times vs. Temperature for Single Supply (SS) and Dual Supply (DS)

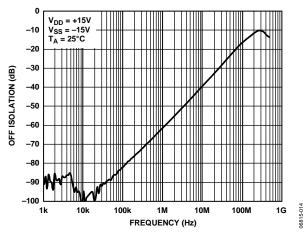


Figure 17. Off Isolation vs. Frequency, ±15 V Dual Supply

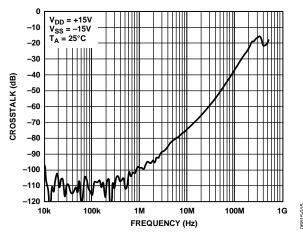


Figure 18. Crosstalk vs. Frequency, ±15 V Dual Supply

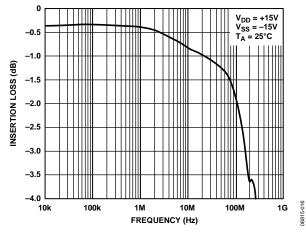


Figure 19. On Response vs. Frequency, ±15 V Dual Supply

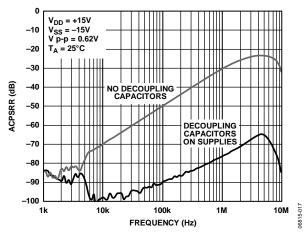


Figure 20. ACPSRR vs. Frequency, ±15 V Dual Supply

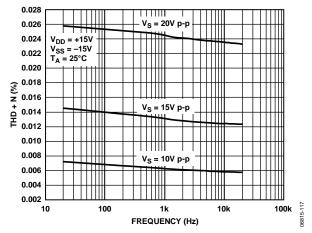


Figure 21. THD + N vs. Frequency, ±15 V Dual Supply

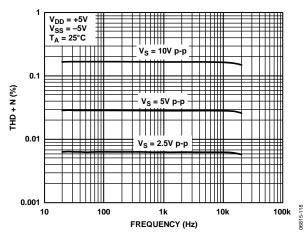


Figure 22. THD + N vs. Frequency, ±5 V Dual Supply

## **TERMINOLOGY**

 $I_{DD}$ 

The positive supply current.

Iss

The negative supply current.

VD, Vs

The analog voltage on Terminal D and Terminal S.

RON

The ohmic resistance between Terminal D and Terminal S.

R<sub>FLAT(ON)</sub>

Flatness is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

Is (Off)

The source leakage current with the switch off.

I<sub>D</sub> (Off)

The drain leakage current with the switch off.

 $I_D$ ,  $I_S$  (On)

The channel leakage current with the switch on.

 $V_{INI}$ 

The maximum input voltage for Logic 0.

 $V_{\text{INH}}$ 

The minimum input voltage for Logic 1.

IINL, IINE

The input current of the digital input when high or when low.

Cs (Off)

The off switch source capacitance, which is measured with reference to ground.

CD (Off)

The off switch drain capacitance, which is measured with reference to ground.

 $C_D$ ,  $C_S$  (On)

The on switch capacitance, which is measured with reference to ground.

 $C_{IN}$ 

The digital input capacitance.

ton

The delay between applying the digital control input and the output switching on. See Figure 30.

 $t_{OFF}$ 

The delay between applying the digital control input and the output switching off.

**Charge Injection** 

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

**Insertion Loss** 

The loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)

A measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of the signal on the output to the amplitude of the modulation is the ACPSRR.

## **TEST CIRCUITS**

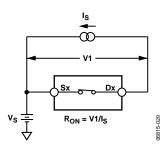


Figure 23. On Resistance

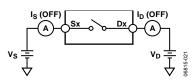
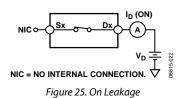


Figure 24. Off Leakage



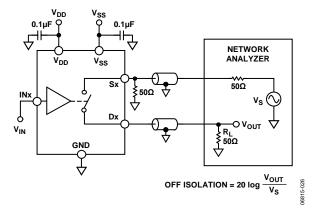


Figure 26. Off Isolation

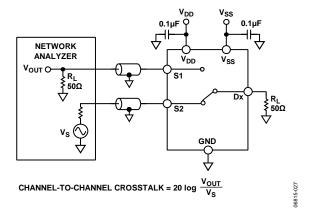


Figure 27. Channel-to-Channel Crosstalk

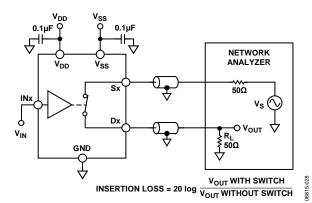


Figure 28. Bandwidth

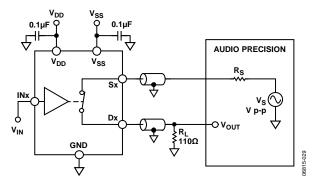


Figure 29. THD + Noise

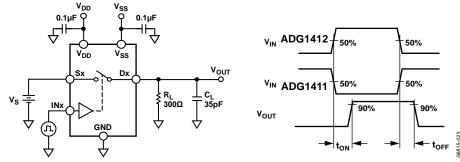


Figure 30. Switching Times

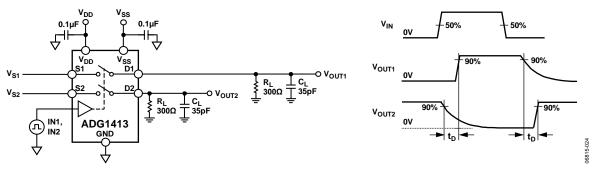


Figure 31. Break-Before-Make Time Delay

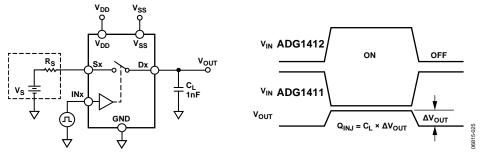
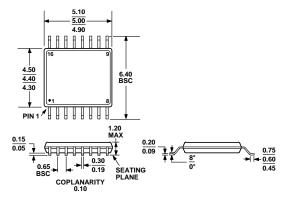


Figure 32. Charge Injection

# **OUTLINE DIMENSIONS**



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 33. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16) Dimensions shown in millimeters

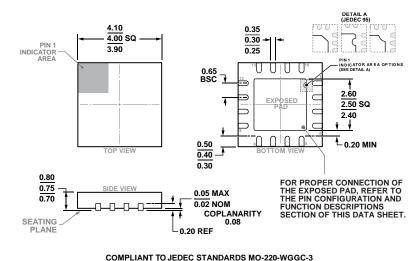


Figure 34. 16-Lead Lead Frame Chip Scale Package [LFCSP] 4 mm × 4 mm Body and 0.75 mm Package Height (CP-16-26) Dimensions shown in millimeters

08-27-20

#### **ORDERING GUIDE**

Model <sup>1, 2</sup>	Temperature Range	Package Description	Package Option
ADG1411YRUZ	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1411YRUZ-REEL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1411YCPZ-REEL	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26
ADG1411YCPZ-REEL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26
ADG1411WBCPZ-REEL	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26
ADG1412YRUZ	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1412YRUZ-REEL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1412YCPZ-REEL	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26
ADG1412YCPZ-REEL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26
ADG1413YRUZ	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1413YRUZ-REEL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1413YCPZ-REEL	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26
ADG1413YCPZ-REEL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26

<sup>&</sup>lt;sup>1</sup> Z = RoHS Compliant Part.

#### **AUTOMOTIVE PRODUCTS**

The ADG1411W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade product shown is available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for this model.

 $<sup>^{2}</sup>$  W = qualified for automotive applications.