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REVISION HISTORY

9/2020—Rev. A to Rev. B

Changed CP-48-1 to CP-48-4 ... Throughout
Added Figure 4; Renumbered Sequentially ... 7
Updated Outline Dimensions ... 23
Changes to Ordering Guide ... 23

9/2007—Rev. 0 to Rev. A

Changes to Figure 14, Figure 15, and Figure 16 ... 10
Changes to Applications Information Section ... 21
Changes to Ordering Guide ... 23

5/2007—Revision 0: Initial Version

SPECIFICATIONS

AVDD = 3.3 V, DVDD = 3.3 V, PVDD = 15 V, ambient temperature = 25°C, load impedance = 6 Ω, clock frequency = 24.576 MHz, measurement bandwidth = 20 Hz to 20 kHz, unless otherwise specified.

AUDIO PERFORMANCE

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT POWER[1]					1 kHz
		12		W	1% THD + N, 8 Ω
		15		W	10% THD + N, 8 Ω
		14.5		W	1% THD + N, 6 Ω
		18		W	10% THD + N, 6 Ω
		19.5		W	1% THD + N, 4 Ω
		24		W	10% THD + N, 4 Ω
EFFICIENCY		87		%	@ 18 W, 6 Ω
R_{DS-ON}					@ T_{CASE} = 25°C
Per High-Side Transistor		0.28		Ω	@ 100 mA
Per Low-Side Transistor		0.25		Ω	@ 100 mA
THERMAL CHARACTERISTICS					
Thermal Warning Active[2]		135		°C	Die temperature
Thermal Shutdown Active		150		°C	Die temperature
OVERCURRENT SHUTDOWN ACTIVE	5	6		A	Peak current
PVDD UNDERVOLTAGE SHUTDOWN		5.1		V	
INPUT LEVEL FOR FULL-SCALE OUTPUT					Full-scale output @ 1% THD + N
		1.0		V_{rms}	PGA gain = 0 dB
		0.5		V_{rms}	PGA gain = 6 dB
		0.25		V_{rms}	PGA gain = 12 dB
		0.125		V_{rms}	PGA gain = 18 dB
TOTAL HARMONIC DISTORTION + NOISE (THD + N)		0.005		%	1 kHz, P_{OUT} = 1 W, PGA gain = 0 dB
SIGNAL-TO-NOISE RATIO (SNR)	99	101		dB	A-weighted, referred to 1% THD + N output
DYNAMIC RANGE (DNR)	99	101		dB	A-weighted, measured with −60 dBFS input
CROSSTALK (LEFT TO RIGHT OR RIGHT TO LEFT)		−90		dB	@ full-scale output voltage, 1% THD + N, 1 kHz
AMPLIFIER GAIN					PVDD = 15 V, 6 Ω
PGA = 0 dB		19		dB	
PGA = 6 dB		25		dB	
PGA = 12 dB		31		dB	
PGA = 18 dB		37		dB	
OUTPUT NOISE VOLTAGE					PVDD = 15 V, 6 Ω
PGA = 0 dB		78		µV	
PGA = 6 dB		100		µV	
PGA = 12 dB		158		µV	
PGA = 18 dB		280		µV	
POWER SUPPLY REJECTION RATIO (PSRR)		65		dB	20 Hz to 20 kHz, 1.5 V p-p ripple, inputs ac-coupled to AGND

[1] Output powers above 12 W at 4 Ω and above 18 W at 6 Ω are not continuous and are thermally limited by the package dissipation.
[2] Thermal warning flag is for indication of device T_J reaching close to shutdown temperature.

DC SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT IMPEDANCE		20		kΩ	AINL/AINR
OUTPUT DC OFFSET VOLTAGE		±3		mV	

POWER SUPPLIES

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG SUPPLY VOLTAGE (AVDD)	3.0	3.3	3.6	V	
DIGITAL SUPPLY VOLTAGE (DVDD)	3.0	3.3	3.6	V	
POWER TRANSISTOR SUPPLY VOLTAGE (PVDD)	9	15	18	V	
POWER-DOWN CURRENT					$\overline{\text{STDN}}$ held low
AVDD		5	60	µA	
DVDD		0.1	0.24	mA	
PVDD		0.082	0.25	mA	
MUTE CURRENT					$\overline{\text{MUTE}}$ held low
AVDD		13	20	mA	
DVDD		1.7	3.2	mA	
PVDD		5.4	8	mA	
OPERATING CURRENT					$\overline{\text{STDN}}$ and $\overline{\text{MUTE}}$ held high, no input
AVDD		13	30	mA	
DVDD		2.7	4	mA	
PVDD		44	65	mA	

DIGITAL I/O

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT VOLTAGE					
Input Voltage High	2			V	
Input Voltage Low			0.8	V	
OUTPUT VOLTAGE					
Output Voltage High	2			V	@ 2 mA
Output Voltage Low			0.4	V	@ 2 mA
LEAKAGE CURRENT ON DIGITAL INPUTS			10	µA	

DIGITAL TIMING

Table 5.

Parameter	Min	Typ	Unit	Test Conditions/Comments
t_{WAIT}	0.01[1]	1000[2]	ms	Wait time for unmute
t_{INT}		650	ms	Internal mute time
t_{HOLD}	10[1]	250[3]	µs	Wait time for shutdown
$t_{OUTx+/OUTx-\ SW}$		200	µs	Time delay after $\overline{MUTE}$ held high until output starts switching
$t_{OUTx+/OUTx-\ MUTE}$		200	µs	Time delay after $\overline{MUTE}$ held low until output stops switching

[1] $t_{WAIT\ MIN}$ and $t_{HOLD\ MIN}$ are the minimum times for fast turn-on and do not guarantee pop-and-click suppression.
[2] $t_{WAIT\ TYP}$ is the recommended value for minimum pop and click during the unmute of the amplifier. The recommended value is 1 sec. It is calculated using the input coupling capacitor value and the input resistance of the device. See the Power-Up/Power-Down Sequence section.
[3] $t_{HOLD\ TYP}$ is the recommended value for minimum pop and click during the mute of the amplifier.

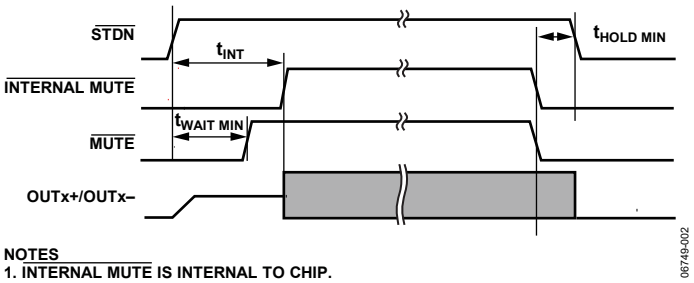


Figure 2. Timing Diagram (Minimum)

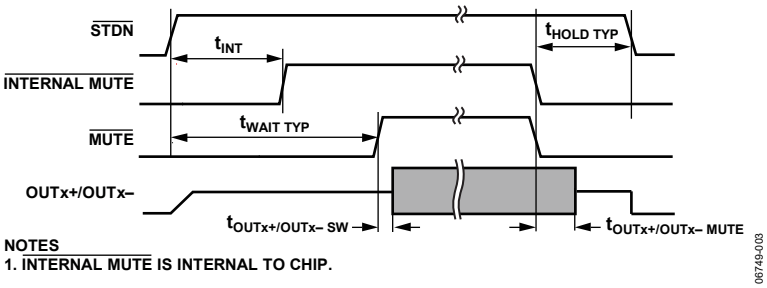


Figure 3. Timing Diagram (Typical)

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
DVDD to DGND	−0.3 V to +3.6 V
AVDD to AGND	−0.3 V to +3.6 V
PVDD to PGND[1]	−0.3 V to +20.0 V
$\overline{\text{MUTE}}$/$\overline{\text{STDN}}$ Inputs	DGND − 0.3 V to DVDD + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature	
Soldering (10 sec)	260°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] Includes any induced voltage due to inductive load.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[1,2]	Ψ_{JB}	Ψ_{JT}	Unit
LFCSP-48	24.6	2.0	8.05	0.18	°C/W
TQFP-48	24.7	1.63	11	0.8	°C/W

[1] With exposed pad (ePAD) soldered to 4-layer JEDEC standard PCB.
[2] Through the bottom (ePAD) surface.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

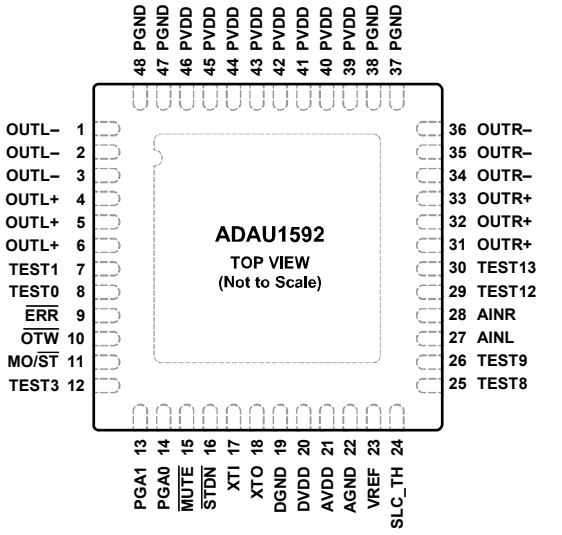


Figure 4. 48-Lead LFCSP Pin Configuration

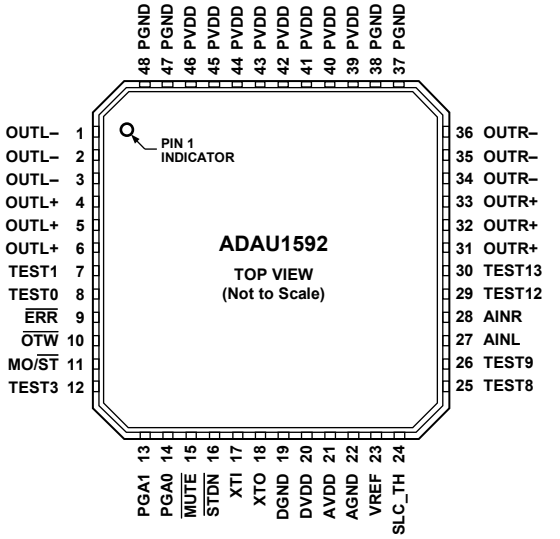


Figure 5. 48-Lead TQFP_EP Pin Configuration

Table 8. Pin Function Descriptions

Pin Number	Mnemonic	Type[1]	Description
1, 2, 3	OUTL–	O	Output of High Power Transistors, Left Channel Negative Polarity.
4, 5, 6	OUTL+	O	Output of High Power Transistors, Left Channel Positive Polarity.
7	TEST1	I	Reserved for Internal Use. Connect to DGND.
8	TEST0	I	Reserved for Internal Use. Connect to DGND.
9	$\overline{\text{ERR}}$	O	Error Indicator (Active Low, Open-Drain Output).
10	$\overline{\text{OTW}}$	O	Overtemperature Warning Indicator (Active Low, Open-Drain Output).
11	MO/$\overline{\text{ST}}$	I	Mono/Stereo Mode Setting Pin for Stereo. Connect to DGND (for mono mode, connect to DVDD).
12	TEST3	I	Reserved for Internal Use. Connect to DVDD.
13	PGA1	I	Programmable Gain Amplifier Select, MSB.
14	PGA0	I	Programmable Gain Amplifier Select, LSB.
15	$\overline{\text{MUTE}}$	I	Mute (Active Low Input).
16	$\overline{\text{STDN}}$	I	Shutdown/Reset Input (Active Low Input).
17	XTI	I	Quartz Crystal Connection/External Clock Input.
18	XTO	O	Quartz Crystal Connection/Clock Output.
19	DGND	P	Digital Ground for Digital Circuitry. Internally connected to exposed pad (ePAD).
20	DVDD	P	Positive Supply for Digital Circuitry.
21	AVDD	P	Positive Supply for Analog Circuitry. (Can be tied to DVDD.)
22	AGND	P	Analog Ground for Analog Circuitry. (See the notes in Figure 5 for connection to ePAD.)
23	VREF	I	AVDD/2 Voltage Reference Connection for External Filter.
24	SLC_TH	I	Slicer Threshold Adjust. (Connect to AGND via a resistor for slicer operation.)
25	TEST8	I	Reserved for Internal Use. Connect to DGND.
26	TEST9	I	Reserved for Internal Use. Connect to DGND.
27	AINL	I	Analog Input Left Channel.
28	AINR	I	Analog Input Right Channel.
29	TEST12	I	Reserved for Internal Use. Connect to DGND.
30	TEST13	I	Reserved for Internal Use. Connect to DGND.
31, 32, 33	OUTR+	O	Output of High Power Transistors, Right Channel Positive Polarity.

Pin Number	Mnemonic	Type[1]	Description
34, 35, 36	OUTR–	O	Output of High Power Transistors, Right Channel Negative Polarity.
37, 38, 47, 48	PGND	P	Power Ground for High Power Transistors. Internally connected to ePAD.
39, 40, 41, 42, 43, 44, 45, 46	PVDD	P	Positive Power Supply for High Power Transistors.

[1] I = input, O = output, P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

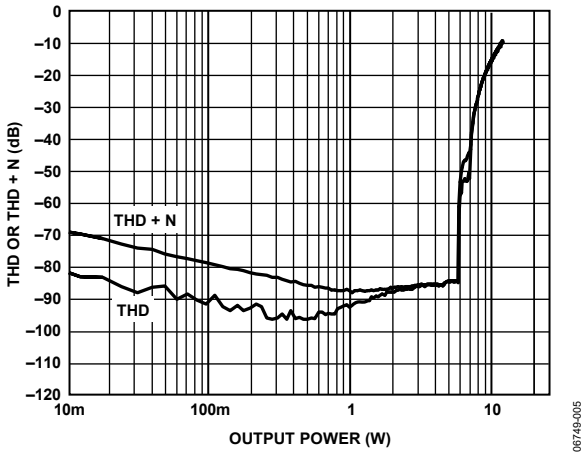


Figure 6. THD or THD + N vs. Output Power, 4 Ω, PVDD = 9 V

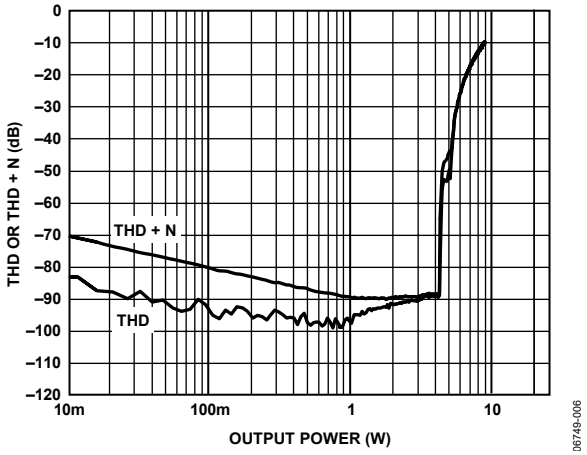


Figure 7. THD or THD + N vs. Output Power, 6 Ω, PVDD = 9 V

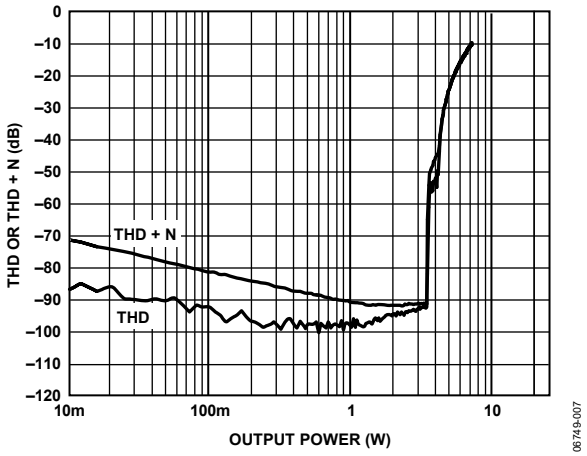


Figure 8. THD or THD + N vs. Output Power, 8 Ω, PVDD = 9 V

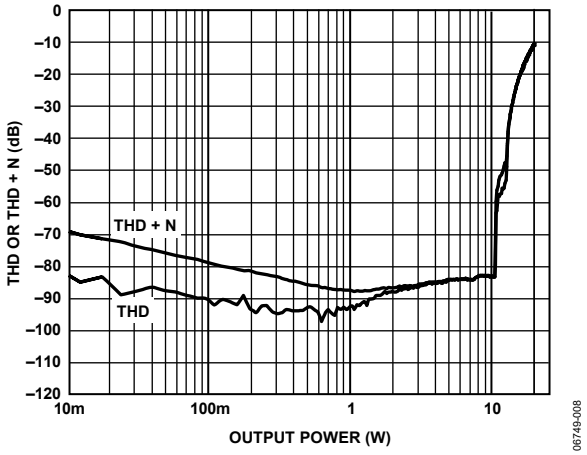


Figure 9. THD or THD + N vs. Output Power, 4 Ω, PVDD = 12 V

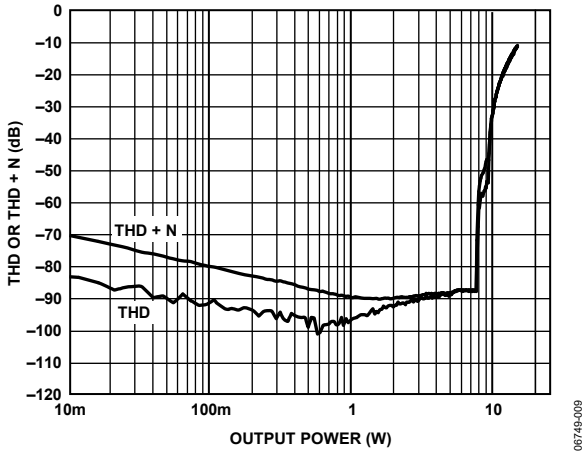


Figure 10. THD or THD + N vs. Output Power, 6 Ω, PVDD = 12 V

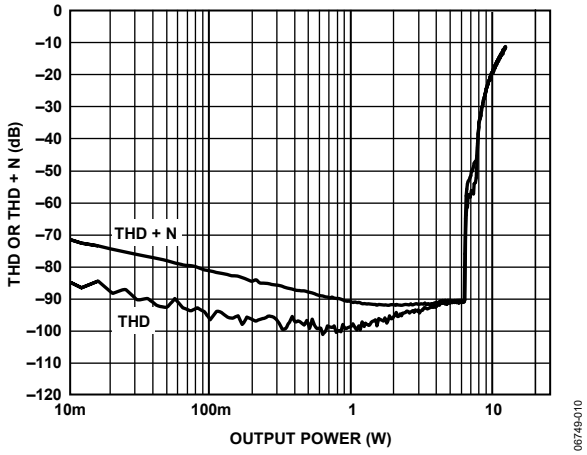


Figure 11. THD or THD + N vs. Output Power, 8 Ω, PVDD = 12 V

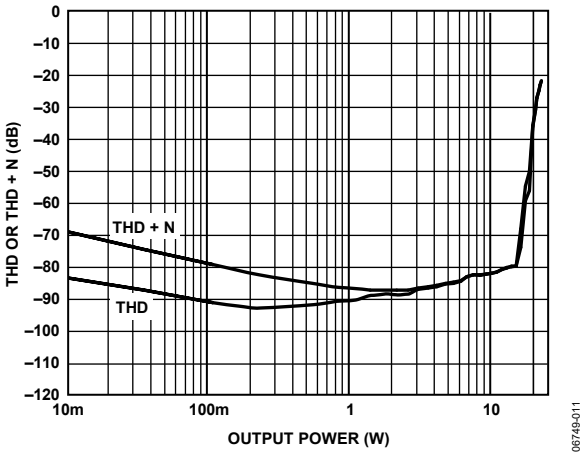


Figure 12. THD or THD + N vs. Output Power, 4 Ω, PVDD = 15 V

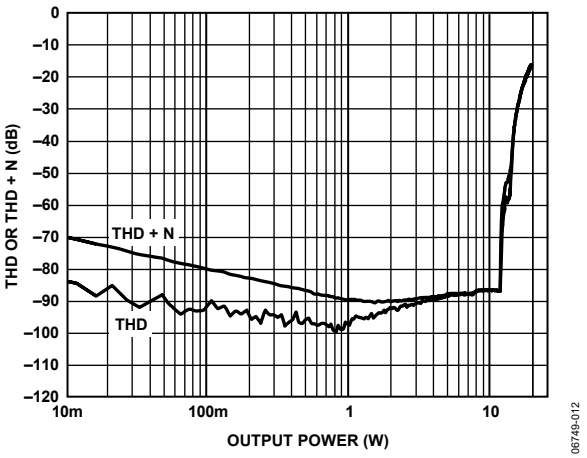


Figure 13. THD or THD + N vs. Output Power, 6 Ω, PVDD = 15 V

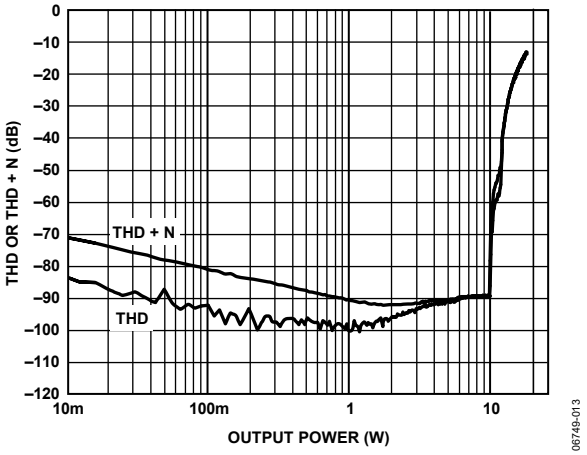


Figure 14. THD or THD + N vs. Output Power, 8 Ω, PVDD = 15 V

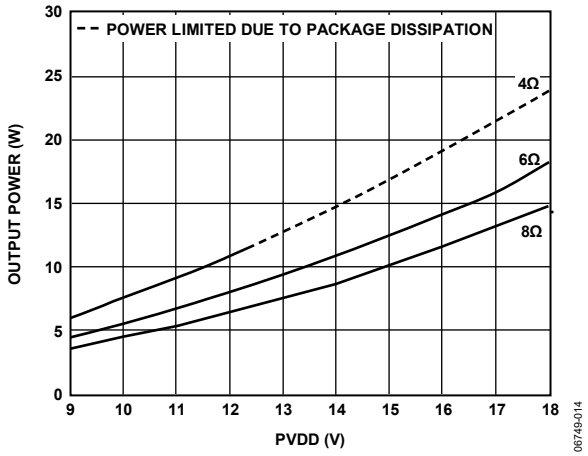


Figure 15. Output Power vs. PVDD @ 0.1% THD + N

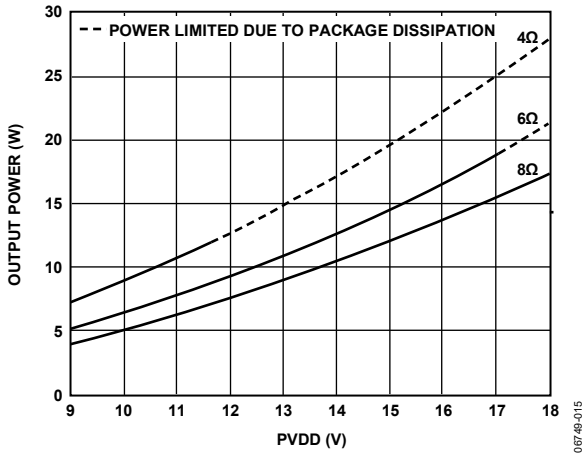


Figure 16. Output Power vs. PVDD @ 1% THD + N

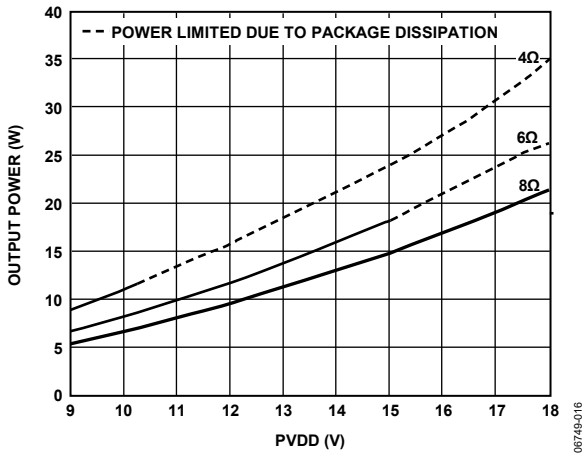


Figure 17. Output Power vs. PVDD @ 10% THD + N

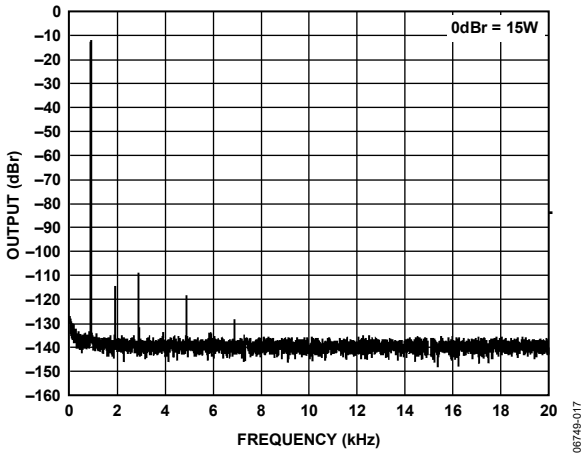


Figure 18. FFT @ 1 W, 6 Ω, PVDD = 15 V, PGA = 0 dB, 1 kHz Sine

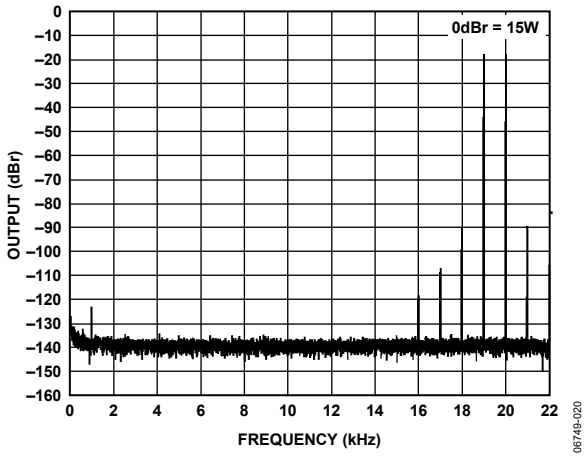


Figure 21. FFT @ 1 W, 6 Ω, PVDD = 15 V, PGA = 0 dB, 19 kHz and 20 kHz Sine

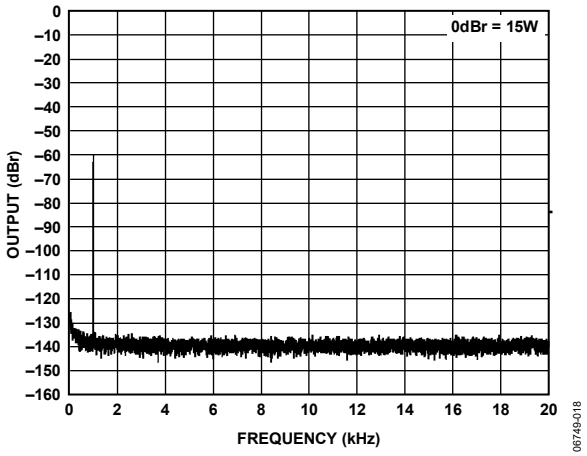


Figure 19. FFT @ −60 dBFS, 6 Ω, PVDD = 15 V, PGA = 0 dB, 1 kHz Sine

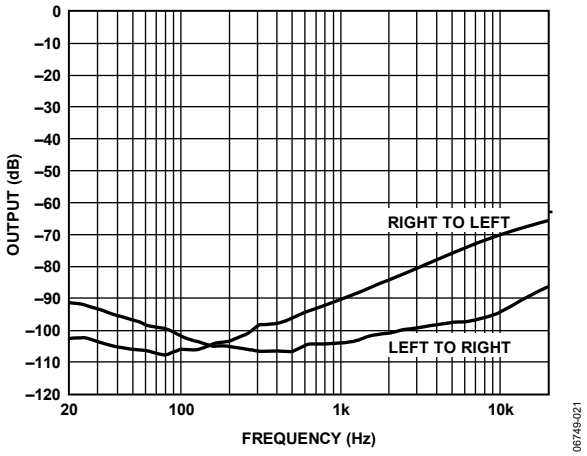


Figure 22. Crosstalk @ 1 W, 6 Ω, PVDD = 15 V, PGA = 0 dB

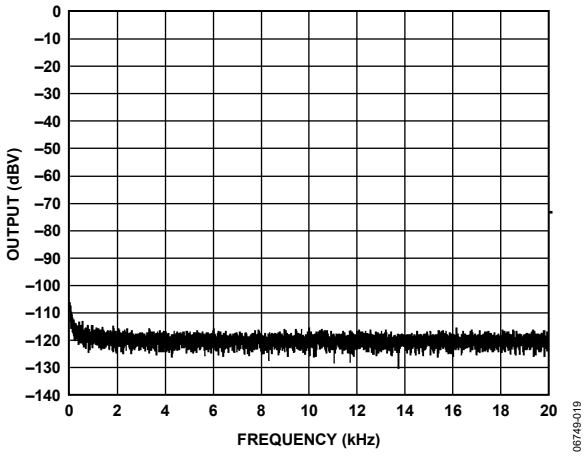


Figure 20. FFT No Input, 6 Ω, PVDD = 15 V, PGA = 0 dB

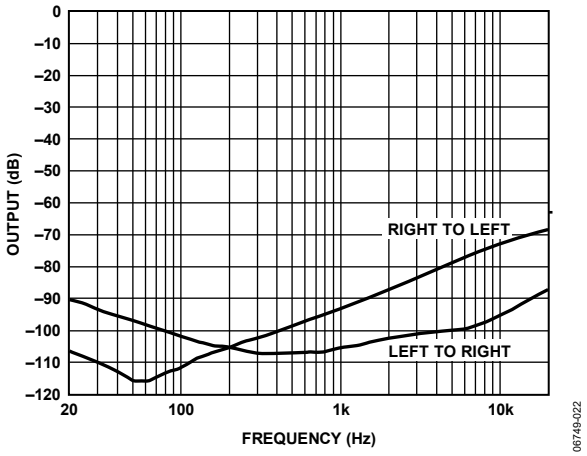


Figure 23. Crosstalk @ Full Scale, 6 Ω, PVDD = 15 V, PGA = 0 dB

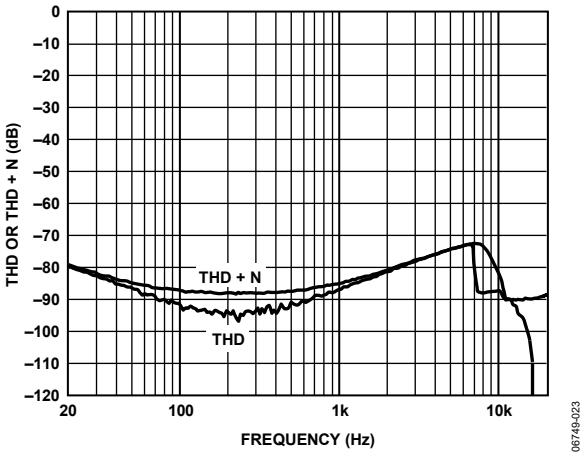


Figure 24. THD or THD + N vs. Frequency @ 1 W, 4 Ω, PVDD = 15 V, PGA = 0 dB

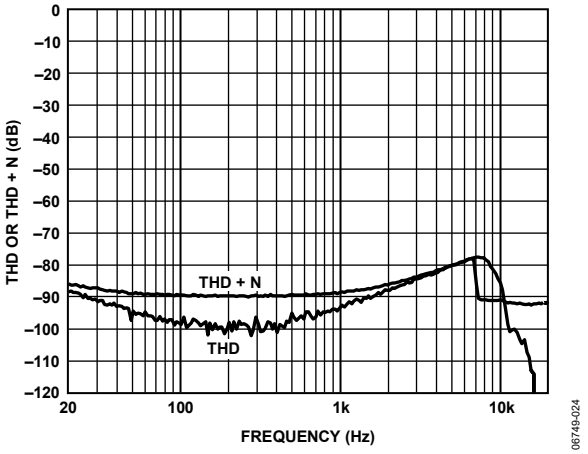


Figure 25. THD or THD + N vs. Frequency @ 1 W, 6 Ω, PVDD = 15 V, PGA = 0 dB

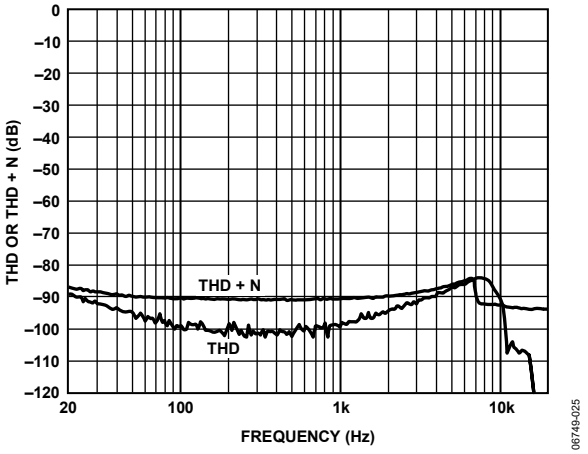


Figure 26. THD or THD + N vs. Frequency @ 1 W, 8 Ω, PVDD = 15 V, PGA = 0 dB

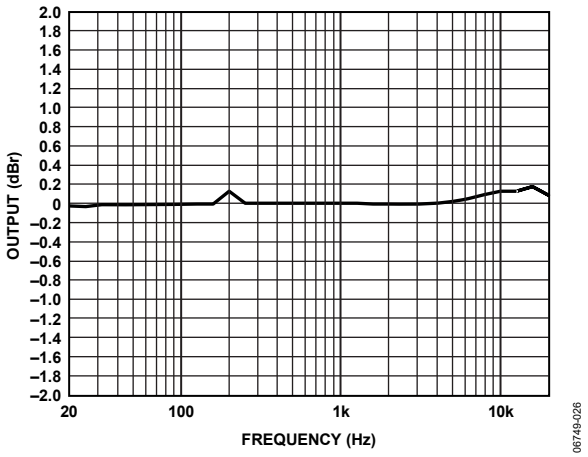


Figure 27. Frequency Response @ 1 W, 6 Ω, PVDD = 15 V, PGA = 0 dB

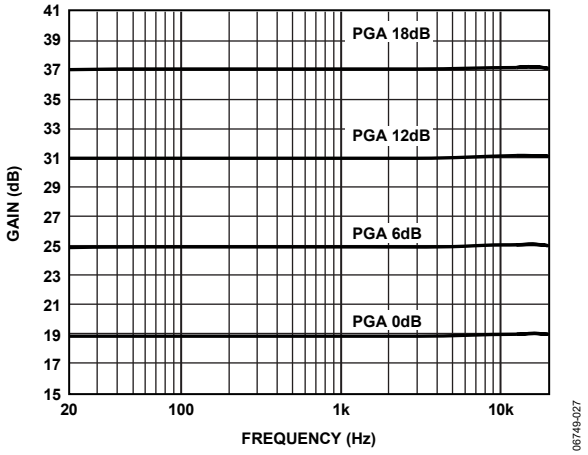


Figure 28. Gain vs. Frequency @ 1 W, 6 Ω, PVDD = 15 V

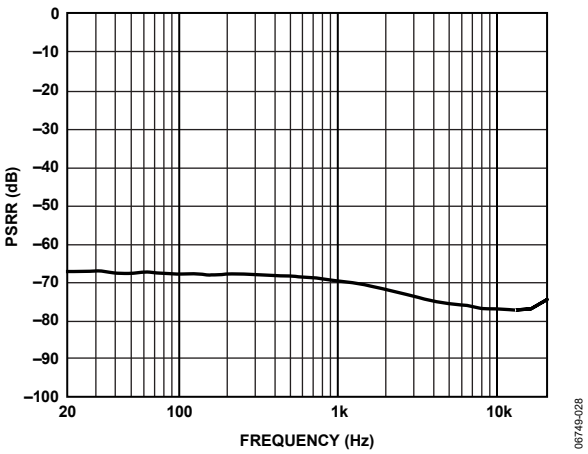


Figure 29. PSRR vs. Frequency, No Input Signal, Ripple = 1.5 V p-p, PVDD = 15 V, 6 Ω

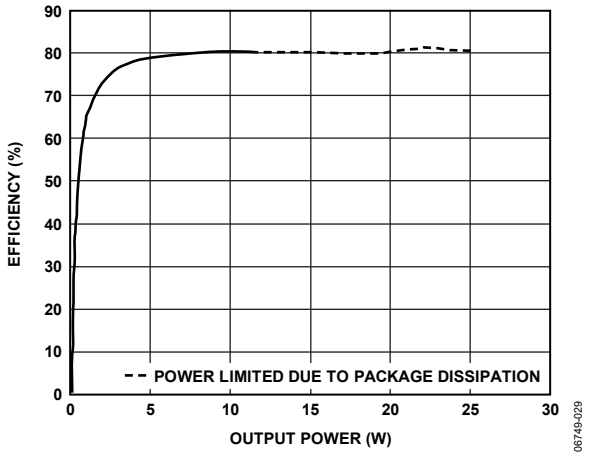


Figure 30. Efficiency vs. Output Power, 15 V, 4 Ω

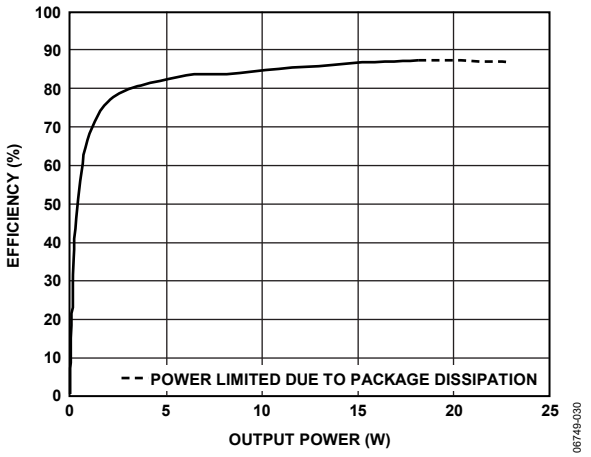


Figure 31. Efficiency vs. Output Power, 15 V, 6 Ω

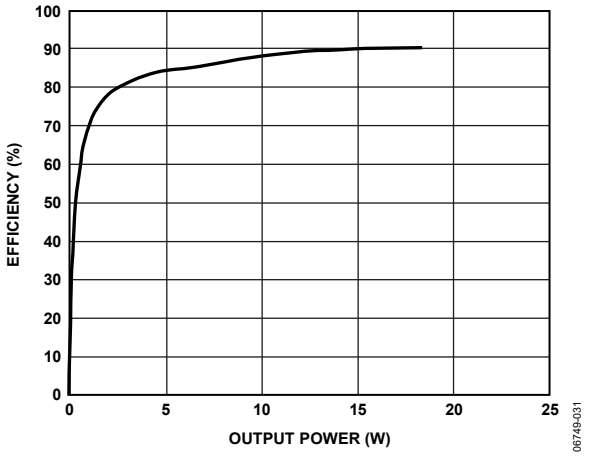


Figure 32. Efficiency vs. Output Power, 15 V, 8 Ω

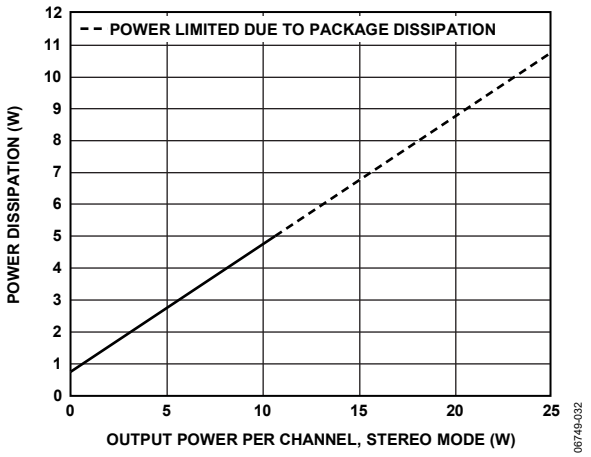


Figure 33. Power Dissipation vs. Output Power, 15 V, 4 Ω, Stereo Mode, Both Channels Driven

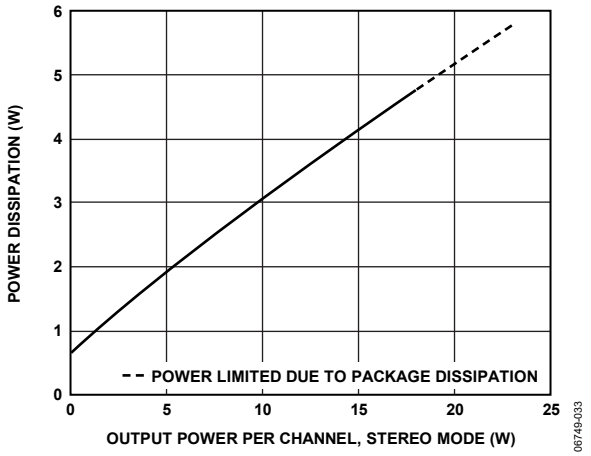


Figure 34. Power Dissipation vs. Output Power, 15 V, 6 Ω, Stereo Mode, Both Channels Driven

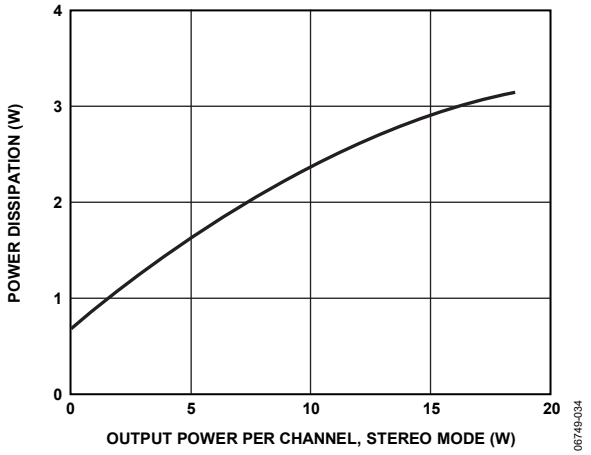


Figure 35. Power Dissipation vs. Output Power, 15 V, 8 Ω, Stereo Mode, Both Channels Driven

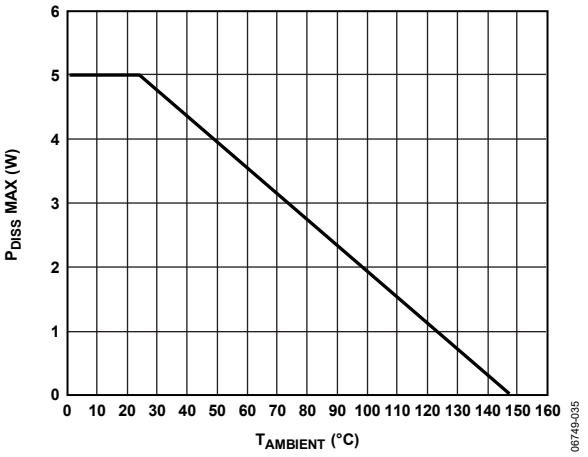


Figure 36. Power Dissipation Derating vs. Ambient Temperature

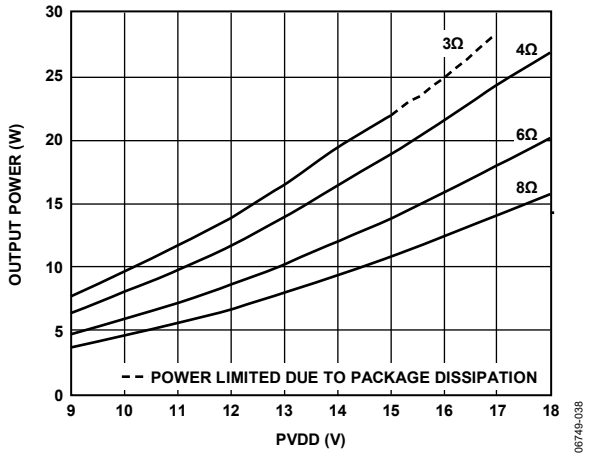


Figure 39. Output Power vs. PVDD, Mono Mode, 60 dB THD + N

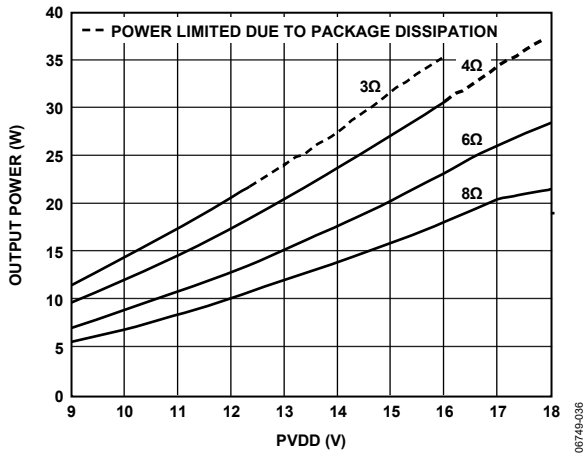


Figure 37. Output Power vs. PVDD, Mono Mode, 20 dB THD + N

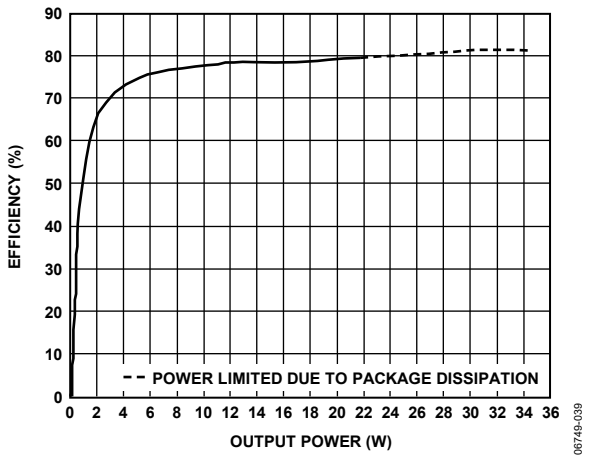


Figure 40. Efficiency vs. Output Power, Mono Mode, 15 V, 3 Ω

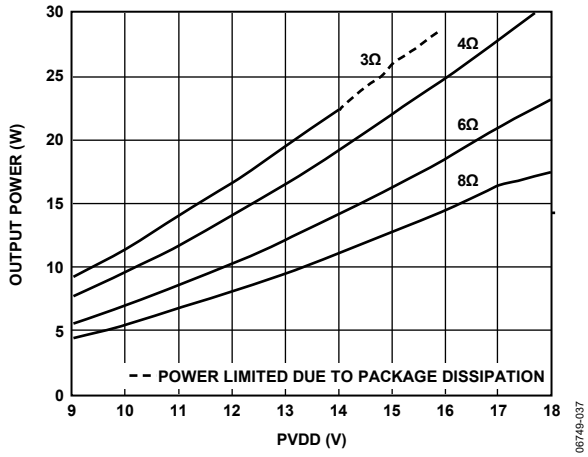


Figure 38. Output Power vs. PVDD, Mono Mode, 40 dB THD + N

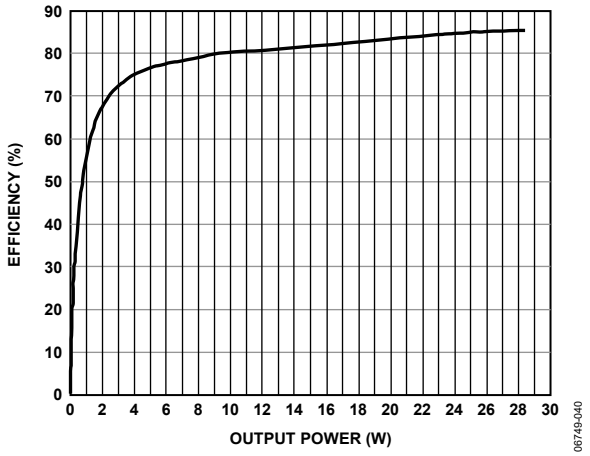


Figure 41. Efficiency vs. Output Power, Mono Mode, 15 V, 4 Ω

THEORY OF OPERATION

OVERVIEW

The ADAU1592 is a 2-channel, high performance switching audio power amplifier. Each of the two Σ-Δ modulators converts a single-ended analog input into a 2-level PDM output. This PDM pulse stream is output from the internal full differential power stage. The ADAU1592 has built-in circuits to suppress the turn-on and turn-off pop and click. The ADAU1592 also offers extensive thermal and overcurrent protection circuits.

MODULATOR

The modulator is a 5th-order Σ-Δ with feedback from the power stage connected internally. This helps reduce the external connections. The 5th-order modulator switches to a lower order near full-scale inputs. The modulator gain is optimized at 19 dB for 15 V operation. The Σ-Δ modulator outputs a pulse density modulation (PDM) 1-bit stream, which does not produce distinct sharp peaks and harmonics in the AM band like conventional fixed-frequency PWM.

The Σ-Δ modulators require feedback to generate PDM stream with respect to the input. The feedback for the modulators comes from the power stage. This helps reduce the nonlinearity in the power stages and achieve excellent THD + N performance. The feedback also helps in achieving good PSRR. In the ADAU1592, the feedback from the power stage is internally connected. This helps reduce the external connections for ease in PCB layout.

The Σ-Δ modulators operate in a discrete time domain and Nyquist frequency limit, which is half the sampling frequency. The modulator uses the master clock of 12.288 MHz. This is generated by dividing the external clock input by 2. This sets the $f_S/2$ around 6.144 MHz. This is sufficient for the audio bandwidth of 22 kHz. The modulator shapes the quantization noise and transfers it outside the audio band. The noise floor rises sharply above 20 kHz. This ensures very good signal-to-noise ratio (SNR) in the audio band of 20 kHz. The 6.144 MHz bandwidth allows the modulator order to be set around the 5th order. The modulator uses proprietary dynamic hysteresis to reduce the switching rate or frequency to around 700 kHz. This reduces the switching losses and achieves good efficiency. The dynamic hysteresis helps the modulator to continuously track the change in PVDD and the input level to keep the modulator stable.

SLICER

The ADAU1592 has a built-in slicer block following the PGA and before the modulator. The slicer block is essentially a hard limiter included for limiting the input signal to the modulator. This, in turn, limits the output power at a given supply voltage. The slicer in the ADAU1592 is normally inactive at lower input levels but is activated as soon as the peak input voltage exceeds the set threshold. The threshold can be set externally by connecting a resistor from SLC_TH (Pin 24) to ground. This feature allows the user to adjust the slicer to the desired value and to limit the output power. For input signals higher than the set threshold, the slicer clips the input signal to the modulator. This adds distortion due to clipping of the signal input to the modulator. This is especially helpful in applications where the output power available needs to be reduced instead of reducing the supply voltage.

Figure 42 is a plot showing THD + N vs. the input level at 0 dB PGA, 15 V, and 6 Ω, and demonstrates the difference between a device with and without the slicer.

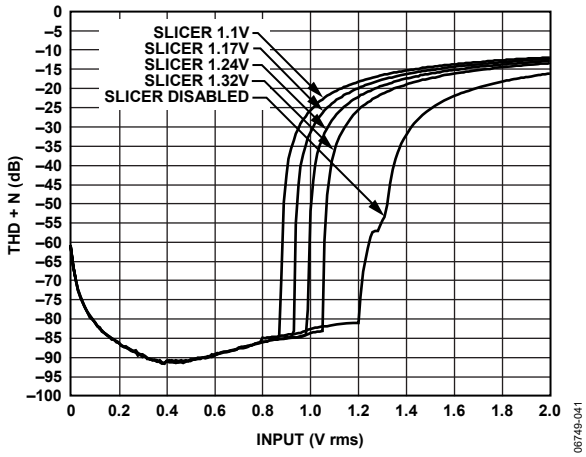


Figure 42. THD + N vs. Input Level @ PGA = 0 dB, 15 V

Figure 43 depicts the typical output power vs. input at different slicer settings.

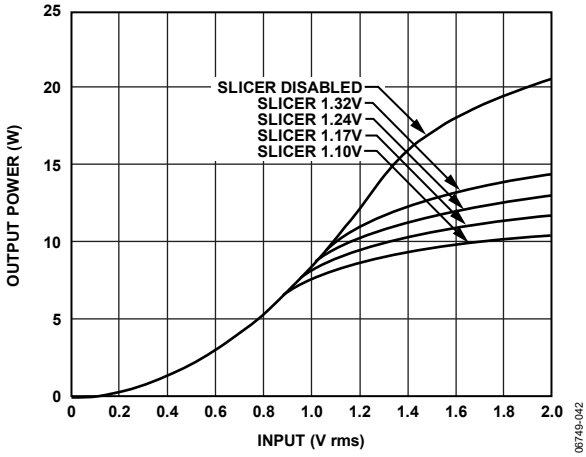


Figure 43. Typical Output Power vs. Input at Different Slicer Settings

From Figure 43, it can be seen that the slicer effectively reduces the output power depending on its setting.

Internally, the slicer block receives the input from the PGA. Figure 44 shows the block for slicer threshold adjust, SLC_TH (Pin 24).

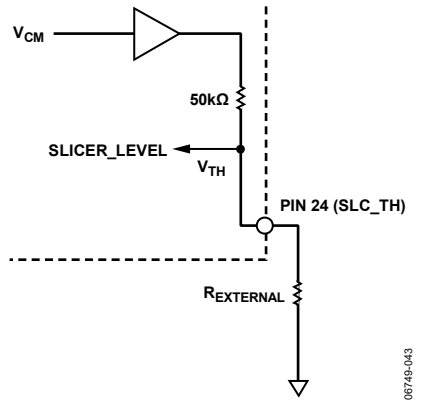


Figure 44. Block for Slicer Threshold Adjust, SLC_TH

The slicer threshold can be set externally using a resistor as follows:

$$V_{TH} = \left(\frac{AVDD}{2}\right) \times \left(\frac{50\ \text{k}\Omega}{50\ \text{k}\Omega + R_{EXTERNAL}}\right)$$

where:
$AVDD$ = 3.3 V typical.
V_{TH} is the voltage threshold at which the slicer is activated.

The following equation can be used to calculate the input signal at which the slicer becomes active:

$$V_{IN\ rms} = \frac{V_{TH}}{1.414 \times 0.9}$$

Therefore, for $AVDD$ = 3.3 V typical and V_{TH} = 1.1 V,

$R_{EXTERNAL}$ = 24.9 kΩ

$V_{IN\ rms}$ = 0.864 V

Thus, the slicer is activated at and above 0.864 $V_{IN\ rms}$.

This feature allows the user to set the slicer and, in turn, reduces the output power at a given supply voltage. To disable the slicer, SLC_TH should be connected directly to AGND. Table 9 shows the typical values for $R_{EXTERNAL}$.

Table 9. Typical $R_{EXTERNAL}$ Values

V_{TH} (V)	$R_{EXTERNAL}$ (kΩ)	$V_{IN\ rms}$ (V)
1.1	24.9	0.864
1.17	20.5	0.919
1.24	16.5	0.974
1.32	12.4	1.037

POWER STAGE

The ADAU1592 power stage comprises a high-side PMOS and a low-side NMOS. The typical $R_{DS\text{-}ON}$ is ~300 mΩ. The PMOS-NMOS stage does not need an external bootstrap capacitor and simplifies the high-side driver design. The power stage also has comprehensive protection circuits to detect the faults in typical applications. See the Protection Circuits section for further details.

GAIN

The gain of the amplifier is set internally using feedback resistors optimized for 15 V nominal operation. The typical gain values are tabulated in Table 1. The typical gain is 19 dB with PGA set to 0 dB. PGA0 (Pin 14) and PGA1 (Pin 13) are used for setting the desired gain.

The gain can be set according to Table 10. Note that the amplifier full-scale input level changes as per the PGA gain setting.

Table 10. Gain Settings

PGA1 (Pin 13)	PGA0 (Pin 14)	PGA Gain (dB)	Amplifier Gain (dB)	Full-Scale Input Level (V_{rms})
0	0	0	19	1
0	1	6	25	0.5
1	0	12	31	0.25
1	1	18	37	0.125

PROTECTION CIRCUITS

The ADAU1592 includes comprehensive protection circuits. It includes thermal warning, thermal overheat, and overcurrent or short-circuit protection on the outputs. The $\overline{\text{ERR}}$ and $\overline{\text{OTW}}$ outputs are open-drain and require external pull-up resistors. The outputs are capable of sinking 10 mA. The open-drain outputs are useful in multichannel applications where more than one ADAU1592 is used. The error outputs of multiple ADAU1592s can be OR'ed to simplify the system design. The logic outputs of the error flags ease the system design of using a microcontroller.

THERMAL PROTECTION

Thermal protection in the ADAU1592 is categorized into two error flags: one as thermal warning and the other as thermal shutdown. When the device junction temperature reaches near 135°C (±5°C), the ADAU1592 outputs a thermal warning error flag by pulling $\overline{\text{OTW}}$ (Pin 10) low. This flag can be used by the microcontroller in the system for indication to the user or can be used to lower the input level to the amplifier to prevent thermal shutdown. The device continues operation until shutdown temperature is reached.

When the device junction temperature exceeds 150°C, the device outputs an error flag by pulling $\overline{\text{ERR}}$ (Pin 9) low. This error flag is latched. To restore the operation, $\overline{\text{MUTE}}$ (Pin 15) needs to be toggled to low and then to high again.

OVERCURRENT PROTECTION

The overcurrent protection in the ADAU1592 is set internally at a 5 A peak output current. The device protects the output devices against excessive output current by pulling $\overline{\text{ERR}}$ (Pin 9) low. This error flag is latched. To restore the normal operation, $\overline{\text{MUTE}}$ (Pin 15) needs to be toggled to low and then to high again. The error flag is useful for the microcontroller in the system to indicate abnormal operation and to initiate the audio $\overline{\text{MUTE}}$ sequence. The device senses the short-circuit condition

on the outputs after the LC filter. Typical short-circuit conditions include shorting of the output load and shorting to either PVDD or PGND.

UNDERVOLTAGE PROTECTION

The ADAU1592 is also comprised of an undervoltage protection circuit, which senses the undervoltage on PVDD. When the PVDD supply goes below the operating threshold, the output FETs are turned to a high-Z condition. In addition, the device issues an error flag by pulling $\overline{\text{ERR}}$ low. This condition is latched. To restore the operation, $\overline{\text{MUTE}}$ (Pin 15) needs to be toggled to low and then to high again.

CLOCK LOSS DETECTION

The ADAU1592 includes a clock loss detection circuit. In case the master clock to the part is lost, the $\overline{\text{ERR}}$ flag is set. This condition is latched. To restore operation, $\overline{\text{MUTE}}$ needs to be toggled low and high again.

AUTOMATIC RECOVERY FROM PROTECTIONS

In certain applications, it is desired for the amplifier to recover itself from thermal protection without the need for system microcontroller intervention.

The ADAU1592 thermal protection circuit issues two error signals for this purpose: one a thermal warning ($\overline{\text{OTW}}$) and the other a thermal shutdown ($\overline{\text{ERR}}$).

With the two error signals, there are two options available for using the protections:

Option 1: Using $\overline{\text{OTW}}$
Option 2: Using $\overline{\text{ERR}}$

The following sections provide further details of these two options.

Option 1: Using $\overline{\text{OTW}}$

The $\overline{\text{OTW}}$ pin is pulled low when the die temperature reaches 130°C to 135°C. This pin can be wired to $\overline{\text{MUTE}}$ as shown in Figure 45, using an RC circuit.

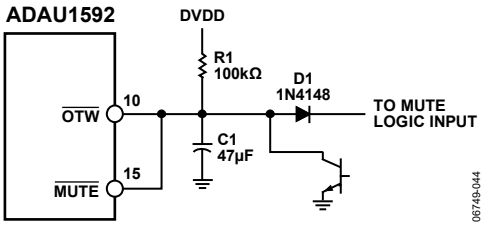


Figure 45. Option 1 Schematic for Autorecovery

The low logic level on $\overline{\text{OTW}}$ also pulls down the $\overline{\text{MUTE}}$ pin. The bridge is shut down and starts cooling or the die temperature starts reducing. When it reaches around 120°C, the $\overline{\text{OTW}}$ signal starts going high. While this pin is tied to a capacitor with a resistor pulled to DVDD, the voltage on this pin starts rising slowly towards DVDD. When it reaches the CMOS threshold, $\overline{\text{MUTE}}$ is deasserted and the amplifier starts functioning again. This cycle repeats itself depending on the input signal conditions and the temperature of the die. This option allows device operation that is safely below the shutdown temperature of 150°C and allows the amplifier to recover itself without the need for microcontroller intervention.

Option 2: Using $\overline{\text{ERR}}$

Option 2 is similar to Option 1 except the $\overline{\text{ERR}}$ pin is tied to $\overline{\text{MUTE}}$ instead of $\overline{\text{OTW}}$. See the circuit in Figure 46.

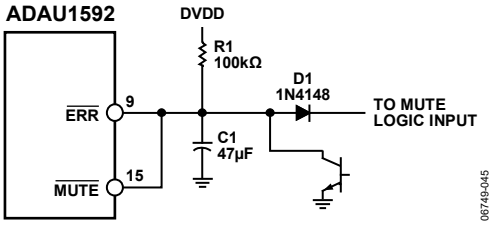


Figure 46. Option 2 Schematic for Autorecovery

In this case, the part goes into shutdown mode due to any of the error-generating events like output overcurrent, overtemperature, missing PVDD or DVDD, or clock loss. The part recovers itself based on the same circuit operation in Figure 45.

However, if the part goes into error mode due to overtemperature, then the device would have reached its maximum limit of 150°C (15°C to 20°C higher than Option 1). If it goes into error mode due to an overcurrent from a short circuit on the speaker outputs, then the part keeps itself recycling on and off until the short circuit is removed.

It is possible that, with this operation, the part is subjected to a much higher temperature and current stress continuously. This, in turn, reduces the part's reliability in the long term. Therefore, using Option 1 for autorecovery from thermal protection and using the system microcontroller to indicate to the user of an error condition is recommended.

$\overline{\text{MUTE}}$ AND $\overline{\text{STDN}}$

The $\overline{\text{MUTE}}$ and $\overline{\text{STDN}}$ pins are 3.3 V logic-compatible inputs used to control the turn-on/turn-off for the ADAU1592.

The $\overline{\text{STDN}}$ input is active low when the $\overline{\text{STDN}}$ pin is pulled low and the device is in its energy saving mode. The modulator is inactive and the power stage is in high-Z state. The high logic level input on the $\overline{\text{STDN}}$ pin wakes up the device. The modulator is running internally but the power stage is still in high-Z state.

When the $\overline{\text{MUTE}}$ pin is pulled high, the power stage becomes active with a soft turn-on to avoid the pop and clicks. The low level on the $\overline{\text{MUTE}}$ pin disables the power stage and is recommended to be used to mute the audio output. See the Power-Up/Power-Down Sequence section for more details.

POWER-UP/POWER-DOWN SEQUENCE

Figure 47 shows the recommended power-up sequence for the ADAU1592.

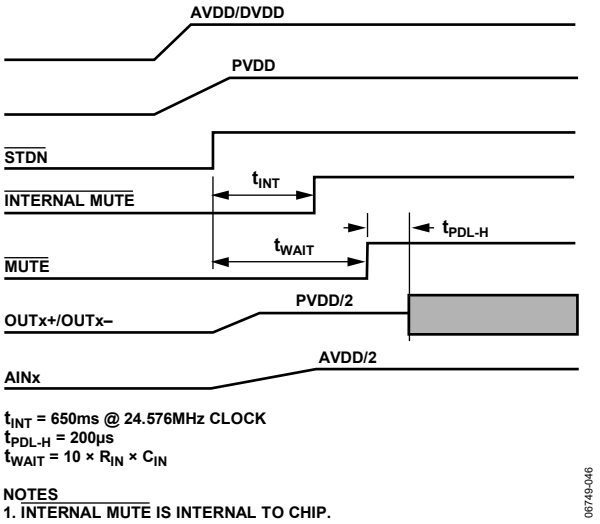


Figure 47. Recommended Power-Up Sequence

The ADAU1592 has a special power-up sequence that consists of a fixed internal mute time during which the power stage does not start switching. This internal mute time depends on the master clock frequency and is 650 ms for a 24.576 MHz clock. Also, the internal mute overrides the external $\overline{\text{MUTE}}$ and ensures that the power stage does not switch on immediately even if the external $\overline{\text{MUTE}}$ signal is pulled high in less than 650 ms after $\overline{\text{STDN}}$. The power stage starts switching only after 650 ms plus a small propagation delay of 200 µs have elapsed and after $\overline{\text{MUTE}}$ is deasserted. Therefore, it is recommended to ensure that $t_{WAIT} > t_{INT}$ to prevent the pop and click during power-up.

Ensure that the $\overline{\text{MUTE}}$ signal is delayed by at least t_{WAIT} seconds after $\overline{\text{STDN}}$. This time is approximately 10 times the charging time constant of the input coupling capacitor.

For example, if the input coupling capacitor is 4.7 µF, the time constant is

$$T = R \times C = 20\ \text{k}\Omega \times 4.7\ \mu\text{F} = 94\ \text{ms}$$

Therefore, $t_{WAIT} = 10 \times T = 940\ \text{ms} \sim 1\ \text{sec}$.

t_{WAIT} is needed to ensure that the input capacitors are charged to AVDD/2 before turning on the power stage.

When $t_{WAIT} < t_{INT}$, the power stage does not start switching until 650 ms have elapsed after $\overline{\text{STDN}}$ (see Figure 48). However, note that this method does not ensure pop-and-click suppression because of less than recommended or insufficient t_{WAIT}.

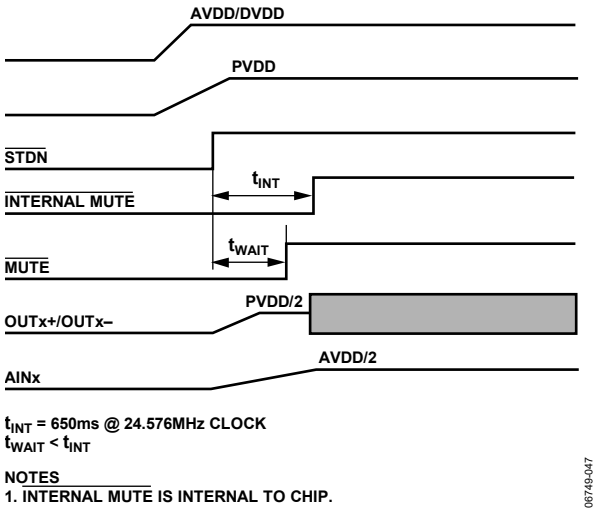


Figure 48. Power-Up Sequence, $t_{WAIT} < t_{INT}$

The ADAU1592 uses three separate supplies: AVDD (3.3 V analog for PGA and modulator), DVDD (3.3 V digital for control logic and clock oscillator), and PVDD (9 V to 18 V power stage and level shifter). Separate pins are provided for the AVDD, DVDD, and PVDD supply connections, as well as AGND, DGND, and PGND.

In addition, the ADAU1592 incorporates a built-in undervoltage lockout logic on DVDD as well as PVDD. This helps detect undervoltage operation and eliminates the need to have an external mechanism to sense the supplies.

The ADAU1592 monitors the DVDD and PVDD supply voltages and prevents the power stage from turning on if either of the supplies is not present or is below the operating threshold. Therefore, if DVDD is missing or below the operating threshold, for example, the power stage does not turn on, even if PVDD is present, or vice versa.

Because this protection is only present on DVDD and PVDD and not on AVDD, shorting both AVDD and DVDD externally or generating AVDD and DVDD from one power source is recommended. This ensures that both AVDD and DVDD supplies are tracking each other and avoids the need to monitor the sequence with respect to PVDD. This also ensures minimal pop and click during power-up.

When using separate AVDD and DVDD supplies, ensure that both supplies are stable before unmuting or turning on the power stage.

Similarly, during shutdown, pulling $\overline{\text{MUTE}}$ to logic low before pulling $\overline{\text{STDN}}$ down is recommended. However, where a fault event occurs, the power stage shuts down to protect the part. In this case, depending on the signal level, there is some pop at the speaker.

To shut down the power supplies to save power, it is highly recommended to mute the amplifier before shutting down any of the supplies. To achieve this, first pull down $\overline{\text{MUTE}}$, then shut down the power supplies in the following order: PVDD, DVDD, and then AVDD. Where AVDD and DVDD are generated from a single source, shut down PVDD before shutting down DVDD and AVDD, and after issuing $\overline{\text{MUTE}}$.

DC OFFSET AND POP NOISE

This section describes the cause of dc offset and pop noise during turn-on/turn-off. The turn-on/turn-off pop in amplifiers depends mainly on the dc offset, therefore, care must be taken to reduce the dc offset at the output.

The first stage of the ADAU1592 has an inverting PGA amplifier, as shown in Figure 49.

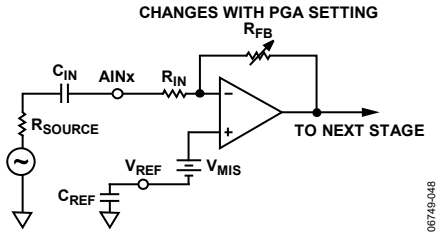


Figure 49. Input Equivalent Circuit

where:
R_{IN} = 20 kΩ, fixed internally.
R_{FB} is the gain feedback resistor (value depends on the PGA setting).
R_{SOURCE} is the source resistance.
C_{IN} is the input coupling capacitor (2.2 µF typical).
C_{REF} is the filter capacitor for V_{REF}.
V_{REF} is the analog reference voltage (AVDD/2 typical).
V_{MIS} is the dc offset due to mismatch in the op amp.

As shown in Figure 49, the dc offset at the output can be due to V_{MIS} (the dc offset from mismatch in the op amp) and due to leakage current of the C_{IN} capacitor.

Normally, the offset due to leakage current in the C_{IN} is less and can be ignored compared to V_{MIS}. The V_{MIS} is mainly responsible for the dc offset at the output. The ADAU1592 uses special self-calibration or a dc offset trim circuit, which controls the dc offset (due to V_{MIS}) to within ±3 mV. The V_{MIS} can vary for each part as well as for voltage and temperature. The trim circuit ensures that the offset is limited within specified limits and provides virtually pop-free operation every time the part is turned on. However, care must be taken while unmuting or during the power-up sequence.

During the initial power-up, C_{IN} and C_{REF} are charging to AVDD/2 and, during this time, there can be dc offset at the output (see Figure 49). This depends on the PGA gain setting. The dc offset is multiplied by the PGA gain setting. If the amplifier is kept in mute during this charging and self-trimming event for the recommended t_{WAIT} time, the dc offset at the output remains within ±3 mV. For more details on t_{WAIT}, refer to the Power-Up/Power-Down Sequence section.

The amount of pop at the turn-on depends on t_{WAIT}, which in turn depends on the values of C_{REF} and C_{IN}. The following section describes how to select the value for the C_{REF} and C_{IN}.

SELECTING VALUES FOR C_{REF} AND C_{IN}

C_{REF} is the capacitor used for filtering the noise from AVDD on V_{REF}. V_{REF} is used for the biasing of the internal analog amplifier as well as the modulator. Therefore, care must be taken to ensure that the recommended minimum value is used. The minimum recommended value for C_{REF} is 4.7 µF.

C_{IN} is the input coupling capacitor and is used to decouple the inputs from the external dc. The C_{IN} value determines the low corner frequency of the amplifier. It can be determined from the following equation:

$$f_{LOW} = \frac{1}{2 \times \pi \times R_{IN} \times C_{IN}}$$

where:
f_{LOW} is the low corner frequency (−3 dB).
R_{IN} is the input resistance (20 kΩ).
C_{IN} is the input coupling capacitor.

Note that R_{IN} = 20 kΩ and R_{SOURCE} < 1 kΩ. If R_{SOURCE} is sizable with respect to R_{IN}, it also must be taken into account in calculation.

From the preceding equation, f_{LOW} can be found for the desired frequency response.

The recommended value for C_{IN} is 2.2 µF, giving f_{LOW} = 3.6 Hz, and should keep 20 Hz roll-off within −0.5 dB.

However, if a higher than recommended C_{IN} value is used for better low frequency response, care must be taken to ensure that appropriate t_{WAIT} is used. See the Power-Up/Power-Down Sequence section for more details.

MONO MODE

The ADAU1592 mono mode can be enabled by pulling MO/$\overline{\text{ST}}$ (Pin 11) to logic high. In this mode, the left channel input and modulator are active and feed PWM data to both the left and right power stages. However, the respective power FETs need to be connected externally for higher current capability. That is, connect OUTL+ with OUTR+ and OUTL− with OUTR−. The mono mode gives the capability to drive lower impedance loads without invoking current limit. However, the output power is limited by PVDD and temperature limits. See the typical application schematic in Figure 51 for details.

POWER SUPPLY DECOUPLING

Because Class-D amplifiers utilize high frequency switching, care must be taken for power supply decoupling.

For reliable operation, using 100 nF ceramic surface-mount capacitors for the PVDD and PGND pins is recommended. A minimum of two capacitors is needed: one between Pin 45/Pin 46 (PVDD) and Pin 47/Pin48 (PGND), the other between Pin 39/Pin 40 (PVDD) and Pin 37/Pin 38 (PGND). In addition, these

capacitors must be placed very close to their respective pins with direct connection. This is important for reliable and safe operation of the device. One additional 1 µF capacitor in parallel to the 100 nF capacitor is also recommended. A bulk bypass capacitor of 470 µF is also recommended to remove the low frequency ripple due to load current.

Similarly, one 100 nF capacitor is recommended between each DVDD/DGND and AVDD/AGND. These capacitors also must be placed close to their respective pins with direct connection.

EXTERNAL PROTECTION FOR PVDD > 15 V

As the PVDD supply voltage approaches 15 V and above, the available headroom with maximum PVDD is reduced. As with any switching amplifier, the outputs swing to full rail and the amount of overshoot due to parasitic elements of the package/board is significant. Therefore, for reliable and safe operation, it is recommended that external protection circuits be added for applications that require supply voltages >15 V. The use of an RC snubber or a Schottky diode on the outputs should be considered.

The RC snubber should be connected between the OUTx+ pin and the OUTx– pin for each channel. The typical recommended values are 10 Ω and 680 pF. Also, both components must be placed close to the output pins. For two channels, two resistors and two capacitors are needed.

If Schottky diodes are preferred, the diodes must be from each OUTx–/OUTx+ pin to PVDD/PGND. Therefore, a total of eight diodes is required for two channels. The Schottky diodes must be placed close to the output pins to be effective.

CLOCK

The ADAU1592 uses 24.576 MHz for the master clock, which is 512 × f_S (f_S = 48 kHz). There are several options for providing the clock.

Option 1: Using a Quartz Crystal

A quartz crystal of 24.576 MHz frequency can be connected between the XTI and XTO pins using two load capacitors suitable for the crystal oscillation mode.

Option 2: Using a Ceramic Resonator

The ADAU1592 can also be used with ceramic resonators similar to crystal by using the XTI and XTO pins.

Option 3: Using an External Clock

The ADAU1592 can be provided with an external clock of 24.576 MHz at the XTI pin. The logic level for the clock input should be in the range of 3.3 V and 50% typical duty cycle.

For systems using multiple ADAU1592s, it is recommended to use only one clock source if the ADAU1592s share the same power supply to prevent the beat frequencies of asynchronous clocks from appearing in the audio band.

Multiple ADAU1592s can be connected in a daisy chain by providing or generating a master clock from one ADAU1592 and subsequently connecting its XTO output to the XTI input of the next ADAU1592, and so on. However, using a simple logic buffer from the XTO pin of one ADAU1592 to the XTI pin of the next ADAU1592 is recommended. Because the clock output is now buffered, it can be connected to the XTI inputs of the remaining ADAU1592s, depending on the fanout capability of the logic buffer used.

APPLICATIONS INFORMATION

For applications with PVDD > 15 V, add components R1 and R2 (10 Ω typical), C5 and C6 (680 pF typical), and D1 through D8 (CRS01/02).

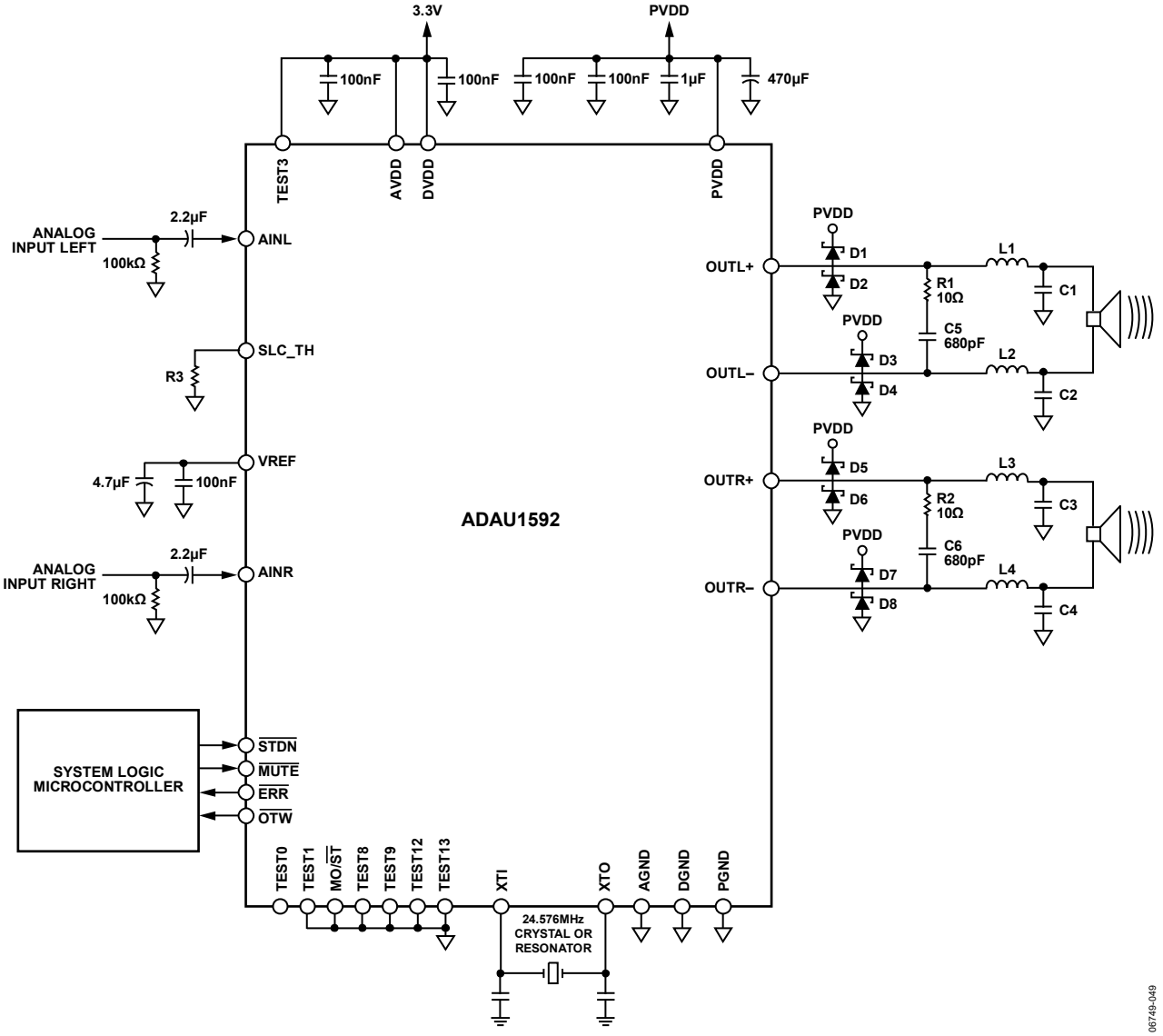


Figure 50. Typical Stereo Application Circuit

Table 11. R3—Slicer Threshold Resistor

V_{TH} (V)	R3 (kΩ)
1.1	24.9
1.17	20.5
1.24	16.5
1.32	12.4

Table 12. Output Filter Component Values

Load Impedance (Ω)	Inductance L1 to L4 (µH)	Capacitance C1 to C4 (µF)
4	10	1.5
6	15	1
8	22	0.68

For applications with PVDD > 15 V, add components R1 (10 Ω typical), C5 (680 pF typical), and D1 through D4 (CRS01/02).

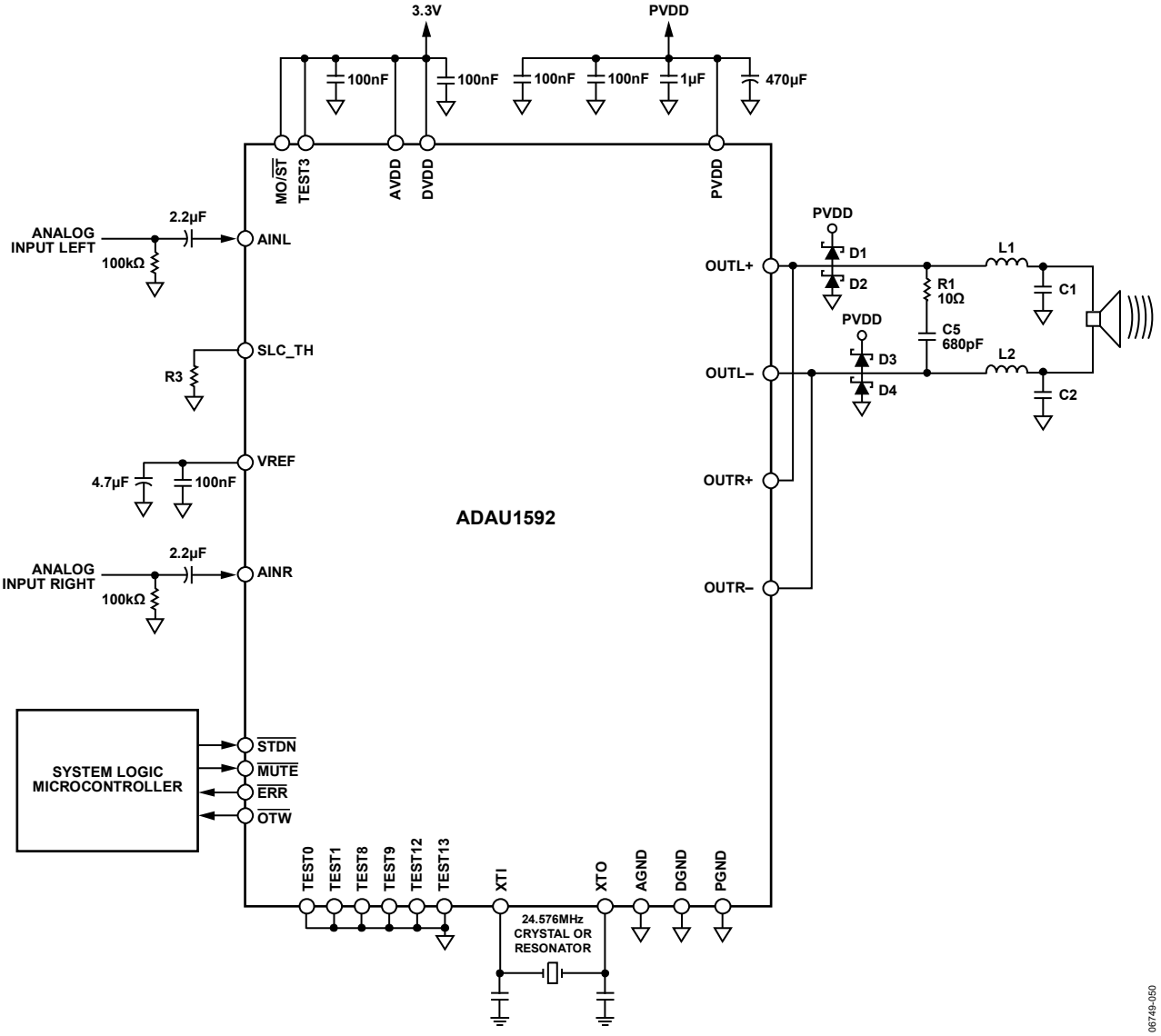


Figure 51. Typical Mono Application Circuit

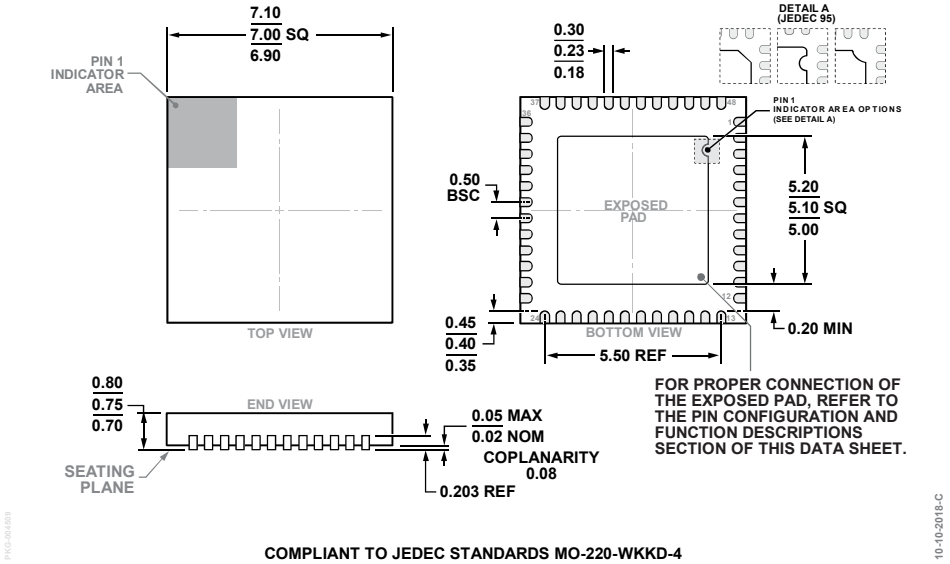
Table 13. R3—Slicer Threshold Resistor

V_{TH} (V)	R3 (kΩ)
1.1	24.9
1.17	20.5
1.24	16.5
1.32	12.4

Table 14. Output Filter Component Values

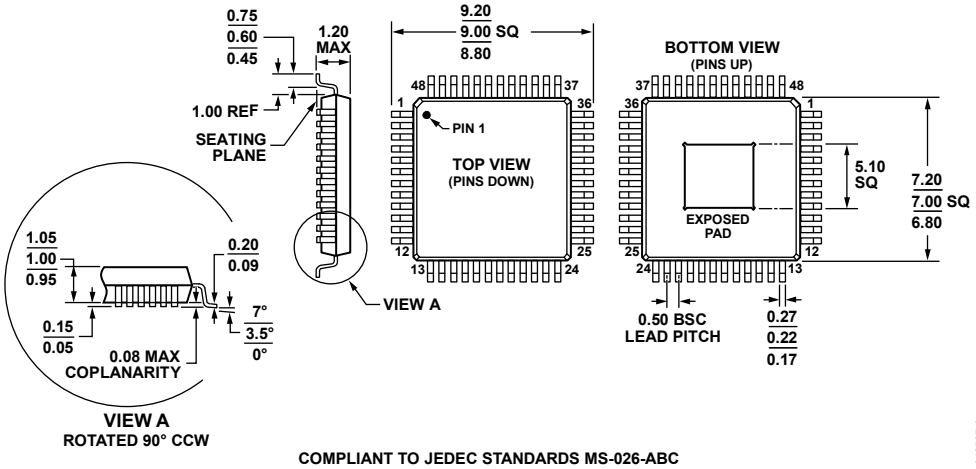
Load Impedance (Ω)	Inductance L1 and L2 (µH)	Capacitance C1 and C2 (µF)
4	10	1.5
6	15	1
8	22	0.68

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD-4

Figure 52. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-4)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-ABC

Figure 53. 48-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-48-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADAU1592ACPZ[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-4
ADAU1592ACPZ-RL[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP], 13" Tape and Reel	CP-48-4
ADAU1592ACPZ-RL7[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP], 7" Tape and Reel	CP-48-4
ADAU1592ASVZ[1]	−40°C to +85°C	48-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-48-5
ADAU1592ASVZ-RL[1]	−40°C to +85°C	48-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP], 13" Tape and Reel	SV-48-5
ADAU1592ASVZ-RL7[1]	−40°C to +85°C	48-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP], 7" Tape and Reel	SV-48-5
EVAL-ADAU1592EBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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