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4/2006—Revision 0: Initial Version

SPECIFICATIONS

V_S+ = 15 V, V_S- = −15 V, V_{REF} = 0 V, T_A = 25°C, T_{OPR} = −40°C to +85°C for A and B grades. T_{OPR} = −40°C to +125°C for W grade, G = 1, R_L = 2 kΩ[1], unless otherwise noted.

Table 1.

		A Grade			B Grade			W Grade			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
COMMON-MODE REJECTION RATIO (CMRR)	T_A for A, B grades, T_{OPR} for W grade										
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = ±10 V										
G = 1		78			86			77			dB
G = 10		94			100			92			dB
G = 100		94			100			92			dB
G = 1000		94			100			92			dB
CMRR at 5 kHz	V_{CM} = ±10 V										
G = 1		74			80			72			dB
G = 10		84			90			80			dB
G = 100		84			90			80			dB
G = 1000		84			90			80			dB
NOISE	RTI noise = $\sqrt{(e_{ni}^2 + (e_{no}/G)^2)}$, T_A										
Voltage Noise, 1 kHz											
Input Voltage Noise, e_{ni}	$V_{IN}+$, $V_{IN}-$ = 0 V		14			14	17		14		nV/√Hz
Output Voltage Noise, e_{no}	$V_{IN}+$, $V_{IN}-$ = 0 V		90			90	100		90		nV/√Hz
RTI, 0.1 Hz to 10 Hz											
G = 1			5			5			5		µV p-p
G = 1000			0.8			0.8			0.8		µV p-p
Current Noise	f = 1 kHz		1			1			1		fA/√Hz
VOLTAGE OFFSET	$V_{OS} = V_{OSI} + V_{OSO}/G$										
Input Offset, V_{OSI}	T_A	−250		+250	−125		+125	−250		+250	µV
Average TC	T_{OPR}	−10		+10	−5		+5	−10		+10	µV/°C
Output Offset, V_{OSO}	T_A	−750		+750	−500		+500	−750		+750	µV
Average TC	T_{OPR}	−10		+10	−5		+5	−10		+10	µV/°C
Offset RTI vs. Supply (PSR)	V_S = ±5 V to ±15 V, T_A for A, B grades, T_{OPR} for W grade										
G = 1		86			86			80			dB
G = 10		96			100			92			dB
G = 100		96			100			92			dB
G = 1000		96			100			92			dB
INPUT CURRENT											
Input Bias Current	T_A			25			10			25	pA
Over Temperature	T_{OPR}		0.3			0.3				100	nA
Input Offset Current	T_A			2			0.6			2	pA
Over Temperature	T_{OPR}		0.005			0.005				10	nA
DYNAMIC RESPONSE											
Small Signal Bandwidth, −3 dB	T_A										
G = 1			1500			1500			1500		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			14			14			14		kHz

Parameter	Test Conditions	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	W Grade Min	W Grade Typ	W Grade Max	Unit
Settling Time 0.01%	10 V step, T_A										
G = 1			5			5			5		µs
G = 10			4.3			4.3			4.3		µs
G = 100			8.1			8.1			8.1		µs
G = 1000			58			58			58		µs
Settling Time 0.001%	10 V step, T_A										
G = 1			6			6			6		µs
G = 10			4.6			4.6			4.6		µs
G = 100			9.6			9.6			9.6		µs
G = 1000			74			74			74		µs
Slew Rate											
G = 1 to 100	T_A	2			2			2			V/µs
GAIN	G = 1 + (49.4 kΩ/R_G), T_A for A, B grades, T_{OPR} for W grade										
Gain Range		1		1000	1		1000	1		1000	V/V
Gain Error	V_{OUT} = ±10 V										
G = 1		−0.06		+0.06	−0.04		+0.04	−0.1		+0.1	%
G = 10		−0.3		+0.3	−0.2		+0.2	−0.8		+0.8	%
G = 100		−0.3		+0.3	−0.2		+0.2	−0.8		+0.8	%
G = 1000		−0.3		+0.3	−0.2		+0.2	−0.8		+0.8	%
Gain Nonlinearity	V_{OUT} = −10 V to +10 V, T_A										
G = 1	R_L = 10 kΩ		10	15		10	15		10	15	ppm
G = 10	R_L = 10 kΩ		5	10		5	10		5	10	ppm
G = 100	R_L = 10 kΩ		30	60		30	60		30	60	ppm
G = 1000	R_L = 10 kΩ		400	500		400	500		400	500	ppm
G = 1	R_L = 2 kΩ		10	15		10	15		10	15	ppm
G = 10	R_L = 2 kΩ		10	15		10	15		10	15	ppm
G = 100	R_L = 2 kΩ		50	75		50	75		50	75	ppm
Gain vs. Temperature											
G = 1			3	10		2	5		3	10	ppm/°C
G > 10				−50			−50			−50	ppm/°C
INPUT											
Impedance (Pin to Ground)[2]	T_A		10^4‖5			10^4‖5			10^4‖5		GΩ‖pF
Input Operating Voltage Range[3]	V_S = ±2.25 V to ±18 V for dual supplies	$-V_S$ + 0.1		$+V_S$ − 2	$-V_S$ + 0.1		$+V_S$ − 2	$-V_S$ + 0.1		$+V_S$ − 2	V
Over Temperature	T_{OPR}	$-V_S$ + 0.1		$+V_S$ − 2.1	$-V_S$ + 0.1		$+V_S$ − 2.1	$-V_S$ + 0.1		$+V_S$ − 2.2	V
OUTPUT											
Output Swing	R_L = 10 kΩ, T_A	−14.7		+14.7	−14.7		+14.7	−14.7		+14.7	V
Over Temperature	T_{OPR}	−14.6		+14.6	−14.6		+14.6	−14.3		+14.3	V
Short-Circuit Current	T_A		15			15			15		mA
REFERENCE INPUT	T_A										kΩ
R_{IN}			40			40			40		µA
I_{IN}	V_{IN}+, V_{IN}− = 0 V			70			70			70	V
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$			$+V_S$	V/V
Gain to Output	T_A		1 ± 0.0001			1 ± 0.0001				1 ± 0.0001	V/V

Parameter	Test Conditions	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	W Grade Min	W Grade Typ	W Grade Max	Unit
POWER SUPPLY											
Operating Range		±2.25[4]		±18	±2.25[4]		±18	±2.25[4]		±18	V
Quiescent Current	T_A			750			750			750	μA
Over Temperature	T_{OPR}			850			850			1000	μA
TEMPERATURE RANGE											
For Specified Performance	T_{OPR}	−40		+85	−40		+85	−40		+125	°C

[1] When the output sinks more than 4 mA, use a 47 pF capacitor in parallel with the load to prevent ringing. Otherwise, use a larger load, such as 10 kΩ.
[2] Differential and common-mode input impedance can be calculated from the pin impedance: $Z_{DIFF} = 2(Z_{PIN})$; $Z_{CM} = Z_{PIN}/2$.
[3] The AD8220 can operate up to a diode drop below the negative supply but the bias current increases sharply. The input voltage range reflects the maximum allowable voltage where the input bias current is within the specification.
[4] At this supply voltage, ensure that the input common-mode voltage is within the input voltage range specification.

V_S + = 5 V, V_S− = 0 V, V_{REF} = 2.5 V, T_A = 25°C, T_{OPR} = −40°C to +85°C for A and B grades. T_{OPR} = −40°C to +125°C for W grade, G = 1, R_L = 2 kΩ[1], unless otherwise noted.

Table 2.

Parameter	Test Conditions	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	W Grade Min	W Grade Typ	W Grade Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	T_A for A, B grades, T_{OPR} for W grade										
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = 0 to 2.5 V										
G = 1		78			86			77			dB
G = 10		94			100			92			dB
G = 100		94			100			92			dB
G = 1000		94			100			92			dB
CMRR at 5 kHz	V_{CM} = 0 to 2.5 V										
G = 1		74			80			72			dB
G = 10		84			90			80			dB
G = 100		84			90			80			dB
G = 1000		84			90			80			dB
NOISE	RTI noise = $\sqrt{(e_{ni}^2 + (e_{no}/G)^2)}$, T_A										
Voltage Noise, 1 kHz	V_S = ±2.5 V										
Input Voltage Noise, e_{ni}	V_{IN}+, V_{IN}− = 0 V, V_{REF} = 0 V		14			14	17		14		nV/√Hz
Output Voltage Noise, e_{no}	V_{IN}+, V_{IN}− = 0 V, V_{REF} = 0 V		90			90	100		90		nV/√Hz
RTI, 0.1 Hz to 10 Hz											
G = 1			5			5			5		μV p-p
G = 1000			0.8			0.8			0.8		μV p-p
Current Noise	f = 1 kHz		1			1			1		fA/√Hz
VOLTAGE OFFSET	$V_{OS} = V_{OSI} + V_{OSO}/G$										
Input Offset, V_{OSI}	T_A	−300		+300	−200		+200	−300		+300	μV
Average TC	T_{OPR}	−10		+10	−5		+5	−10		10	μV/°C
Output Offset, V_{OSO}	T_A	−800		+800	−600		+600	−800		+800	μV
Average TC	T_{OPR}	−10		+10	−5		+5	−10		+10	μV/°C
Offset RTI vs. Supply (PSR)	T_A for A, B grades, T_{OPR} for W grade										
G = 1		86			86			80			dB
G = 10		96			100			92			dB
G = 100		96			100			92			dB
G = 1000		96			100			92			dB

Parameter	Test Conditions	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	W Grade Min	W Grade Typ	W Grade Max	Unit
INPUT CURRENT											
Input Bias Current	T_A			25			10			25	pA
Over Temperature	T_{OPR}		0.3			0.3				100	nA
Input Offset Current	T_A			2			0.6			2	pA
Over Temperature	T_{OPR}		0.005			0.005				10	nA
DYNAMIC RESPONSE	T_A										
Small Signal Bandwidth, −3 dB											
G = 1			1500			1500			1500		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			14			14			14		kHz
Settling Time 0.01%	T_A										
G = 1	3 V step		2.5			2.5			2.5		µs
G = 10	4 V step		2.5			2.5			2.5		µs
G = 100	4 V step		7.5			7.5			7.5		µs
G = 1000	4 V step		30			30			30		µs
Settling Time 0.001%	T_A										
G = 1	3 V step		3.5			3.5			3.5		µs
G = 10	4 V step		3.5			3.5			3.5		µs
G = 100	4 V step		8.5			8.5			8.5		µs
G = 1000	4 V step		37			37			37		µs
Slew Rate											
G = 1 to 100	T_A	2			2			2			V/µs
GAIN	G = 1 + (49.4 kΩ/R_G), T_A for A, B grades, T_{OPR} for W grade										
Gain Range		1		1000	1		1000	1		1000	V/V
Gain Error	V_{OUT} = 0.3 V to 2.9 V for G = 1, V_{OUT} = 0.3 V to 3.8 V for G > 1										
G = 1		−0.06		+0.06	−0.04		+0.04	−0.1		+0.1	%
G = 10		−0.3		+0.3	−0.2		+0.2	−0.8		+0.8	%
G = 100		−0.3		+0.3	−0.2		+0.2	−0.8		+0.8	%
G = 1000		−0.3		+0.3	−0.2		+0.2	−0.8		+0.8	%
Nonlinearity	V_{OUT} = 0.3 V to 2.9 V for G = 1, V_{OUT} = 0.3 V to 3.8 V for G > 1, T_A										
G = 1	R_L = 10 kΩ		35	50		35	50			50	ppm
G = 10	R_L = 10 kΩ		35	50		35	50			50	ppm
G = 100	R_L = 10 kΩ		50	75		50	75			75	ppm
G = 1000	R_L = 10 kΩ		650	750		650	750			750	ppm
G = 1	R_L = 2 kΩ		35	50		35	50			50	ppm
G = 10	R_L = 2 kΩ		35	50		35	50			50	ppm
G = 100	R_L = 2 kΩ		50	75		50	75			75	ppm
Gain vs. Temperature											
G = 1			3	10		2	5		3	10	ppm/°C
G > 10				−50			−50			−50	ppm/°C
INPUT											
Impedance (Pin to Ground)[2]	T_A		10^4‖6			10^4‖6			10^4‖6		GΩ‖pF
Input Voltage Range[3]	T_A	−0.1		$+V_S$ − 2	−0.1		$+V_S$ − 2				V
Over Temperature	T_{OPR}	−0.1		$+V_S$ − 2.1	−0.1		$+V_S$ − 2.1	−0.1		$+V_S$ − 2.2	V

Parameter	Test Conditions	A Grade			B Grade			W Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT											
Output Swing	R_L = 10 kΩ	0.15		4.85	0.15		4.85	0.15		4.85	V
Over Temperature	T_{OPR}	0.2		4.80	0.2		4.80	0.3		4.70	V
Short-Circuit Current			15			15			15		mA
REFERENCE INPUT	T_A										
R_{IN}			40			40			40		kΩ
I_{IN}	V_{IN}+, V_{IN}− = 0 V			70			70			70	μA
Voltage Range		−V_S		+V_S	−V_S		+V_S	−V_S		+V_S	V
Gain to Output	T_A		1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		V/V
POWER SUPPLY											
Operating Range		4.5		36	4.5		36	4.5		36	V
Quiescent Current	T_A			750			750			750	μA
Over Temperature	T_{OPR}			850			850			1000	μA
TEMPERATURE RANGE											
T_{OPR}, For Specified Performance	T_{OPR}	−40		+85	−40		+85	−40		+125	°C

[1] When the output sinks more than 4 mA, use a 47 pF capacitor in parallel with the load to prevent ringing. Otherwise, use a larger load, such as 10 kΩ.
[2] Differential and common-mode impedance can be calculated from the pin impedance: $Z_{DIFF} = 2(Z_{PIN})$; $Z_{CM} = Z_{PIN}/2$.
[3] The AD8220 can operate up to a diode drop below the negative supply but the bias current increases sharply. The input voltage range reflects the maximum allowable voltage where the input bias current is within the specification.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Power Dissipation	See Figure 3
Output Short-Circuit Current	Indefinite[1]
Input Voltage (Common Mode)	±Vs
Differential Input Voltage	±Vs
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range[2]	−40°C to +125°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	140°C
θ_{JA} (4-Layer JEDEC Standard Board)	135°C/W
Package Glass Transition Temperature	140°C
ESD (Human Body Model)	4 kV
ESD (Charge Device Model)	1 kV
ESD (Machine Model)	0.4 kV

[1] Assumes the load is referenced to midsupply.
[2] Temperature for specified performance is −40°C to +85°C. For performance to 125°C, see the Typical Performance Characteristics section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the MSOP on a 4-layer JEDEC standard board. θ_{JA} values are approximations.

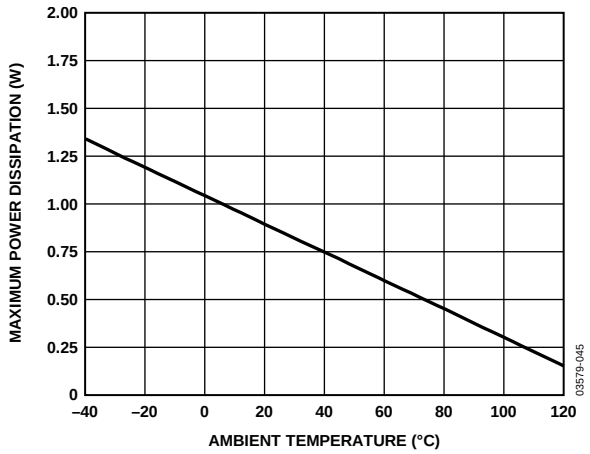

Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

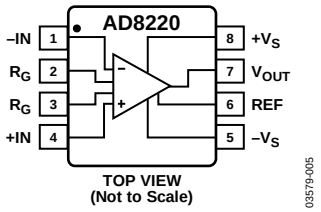

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	–IN	Negative Input Terminal (True Differential Input)
2, 3	R_G	Gain Setting Terminals (Place Resistor Across the R_G Pins)
4	+IN	Positive Input Terminal (True Differential Input)
5	$-V_S$	Negative Power Supply Terminal
6	REF	Reference Voltage Terminal (Drive This Terminal with a Low Impedance Voltage Source to Level-Shift the Output)
7	V_{OUT}	Output Terminal
8	$+V_S$	Positive Power Supply Terminal

TYPICAL PERFORMANCE CHARACTERISTICS

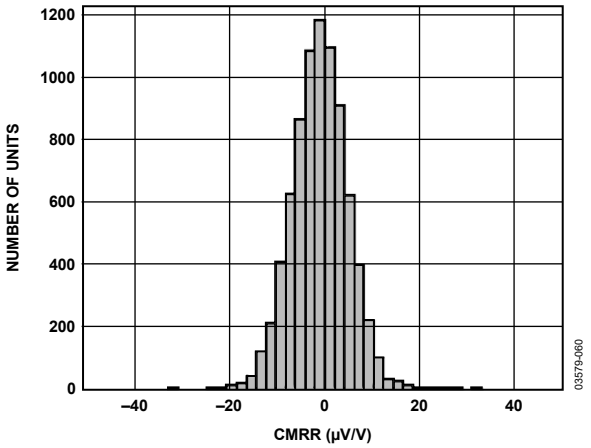

Figure 5. Typical Distribution of CMRR (G = 1)

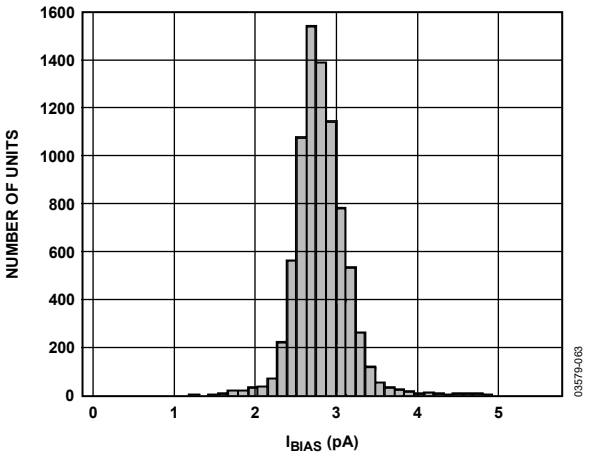

Figure 8. Typical Distribution of Input Bias Current

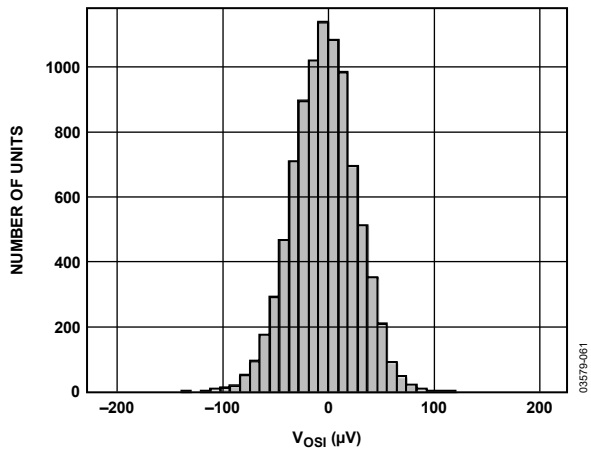

Figure 6. Typical Distribution of Input Offset Voltage

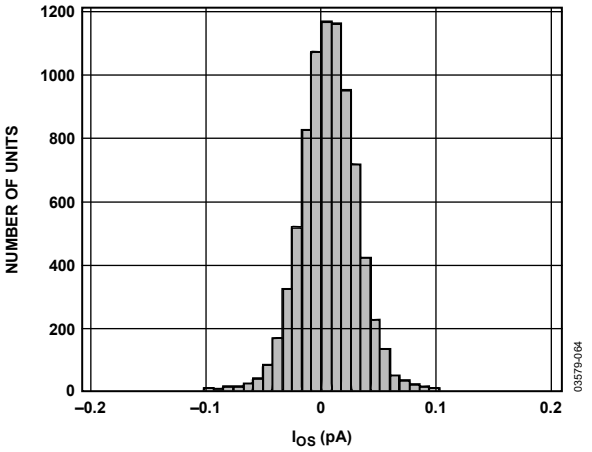

Figure 9. Typical Distribution of Input Offset Current

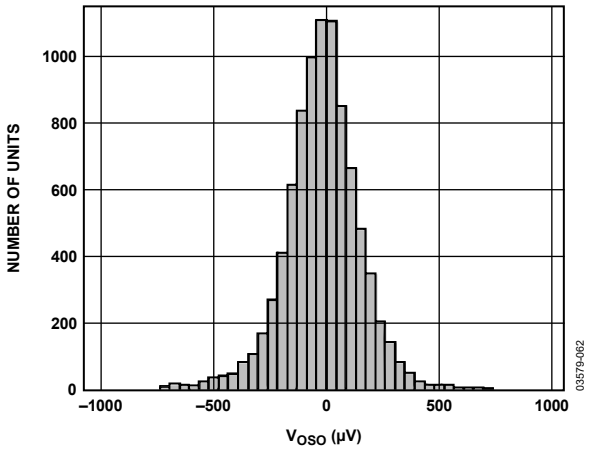

Figure 7. Typical Distribution of Output Offset Voltage

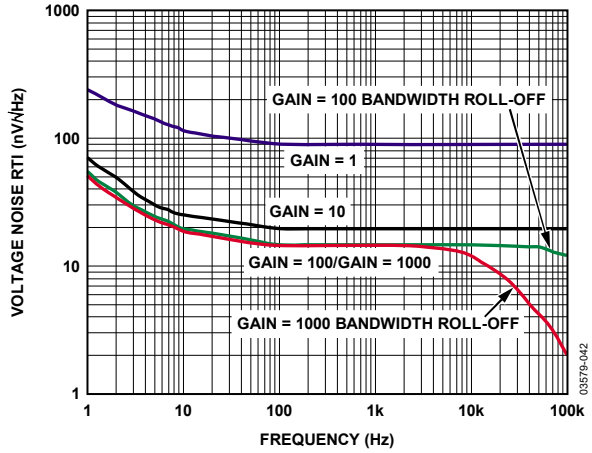

Figure 10. Voltage Spectral Density vs. Frequency

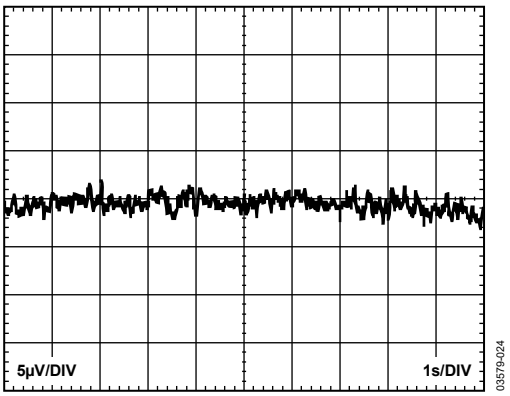

Figure 11. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1)

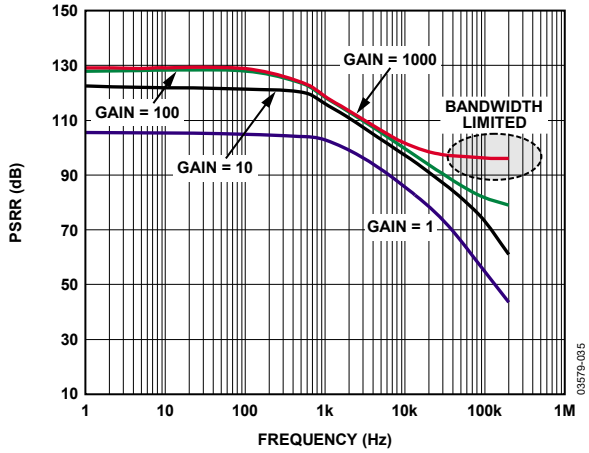

Figure 14. Positive PSRR vs. Frequency, RTI

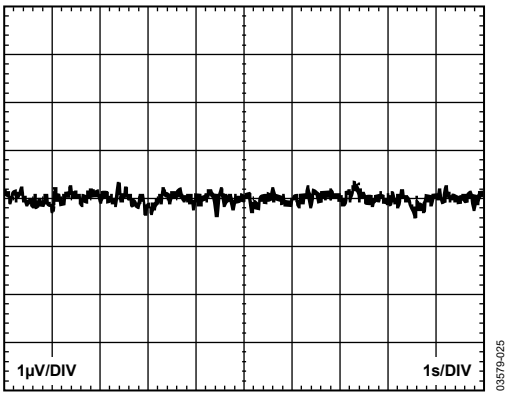

Figure 12. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1000)

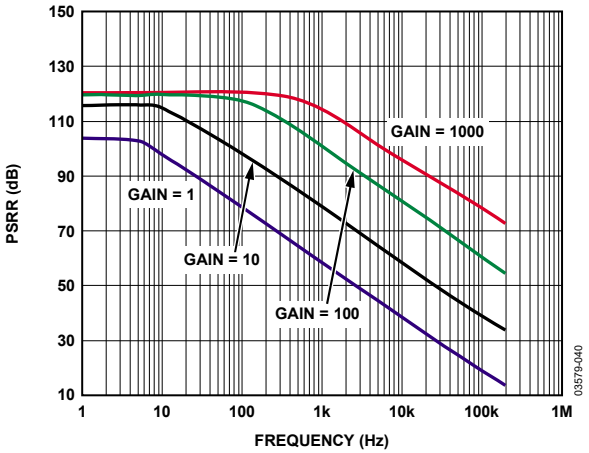

Figure 15. Negative PSRR vs. Frequency, RTI

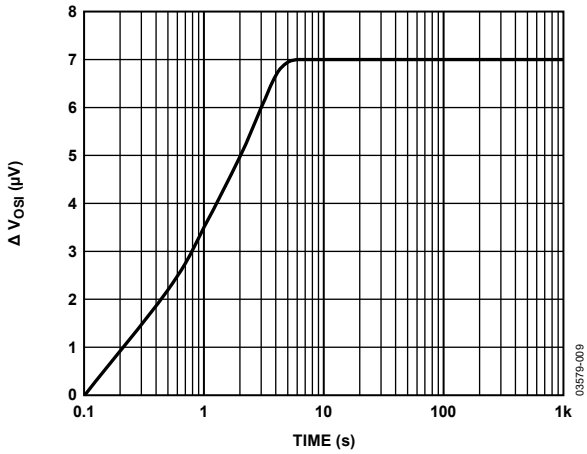

Figure 13. Change in Input Offset Voltage vs. Warmup Time

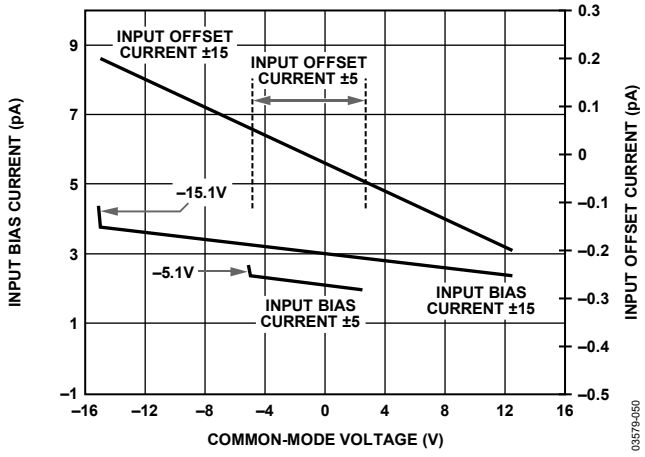

Figure 16. Input Bias Current and Input Offset Current vs. Common-Mode Voltage

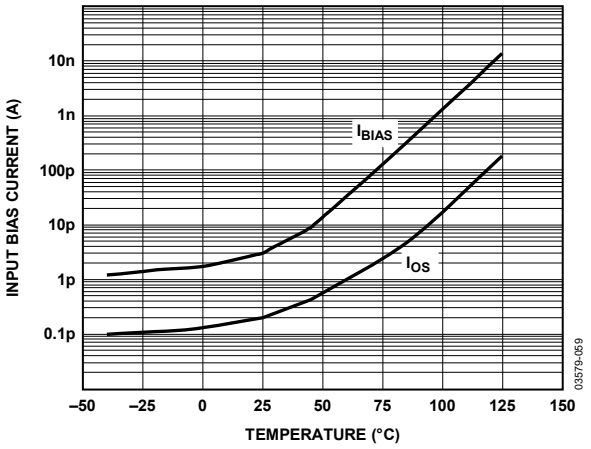

Figure 17. Input Bias Current and Offset Current vs. Temperature, $V_S = \pm 15$ V, $V_{REF} = 0$ V

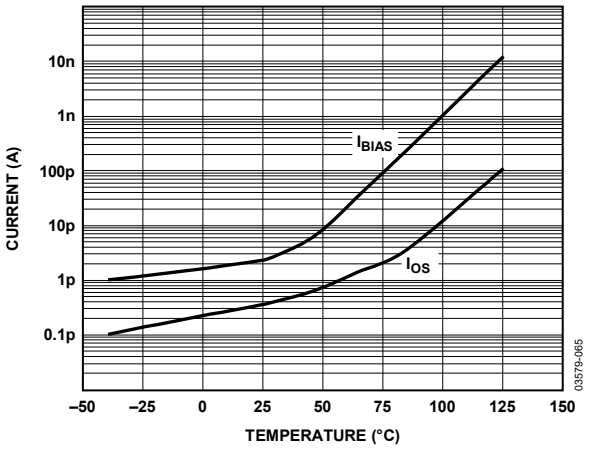

Figure 18. Input Bias Current and Offset Current vs. Temperature, $V_S = +5$ V, $V_{REF} = 2.5$ V

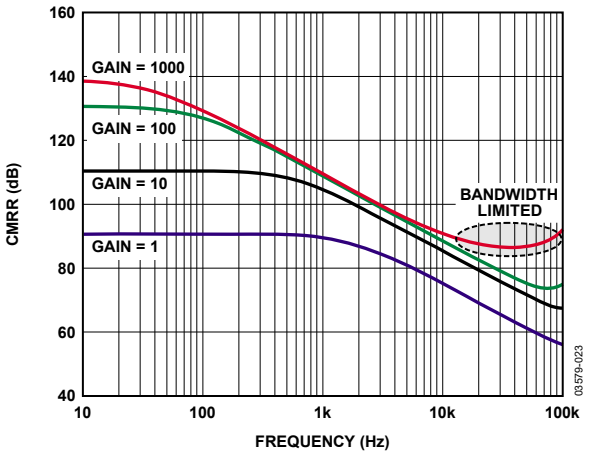

Figure 19. CMRR vs. Frequency

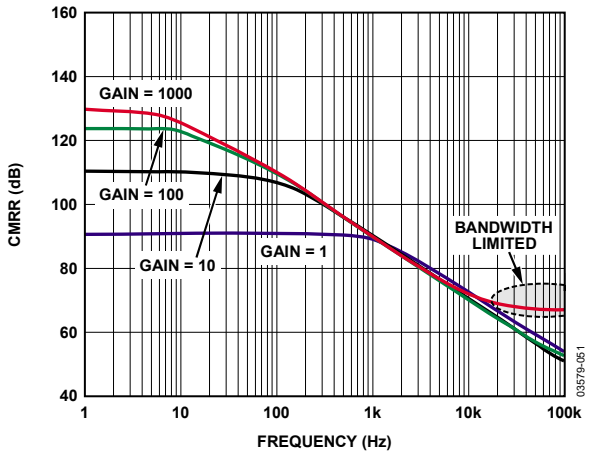

Figure 20. CMRR vs. Frequency, 1 kΩ Source Imbalance

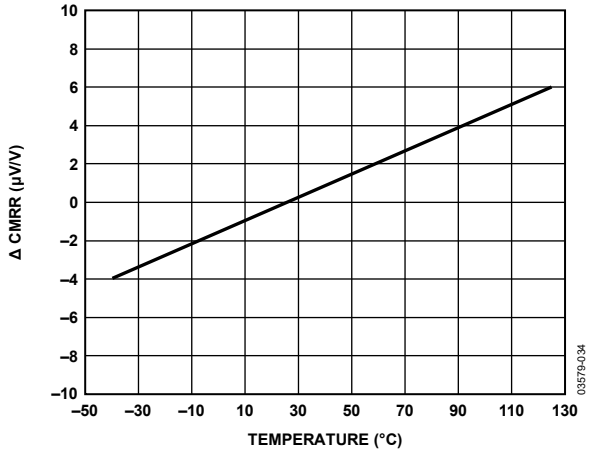

Figure 21. Change in CMRR vs. Temperature, G = 1

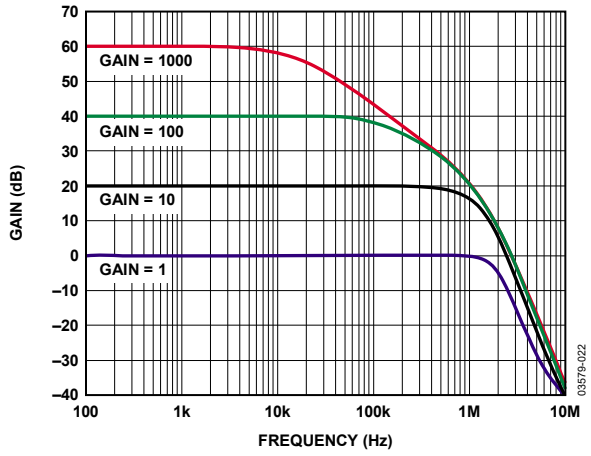

Figure 22. Gain vs. Frequency

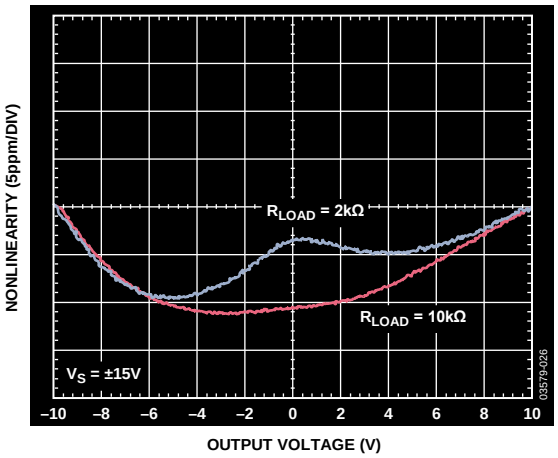

Figure 23. Gain Nonlinearity, G = 1

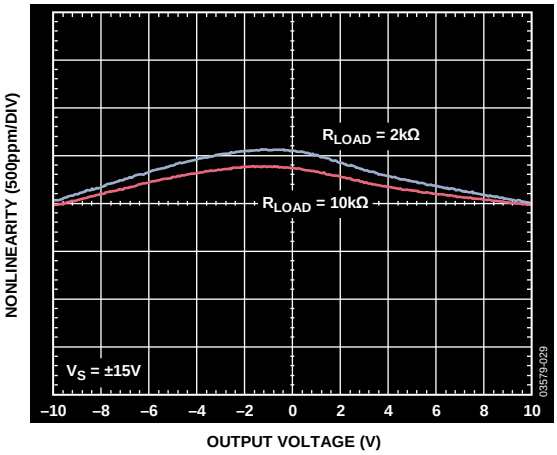

Figure 26. Gain Nonlinearity, G = 1000

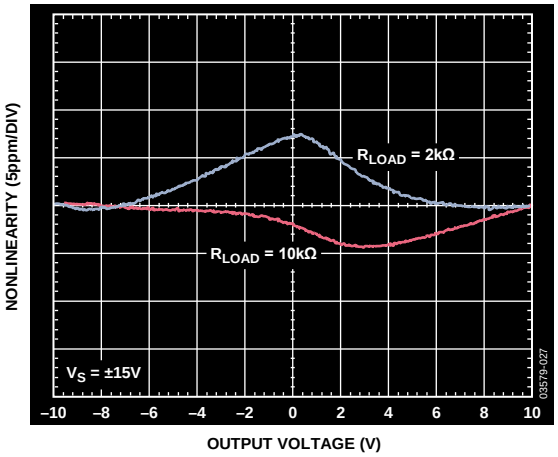

Figure 24. Gain Nonlinearity, G = 10

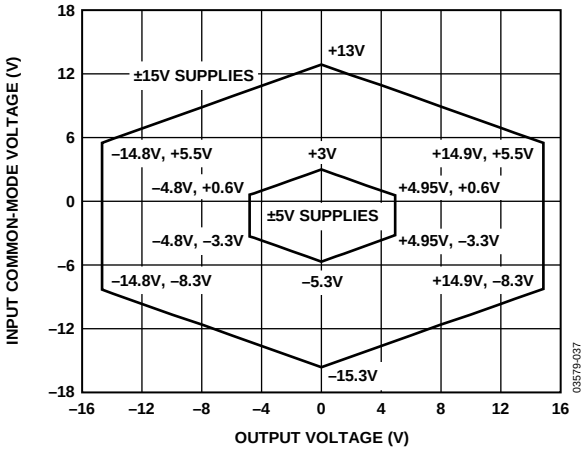

Figure 27. Input Common-Mode Voltage Range vs. Output Voltage, G = 1, V_{REF} = 0 V

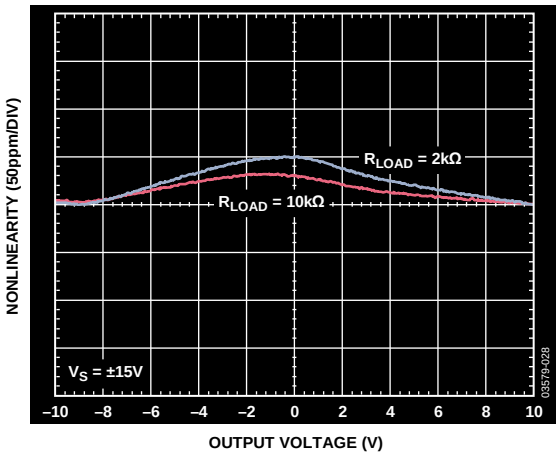

Figure 25. Gain Nonlinearity, G = 100

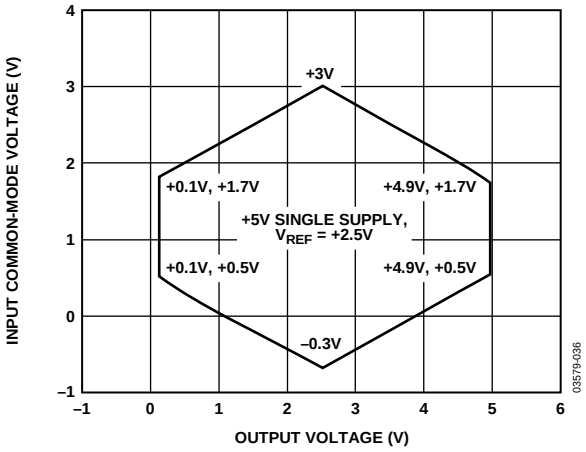

Figure 28. Input Common-Mode Voltage Range vs. Output Voltage, G = 1, V_S = +5 V, V_{REF} = 2.5 V

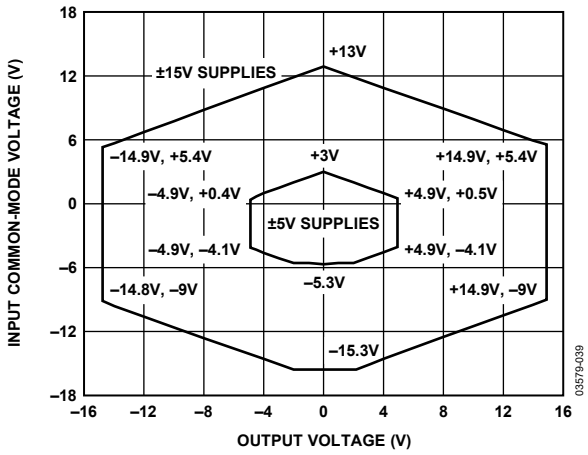

Figure 29. Input Common-Mode Voltage Range vs. Output Voltage, G = 100, V_{REF} = 0 V

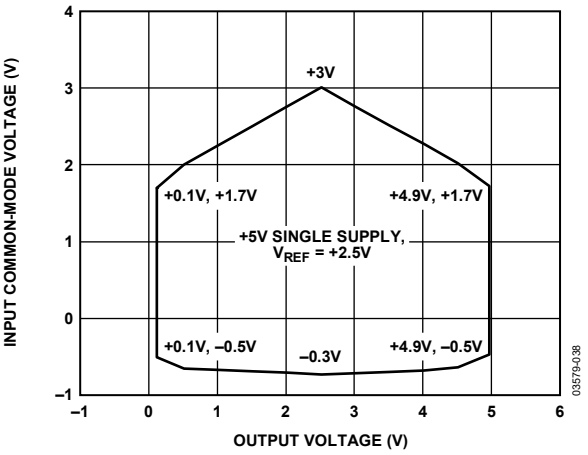

Figure 30. Input Common-Mode Voltage Range vs. Output Voltage, G = 100, V_S = +5 V, V_{REF} = 2.5 V

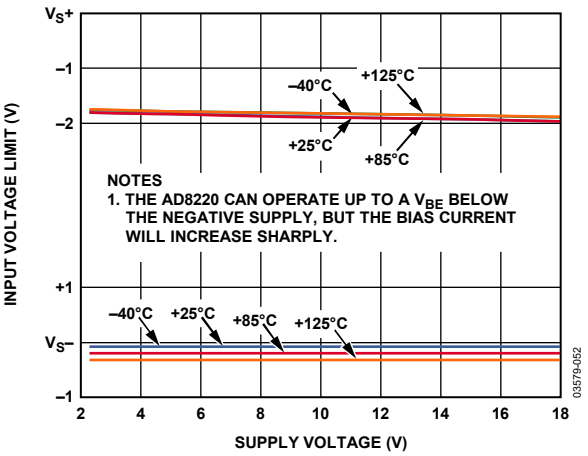

Figure 31. Input Voltage Limit vs. Supply Voltage, G = 1, V_{REF} =0 V

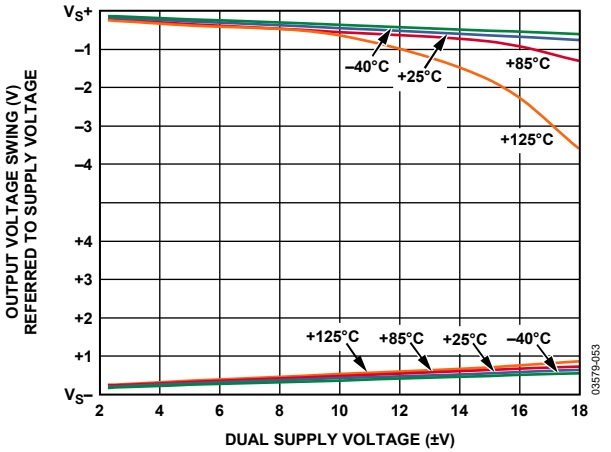

Figure 32. Output Voltage Swing vs. Supply Voltage, R_{LOAD} = 2 kΩ, G = 10, V_{REF} = 0 V

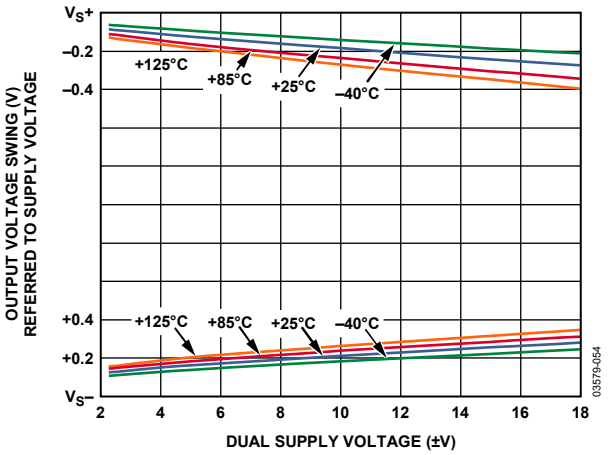

Figure 33. Output Voltage Swing vs. Supply Voltage, R_{LOAD} = 10 kΩ, G = 10, V_{REF} = 0 V

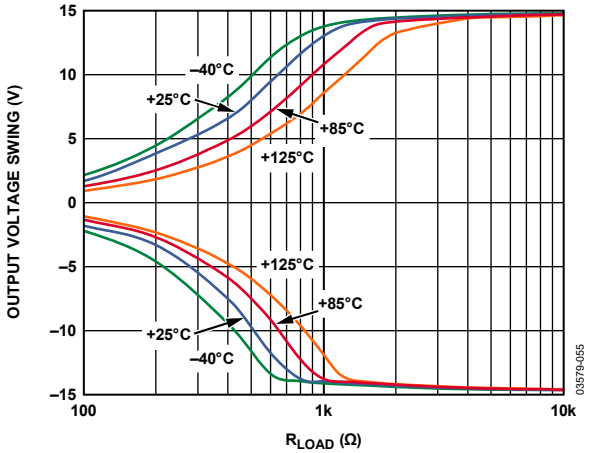

Figure 34. Output Voltage Swing vs. Load Resistance V_S = ±15 V, V_{REF} = 0 V

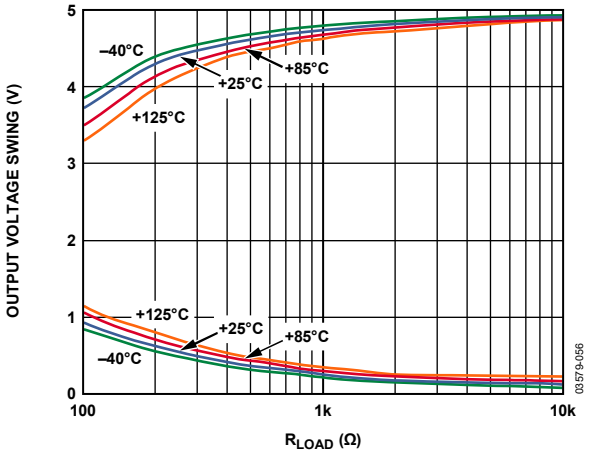

Figure 35. Output Voltage Swing vs. Load Resistance V_S = +5 V, V_{REF} = 2.5 V

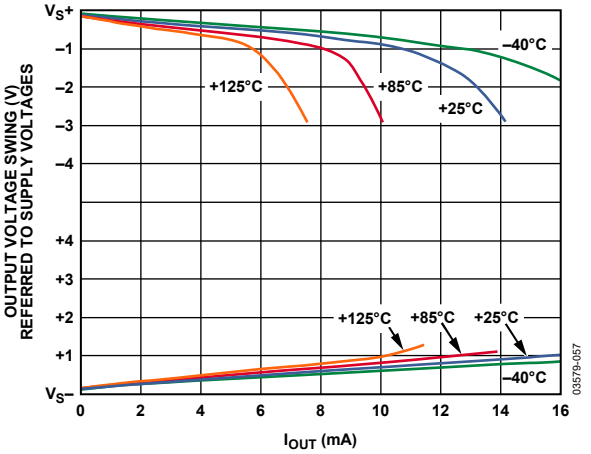

Figure 36. Output Voltage Swing vs. Output Current, V_S = ±15 V, V_{REF} = 0 V

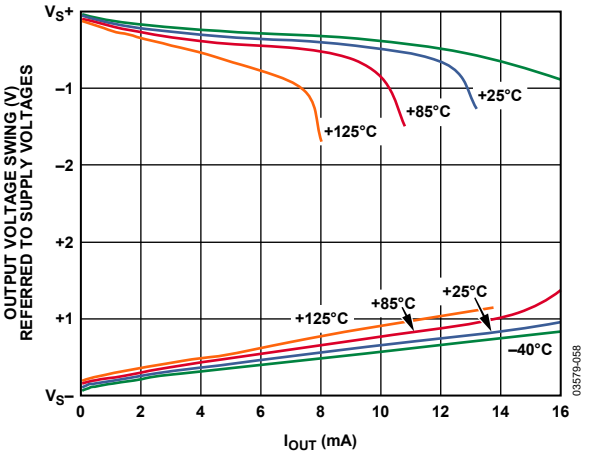

Figure 37. Output Voltage Swing vs. Output Current, V_S = 5 V, V_{REF} = 2.5 V

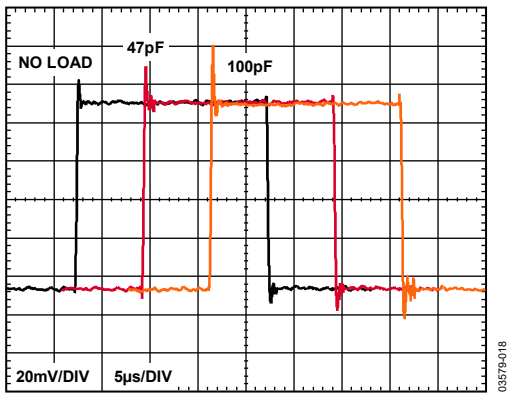

Figure 38. Small Signal Pulse Response for Various Capacitive Loads, V_S = ±15 V, V_{REF} = 0 V

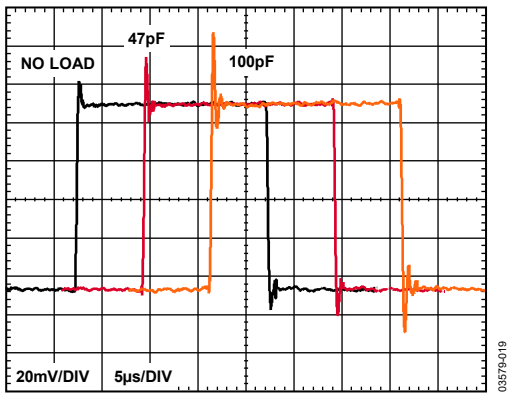

Figure 39. Small Signal Pulse Response for Various Capacitive Loads, V_S = 5 V, V_{REF} = 2.5 V

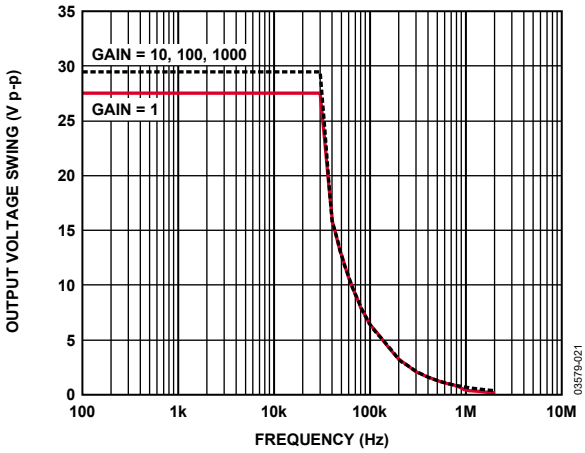

Figure 40. Output Voltage Swing vs. Large Signal Frequency Response

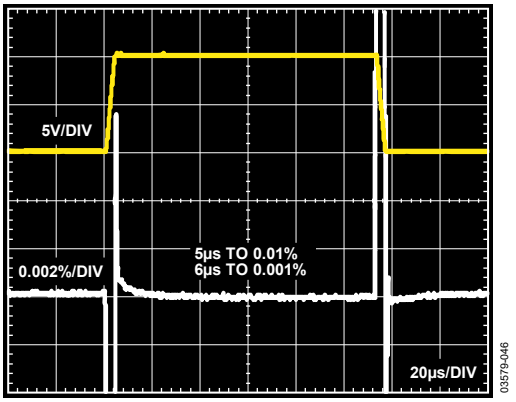

Figure 41. Large Signal Pulse Response and Settle Time, G = 1, R_{LOAD} = 10 kΩ, V_S = ±15 V, V_{REF} = 0 V

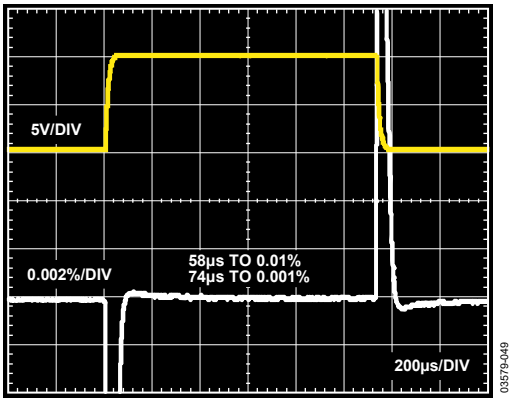

Figure 44. Large Signal Pulse Response and Settle Time, G = 1000, R_{LOAD} = 10 kΩ, V_S = ±15 V, V_{REF} = 0 V

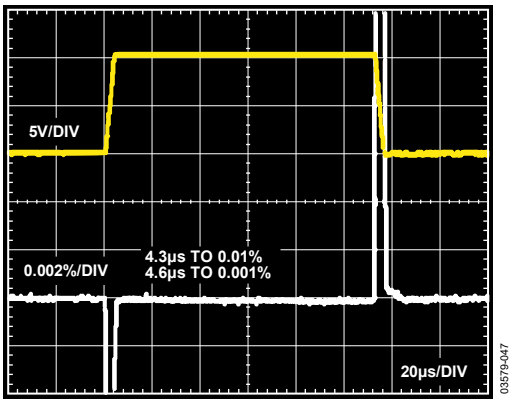

Figure 42. Large Signal Pulse Response and Settle Time, G = 10, R_{LOAD} = 10 kΩ, V_S = ±15 V, V_{REF} = 0 V

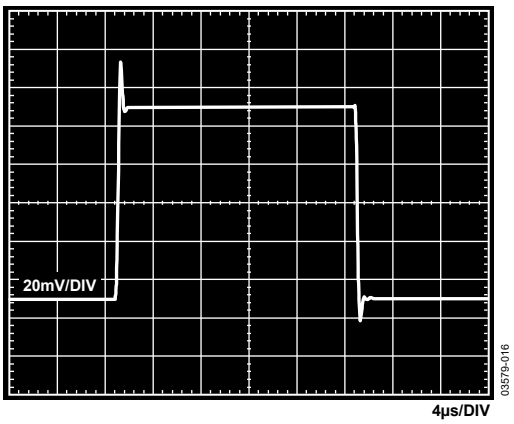

Figure 45. Small Signal Pulse Response, G = 1, R_{LOAD} = 2 kΩ, C_{LOAD} = 100 pF, V_S = ±15 V, V_{REF} = 0 V

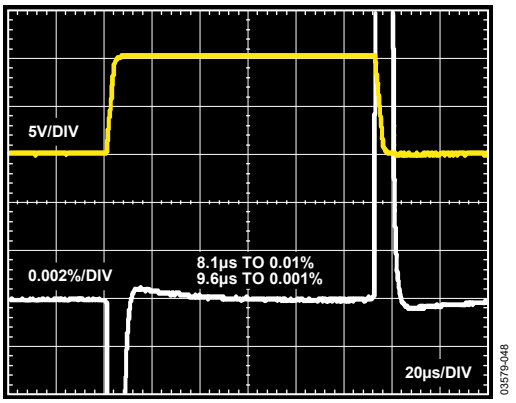

Figure 43. Large Signal Pulse Response and Settle Time, G = 100, R_{LOAD} = 10 kΩ, V_S = ±15 V, V_{REF} = 0 V

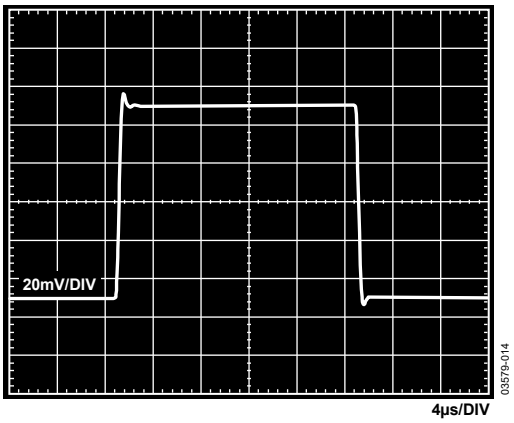

Figure 46. Small Signal Pulse Response, G = 10, R_{LOAD} = 2 kΩ, C_{LOAD} = 100 pF, V_S = ±15 V, V_{REF} = 0 V

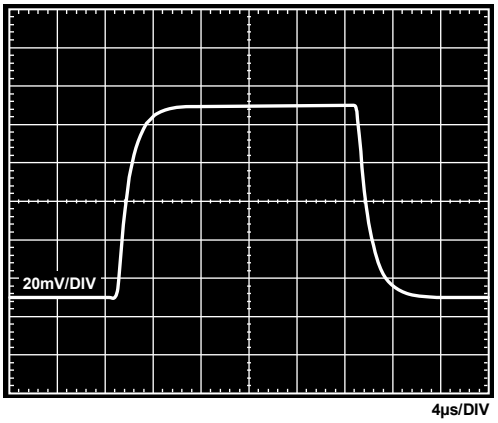

Figure 47. Small Signal Pulse Response, G = 100, R_{LOAD} = 2 kΩ, C_{LOAD} = 100 pF, V_S = ±15 V, V_{REF} =0 V

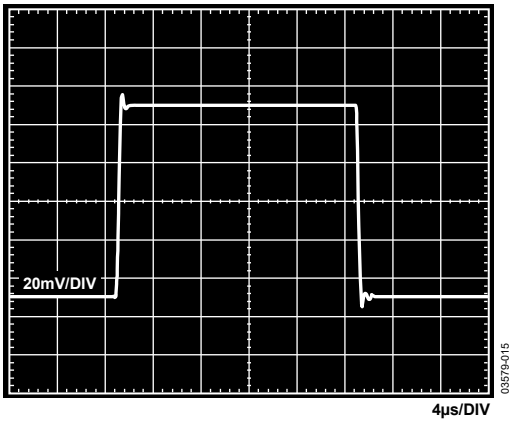

Figure 50. Small Signal Pulse Response, G = 10, R_{LOAD} = 2 kΩ, C_{LOAD} = 100 pF, V_S = 5 V, V_{REF} = 2.5 V

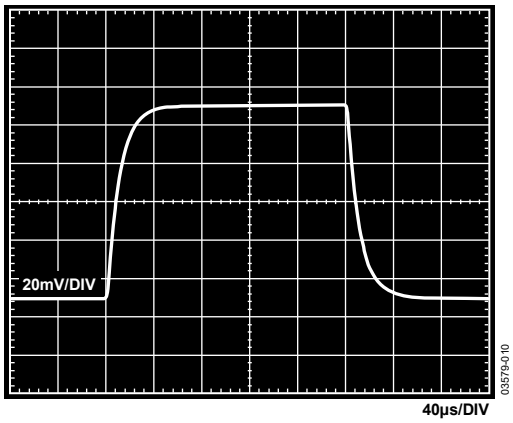

Figure 48. Small Signal Pulse Response, G = 1000, R_{LOAD} = 2 kΩ, C_{LOAD} = 100 pF, V_S = ±15 V, V_{REF} = 0 V

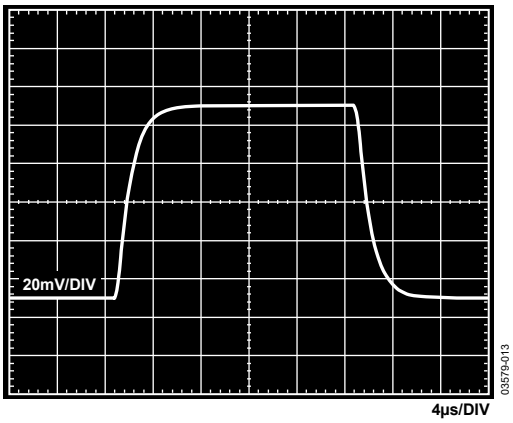

Figure 51. Small Signal Pulse Response, G = 100, R_{LOAD} = 2 kΩ, C_{LOAD} = 100 pF, V_S = 5 V, V_{REF} = 2.5 V

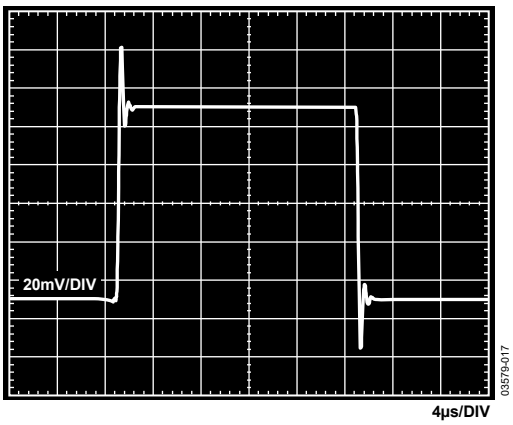

Figure 49. Small Signal Pulse Response, G = 1, R_{LOAD} = 2 kΩ, C_{LOAD} = 100 pF, V_S = 5 V, V_{REF} = 2.5 V

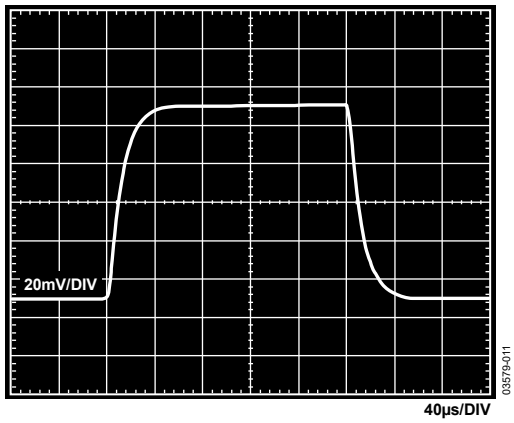

Figure 52. Small Signal Pulse Response, G = 1000, R_{LOAD} = 2 kΩ, C_{LOAD} = 100 pF, V_S = 5 V, V_{REF} = 2.5 V

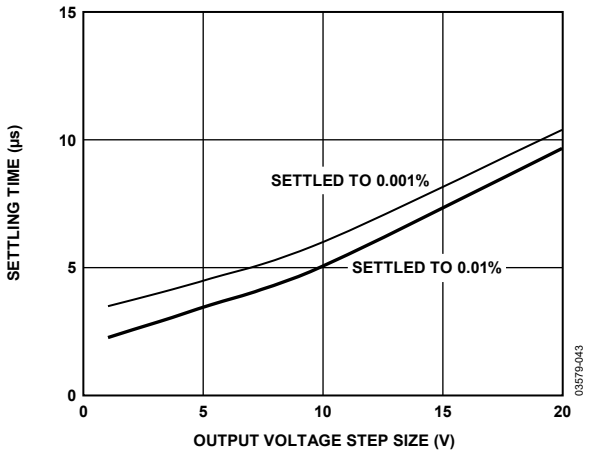

Figure 53. Settling Time vs. Output Voltage Step Size (G = 1) ±15 V, V_{REF} = 0 V

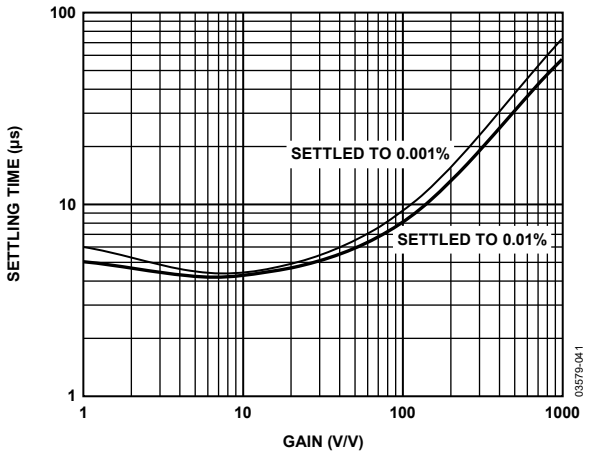

Figure 54. Settling Time vs. Gain for a 10 V Step, V_S = ±15 V, V_{REF} = 0 V

THEORY OF OPERATION

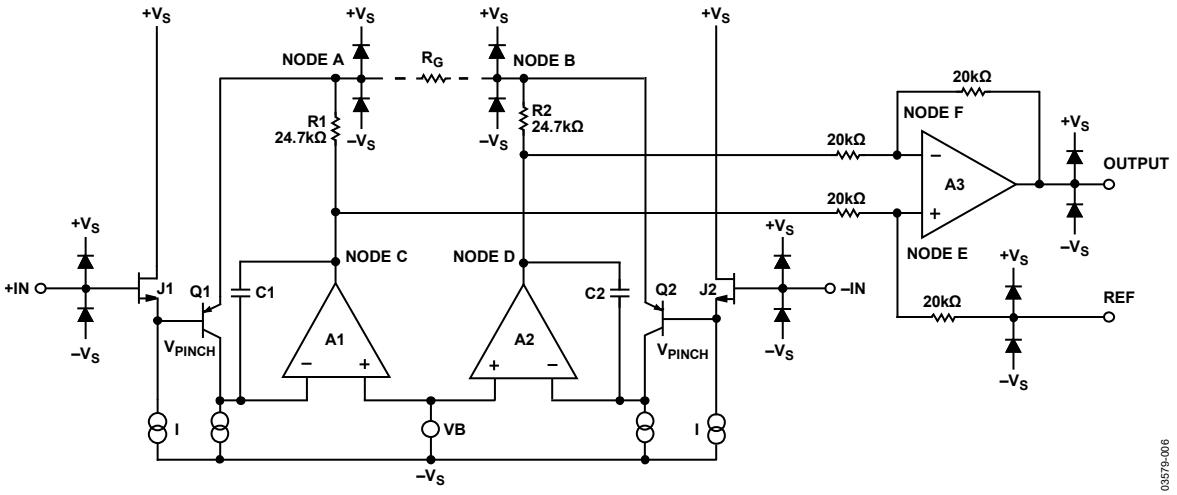

Figure 55. Simplified Schematic

The AD8220 is a JFET input, monolithic instrumentation amplifier based on the classic 3-op amp topology (see Figure 55). Input Transistor J1 and Input Transistor J2 are biased at a fixed current so that any input signal forces the output voltages of A1 and A2 to change accordingly; the input signal creates a current through R_G that flows in R1 and R2 such that the outputs of A1 and A2 provide the correct, gained signal. Topologically, J1, A1, and R1 and J2, A2, and R2 can be viewed as precision current feedback amplifiers that have a gain bandwidth of 1.5 MHz. The common-mode voltage and amplified differential signal from A1 and A2 are applied to a difference amplifier that rejects the common-mode voltage but amplifies the differential signal. The difference amplifier employs 20 kΩ laser-trimmed resistors that result in an in-amp with gain error less than 0.04%. New trim techniques were developed to ensure that CMRR exceeds 86 dB (G = 1).

Using JFET transistors, the AD8220 offers an extremely high input impedance, extremely low bias currents of 10 pA maximum, a low offset current of 0.6 pA maximum, and no input bias current noise. In addition, input offset is less than 125 µV and drift is less than 5 µV/°C. Ease of use and robustness were considered. A common problem for instrumentation amplifiers is that at high gains, when the input is overdriven,[1] an excessive milliampere input bias current can result and the output can undergo phase reversal. The AD8220 has none of these problems; its input bias current is limited to less than 10 µA, and the output does not phase reverse under overdrive fault conditions.

[1] Overdriving the input at high gains refers to when the input signal is within the supply voltages but the amplifier cannot output the gained signal. For example, at a gain of 100, driving the amplifier with 10 V on ±15 V constitutes overdriving the inputs since the amplifier cannot output 100 V.

The AD8220 has extremely low load-induced nonlinearity. All amplifiers that comprise the AD8220 have rail-to-rail output capability for enhanced dynamic range. The input of the AD8220 can amplify signals with wide common-mode voltages even slightly lower than the negative supply rail. The AD8220 operates over a wide supply voltage range. It can operate from either a single +4.5 V to +36 V supply or a dual ±2.25 V to ±18 V. The transfer function of the AD8220 is

$$G = 1 + \frac{49.4\ \text{k}\Omega}{R_G}$$

Users can easily and accurately set the gain using a single, standard resistor. Because the input amplifiers employ a current feedback architecture, the AD8220 gain-bandwidth product increases with gain, resulting in a system that does not suffer as much bandwidth loss as voltage feedback architectures at higher gains. A unique pinout enables the AD8220 to meet a CMRR specification of 80 dB through 5 kHz (G = 1). The balanced pinout, shown in Figure 56, reduces parasitics that adversely affect CMRR performance. In addition, the new pinout simplifies board layout because associated traces are grouped together. For example, the gain setting resistor pins are adjacent to the inputs, and the reference pin is next to the output.

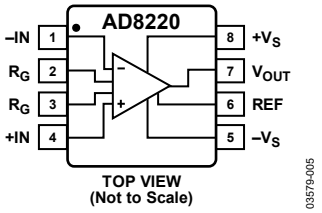

Figure 56. Pin Configuration

GAIN SELECTION

Placing a resistor across the R_G terminals sets the AD8220 gain, which can be calculated by referring to Table 5 or by using the gain equation

$$R_G = \frac{49.4\ \text{k}\Omega}{G-1}$$

Table 5. Gains Achieved Using 1% Resistors

1% Standard Table Value of RG (Ω)	Calculated Gain
49.9 k	1.990
12.4 k	4.984
5.49 k	9.998
2.61 k	19.93
1.00 k	50.40
499	100.0
249	199.4
100	495.0
49.9	991.0

The AD8220 defaults to G = 1 when no gain resistor is used. Gain accuracy is determined by the absolute tolerance of R_G. The TC of the external gain resistor increases the gain drift of the instrumentation amplifier. Gain error and gain drift are kept to a minimum when the gain resistor is not used.

LAYOUT

Careful board layout maximizes system performance. In applications that need to take advantage of the low input bias current of the AD8220, avoid placing metal under the input path to minimize leakage current. To maintain high CMRR over frequency, lay out the input traces symmetrically and lay out the traces of the R_G resistor symmetrically. Ensure that the traces maintain resistive and capacitive balance; this holds for additional PCB metal layers under the input and R_G pins. Traces from the gain setting resistor to the R_G pins should be kept as short as possible to minimize parasitic inductance. An example layout is shown in Figure 57 and Figure 58. To ensure the most accurate output, the trace from the REF pin should either be connected to the AD8220 local ground (see Figure 59) or connected to a voltage that is referenced to the AD8220 local ground.

Common-Mode Rejection Ratio (CMRR)

The AD8220 has high CMRR over frequency giving it greater immunity to disturbances, such as line noise and its associated harmonics, in contrast to typical in-amps whose CMRR falls off around 200 Hz. These in-amps often need common-mode filters at the inputs to compensate for this shortcoming. The AD8220 is able to reject CMRR over a greater frequency range, reducing the need for input common-mode filtering.

A well-implemented layout helps to maintain the high CMRR over frequency of the AD8220. Input source impedance and capacitance should be closely matched. In addition, source resistance and capacitance should be placed as close to the inputs as possible.

Grounding

The output voltage of the AD8220 is developed with respect to the potential on the reference terminal. Care should be taken to tie REF to the appropriate local ground (see Figure 59).

In mixed-signal environments, low level analog signals need to be isolated from the noisy digital environment. Many ADCs have separate analog and digital ground pins. Although it is convenient to tie both grounds to a single ground plane, the current traveling through the ground wires and PC board can cause a large error. Therefore, separate analog and digital ground returns should be used to minimize the current flow from sensitive points to the system ground.

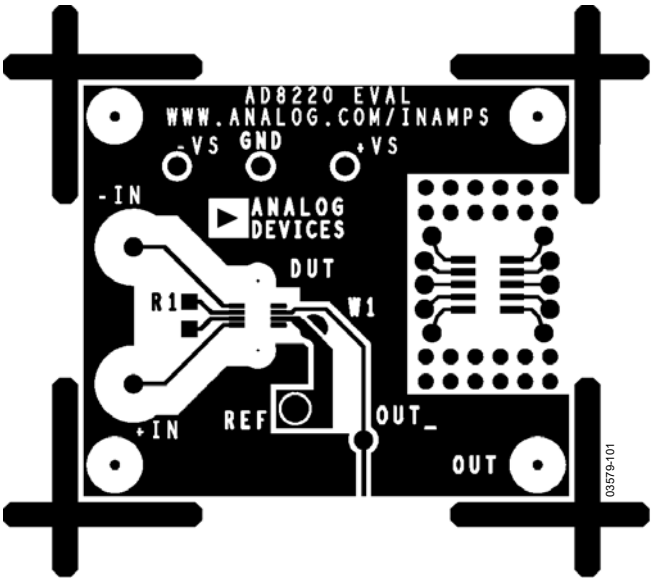

Figure 57. Example Layout—Top Layer of the AD8220 Evaluation Board

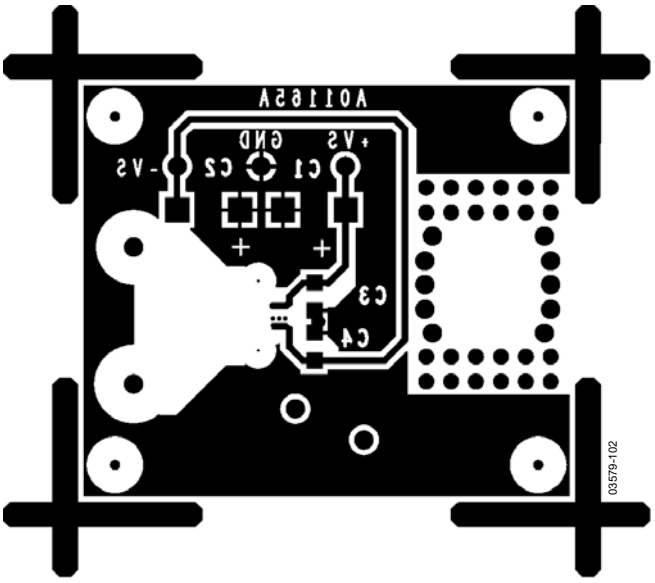

Figure 58. Example Layout—Bottom Layer of the AD8220 Evaluation Board

REFERENCE TERMINAL

The reference terminal, REF, is at one end of a 20 kΩ resistor (see Figure 55). The output of the instrumentation amplifier is referenced to the voltage on the REF terminal; this is useful when the output signal needs to be offset to voltages other than common. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8220 can interface with an ADC. The allowable reference voltage range is a function of the gain, common-mode input, and supply voltages. The REF pin should not exceed either $+V_S$ or $-V_S$ by more than 0.5 V.

For best performance, especially in cases where the output is not measured with respect to the REF terminal, source impedance to the REF terminal should be kept low, because parasitic resistance can adversely affect CMRR and gain accuracy.

POWER SUPPLY REGULATION AND BYPASSING

The AD8220 has high PSRR. However, for optimal performance, a stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. As in all linear circuits, bypass capacitors must be used to decouple the amplifier.

A 0.1 µF capacitor should be placed close to each supply pin. A 10 µF tantalum capacitor can be used further away from the part (see Figure 59). In most cases, it can be shared by other precision integrated circuits.

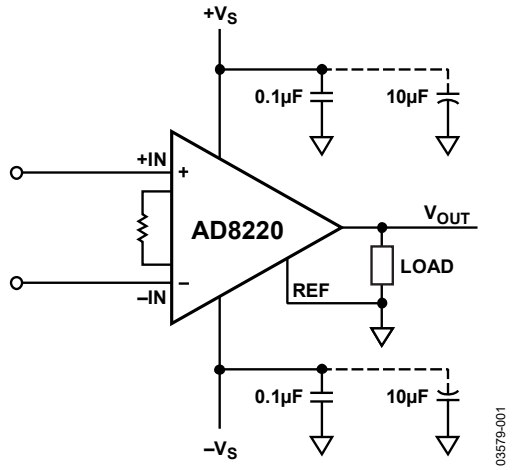

Figure 59. Supply Decoupling, REF and Output Referred to Ground

INPUT BIAS CURRENT RETURN PATH

The AD8220 input bias current is extremely small at less than 10 pA. Nonetheless, the input bias current must have a return path to common. When the source, such as a transformer, cannot provide a return current path, one should be created (see Figure 60).

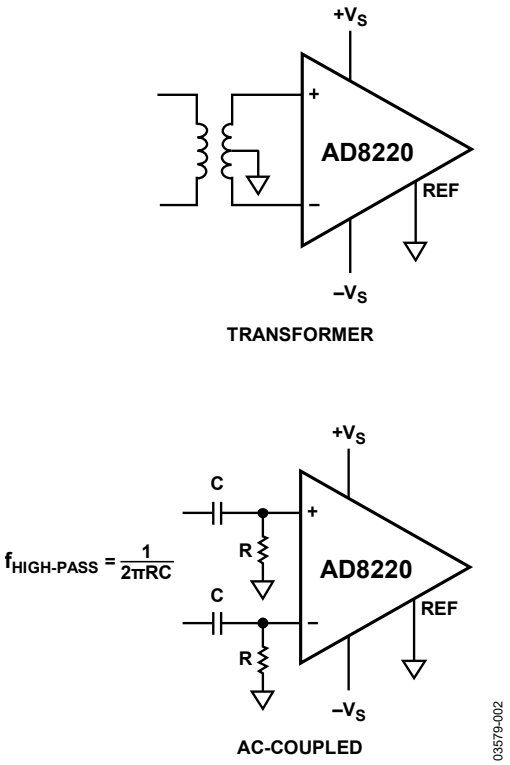

Figure 60. Creating an I_{BIAS} Path

INPUT PROTECTION

All terminals of the AD8220 are protected against ESD. (ESD protection is guaranteed to 4 kV, human body model.) In addition, the input structure allows for dc overload conditions a diode drop above the positive supply and a diode drop below the negative supply. Voltages beyond a diode drop of the supplies cause the ESD diodes to conduct and enable current to flow through the diode. Therefore, an external resistor should be used in series with each of the inputs to limit current for voltages above +Vs. In either scenario, the AD8220 safely handles a continuous 6 mA current at room temperature.

For applications where the AD8220 encounters extreme overload voltages, as in cardiac defibrillators, external series resistors and low leakage diode clamps, such as BAV199Ls, FJH1100s, or SP720s, should be used.

RF INTERFERENCE

RF rectification is often a problem in applications where there are large RF signals. The problem appears as a small dc offset voltage. The AD8220 by its nature has a 5 pF gate capacitance, C_G, at its inputs. Matched series resistors form a natural low-pass filter that reduces rectification at high frequency (see Figure 61). The relationship between external, matched series resistors and the internal gate capacitance is expressed as follows:

$$FilterFreq_{DIFF} = \frac{1}{2\pi RC_G}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_G}$$

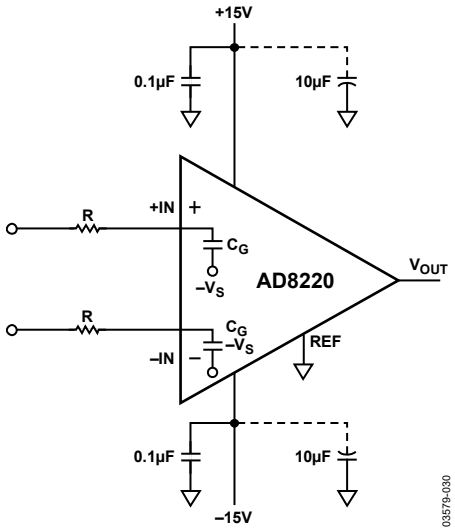

Figure 61. RFI Filtering Without External Capacitors

To eliminate high frequency common-mode signals while using smaller source resistors, a low-pass RC network can be placed at the input of the instrumentation amplifier (see Figure 62). The filter limits the input signal bandwidth according to the following relationship:

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2\,C_D + C_C + C_G)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi R(C_C + C_G)}$$

Mismatched C_C capacitors result in mismatched low-pass filters. The imbalance causes the AD8220 to treat what would have been a common-mode signal as a differential signal. To reduce the effect of mismatched external C_C capacitors, select a value of C_D greater than 10 times C_C. This sets the differential filter frequency lower than the common-mode frequency.

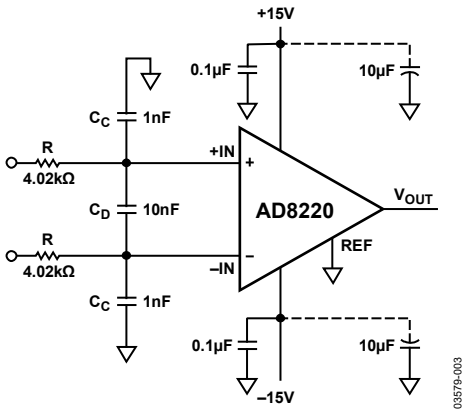

Figure 62. RFI Suppression

COMMON-MODE INPUT VOLTAGE RANGE

The common-mode input voltage range is a function of the input range and the outputs of Internal Amplifier A1, Internal Amplifier A2, and Internal Amplifier A3, the reference voltage, and the gain. Figure 27 to Figure 30 show common-mode voltage ranges for various supply voltages and gains.

DRIVING AN ADC

An instrumentation amplifier is often used in front of an ADC to provide CMRR and additional conditioning, such as a voltage level shift and gain (see Figure 63). In this example, a 2.7 nF capacitor and a 1 kΩ resistor create an antialiasing filter for the AD7685. The 2.7 nF capacitor also serves to store and deliver the necessary charge to the switched capacitor input of the ADC. The 1 kΩ series resistor reduces the burden of the 2.7 nF load from the amplifier. However, large source impedance in front of the ADC can degrade THD.

The example shown in Figure 63 is for sub-60 kHz applications. For higher bandwidth applications where THD is important, the series resistor needs to be small. At worst, a small series resistor can load the AD8220, potentially causing the output to overshoot or ring. In such cases, a buffer amplifier, such as the AD8615, should be used after the AD8220 to drive the ADC.

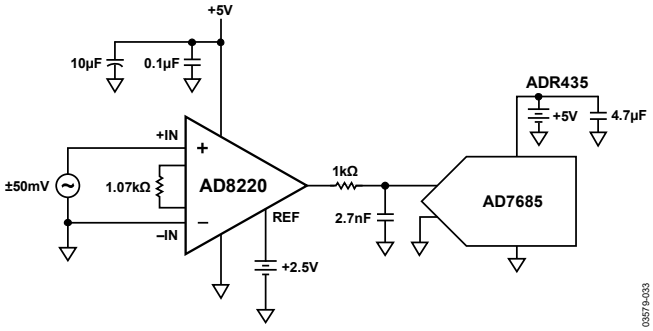

Figure 63. Driving an ADC in a Low Frequency Application

APPLICATIONS INFORMATION

AC-COUPLED INSTRUMENTATION AMPLIFIER

Measuring small signals that are in the noise or offset of the amplifier can be a challenge. Figure 64 shows a circuit that can improve the resolution of small ac signals. The large gain reduces the referred input noise of the amplifier to 14 nV/√Hz. Therefore, smaller signals can be measured because the noise floor is lower. DC offsets that would have been gained by 100 are eliminated from the AD8220 output by the integrator feedback network.

At low frequencies, the OP1177 forces the AD8220 output to 0 V. Once a signal exceeds $f_{HIGH\text{-}PASS}$, the AD8220 outputs the amplified input signal.

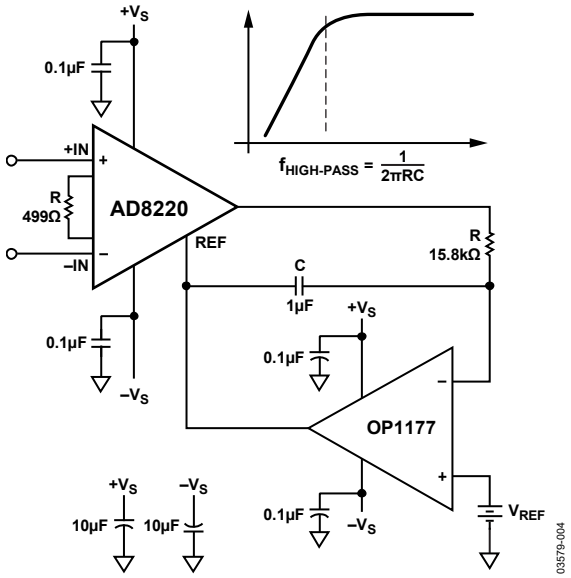

Figure 64. AC-Coupled Circuit

DIFFERENTIAL OUTPUT

In certain applications, it is necessary to create a differential signal. New high resolution ADCs often require a differential input. In other cases, transmission over a long distance can require differential processing for better immunity to interference.

Figure 65 shows how to configure the AD8220 to output a differential signal. An OP1177 op amp is used to create a differential voltage. Errors from the op amp are common to both outputs and are thus common mode. Likewise, errors from using mismatched resistors cause a common-mode dc offset error. Such errors are rejected in differential signal processing by differential input ADCs or instrumentation amplifiers.

When using this circuit to drive a differential ADC, V_{REF} can be set using a resistor divider from the reference of the ADC to make the output ratiometric with the ADC as shown in Figure 66.

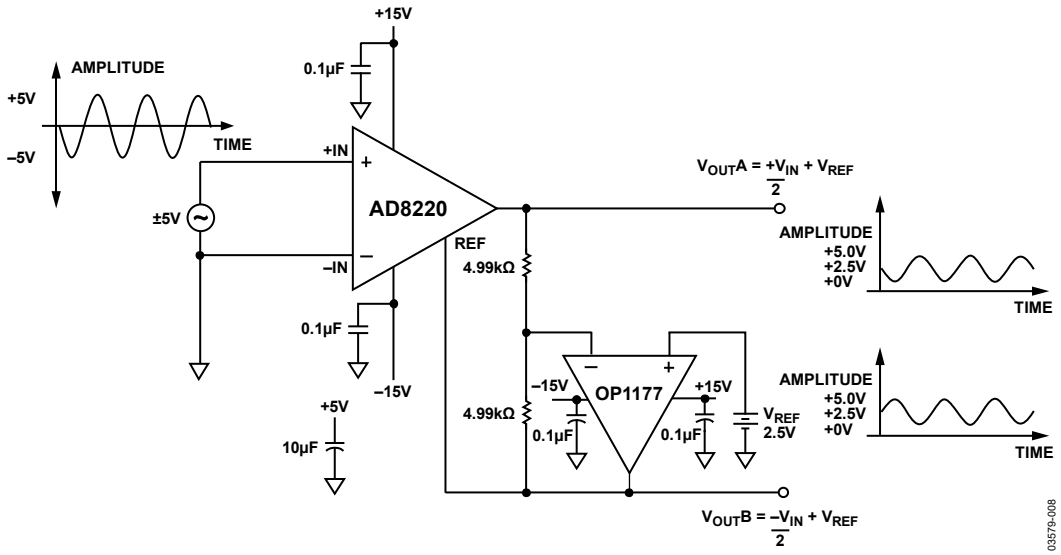

Figure 65. Differential Output with Level Shift

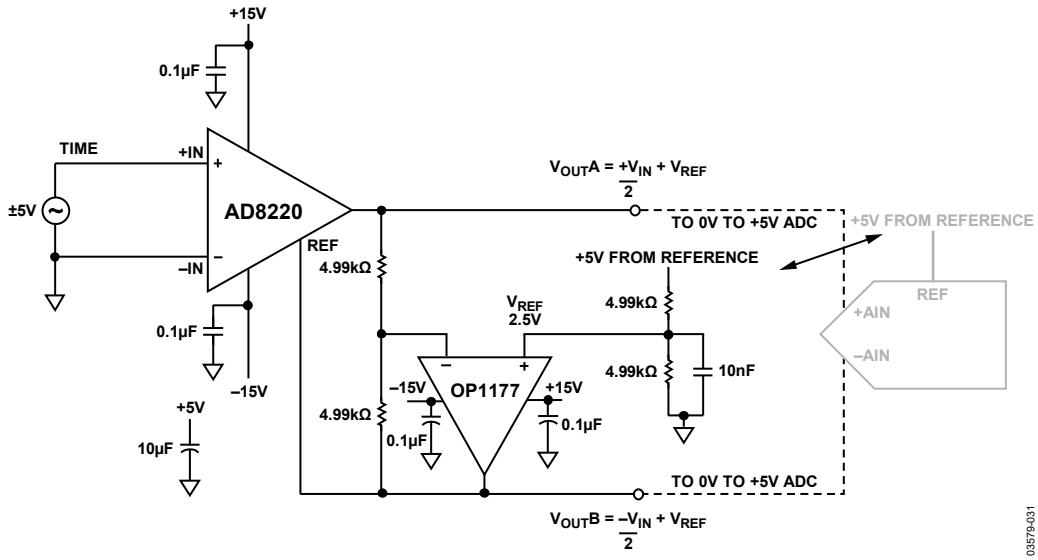

Figure 66. Configuring the AD8220 to Output A Ratiometric, Differential Signal

ELECTROCARDIOGRAM SIGNAL CONDITIONING

The AD8220 makes an excellent input amplifier for next generation ECGs. Its small size, high CMRR over frequency, rail-to-rail output, and JFET inputs are well suited for this application. Potentials measured on the skin range from 0.2 mV to 2 mV. The AD8220 solves many of the typical challenges of measuring these body surface potentials. The high CMRR of the AD8220 helps reject common-mode signals that come in the form of line noise or high frequency EMI from equipment in the operating room. Its rail-to-rail output offers a wide dynamic range allowing for higher gains than would be possible using other instrumentation amplifiers. JFET inputs offer a large input capacitance of 5 pF. A natural RC filter is formed reducing high frequency noise when series input resistors are used in front of the AD8220 (see the RF Interference section).

In addition, the AD8220 JFET inputs have ultralow input bias current and no current noise, making it useful for ECG applications where there are often large impedances. The MSOP and the optimal pinout of the AD8220 allow smaller footprints and more efficient layout, paving the way for next-generation portable ECGs.

Figure 67 shows an example ECG schematic. Following the AD8220 is a 0.033 Hz high-pass filter, formed by the 4.7 µF capacitor and the 1 MΩ resistor, which removes the dc offset that develops between the electrodes. An additional gain of 50, provided by the AD8618, makes use of the 0 V to 5 V input range of the ADC. An active, fifth-order, low-pass Bessel filter removes signals greater than approximately 160 Hz. An OP2177 buffers, inverts, and gains the common-mode voltage taken at the midpoint of the AD8220 gain setting resistors. This right-leg drive circuit helps cancel common-mode signals by inverting the common-mode signal and driving it back into the body. A 499 kΩ series resistor at the output of the OP2177 limits the current driven into the body.

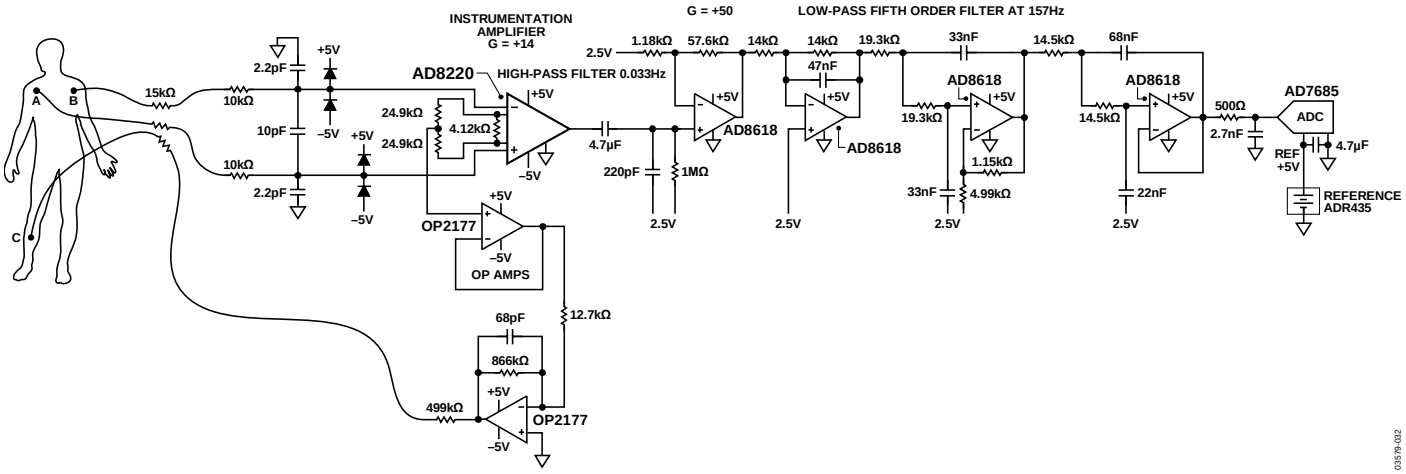

Figure 67. Example ECG Schematic

OUTLINE DIMENSIONS

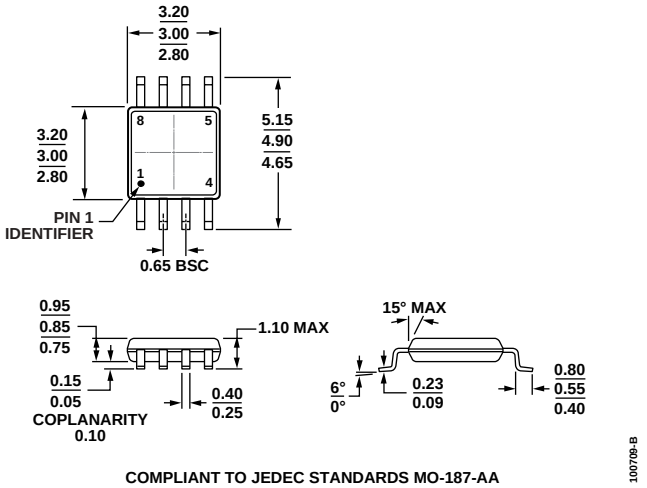

Figure 68. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range[3]	Package Description	Package Option	Marking Code
AD8220ARMZ	−40°C to +85°C	8-Lead MSOP	RM-8	H01
AD8220ARMZ-R7	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	H01
AD8220BRMZ	−40°C to +85°C	8-Lead MSOP	RM-8	H0P
AD8220BRMZ-RL	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	H0P
AD8220BRMZ-R7	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	H0P
AD8220WARMZ	−40°C to +125°C	8-Lead MSOP	RM-8	Y2D
AD8220WARMZ-RL	−40°C to +125°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y2D
AD8220WARMZ-R7	−40°C to +125°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y2D

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] See the Typical Performance Characteristics section for expected operation from 85°C to 125°C.

AUTOMOTIVE PRODUCTS

The AD8220W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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