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SPECIFICATIONS

T_A = 25°C, V_S = 5 V, R_L = 2 kΩ to 2.5 V, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth, V_O < 0.5 V p-p	G = +1	125	160		MHz
Bandwidth for 0.1 dB Flatness	G = +2, R_L = 150 Ω, R_F = 200 Ω		14		MHz
Slew Rate	G = −1, V_{OUT} = 2 V step	130	200		V/µs
Full Power Response	V_O = 2 V p-p		30		MHz
Settling Time to 1%	G = −1, V_{OUT} = 2 V step		26		ns
Settling Time to 0.1%			39		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_{OUT} = 2 V p-p, G = +2, R_L = 1 kΩ		−73		dB
Input Voltage Noise	f = 10 kHz		15		nV/√Hz
Input Current Noise	f = 10 kHz		700		fA/√Hz
Differential Gain Error (NTSC, 100 IRE)	G = +2, R_L = 150 Ω to 2.5 V		0.04	0.06	%
	G = +2, R_L = 75 Ω to 2.5 V		0.04		%
Differential Phase Error (NTSC, 100 IRE)	G = +2, R_L = 150 Ω to 2.5 V		0.06	0.12	Degrees
	G = +2, R_L = 75 Ω to 2.5 V		0.24		Degrees
Worst-Case Crosstalk	f = 5 MHz, R_L = 150 Ω to 2.5 V		−63		dB
DC PERFORMANCE					
Input Offset Voltage			3	9	mV
	T_{MIN} to T_{MAX}			12	mV
Offset Drift			12		µV/°C
Input Bias Current			1.2	3.2	µA
	T_{MIN} to T_{MAX}			4.8	µA
Input Offset Current			0.2	0.5	µA
Open-Loop Gain	R_L = 1 kΩ	90	100		dB
	T_{MIN} to T_{MAX}		90		dB
INPUT CHARACTERISTICS					
Input Resistance			300		kΩ
Input Capacitance			1.5		pF
Input Common-Mode Voltage Range			−0.2 to +4		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 3.5 V	68	74		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 10 kΩ to 2.5 V		0.03 to 4.97		V
	R_L = 1 kΩ to 2.5 V	0.10 to 4.9	0.05 to 4.95		V
	R_L = 50 Ω to 2.5 V	0.4 to 4.4	0.36 to 4.45		V
Output Current	T_{MIN} to T_{MAX}, V_{OUT} = 0.5 V to 4.5 V		50		mA
Short-Circuit Current	Sourcing		90		mA
	Sinking		100		mA
Capacitive Load Drive	G = +1		20		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current (Per Amplifier)			5.5	6.4	mA
Power Supply Rejection Ratio	V_{S-} = 0 V to −1 V, or V_{S+} = 5 V to 6 V	72	80		dB
OPERATING TEMPERATURE RANGE		−40		+85	°C

T_A = 25°C, V_S = 3 V, R_L = 2 kΩ to 1.5 V, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth, V_O < 0.5 V p-p	G = +1	120	140		MHz
Bandwidth for 0.1 dB Flatness	G = +2, R_L = 150 Ω, R_F = 200 Ω		11		MHz
Slew Rate	G = −1, V_{OUT} = 2 V step	120	170		V/µs
Full Power Response	V_O = 2 V p-p		25		MHz
Settling Time to 1%	G = −1, V_{OUT} = 1 V step		30		ns
Settling Time to 0.1%			45		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_{OUT} = 2 V p-p, G = −1, R_L = 100 Ω		−56		dB
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 10 kHz		500		fA/√Hz
Differential Gain Error (NTSC, 100 IRE)	G = +2, R_L = 150 Ω to 1.5 V, Input V_{CM} = 1 V		0.10		%
	R_L = 75 Ω to 1.5 V, Input V_{CM} = 1 V		0.10		%
Differential Phase Error (NTSC, 100 IRE)	G = +2, R_L = 150 Ω to 1.5 V, Input V_{CM} = 1 V		0.12		Degrees
	R_L = 75 Ω to 1.5 V, Input V_{CM} = 1 V		0.27		Degrees
Worst-Case Crosstalk	f = 5 MHz, R_L = 1 kΩ to 1.5 V		−68		dB
DC PERFORMANCE					
Input Offset Voltage			3	9	mV
	T_{MIN} to T_{MAX}			12	mV
Offset Drift			12		µV/°C
Input Bias Current			1.2	3.2	µA
	T_{MIN} to T_{MAX}			4.8	µA
Input Offset Current			0.2	0.6	µA
Open-Loop Gain	R_L = 1 kΩ	90	100		dB
	T_{MIN} to T_{MAX}		90		dB
INPUT CHARACTERISTICS					
Input Resistance			300		kΩ
Input Capacitance			1.5		pF
Input Common-Mode Voltage Range			−0.2 to +2		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 1.5 V	66	74		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 10 kΩ to 1.5 V		0.03 to 2.97		V
	R_L = 1 kΩ to 1.5 V	0.1 to 2.9	0.05 to 2.95		V
	R_L = 50 Ω to 1.5 V	0.3 to 2.6	0.25 to 2.65		V
Output Current	T_{MIN} to T_{MAX}, V_{OUT} = 0.5 V to 2.5 V		50		mA
Short-Circuit Current	Sourcing		50		mA
	Sinking		70		mA
Capacitive Load Drive	G = +1		17		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current (Per Amplifier)			5.5	6.4	mA
Power Supply Rejection Ratio	V_{S-} = 0 V to −1 V, or V_{S+} = 3 V to 4 V	68	80		dB
OPERATING TEMPERATURE RANGE		0		70	°C

T_A = 25°C, V_S = ±5 V, R_L = 2 kΩ to 0 V, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth, V_O < 0.5 V p-p	G = +1	125	170		MHz
Bandwidth for 0.1 dB Flatness	G = +2, R_L = 150 Ω, R_F = 200 Ω		18		MHz
Slew Rate	G = −1, V_{OUT} = 2 V step	145	225		V/µs
Full Power Response	V_O = 2 V p-p		35		MHz
Settling Time to 1%	G = −1, V_{OUT} = 2 V step		22		ns
Settling Time to 0.1%			32		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, G = +2, R_L = 1 kΩ		−78		dB
Input Voltage Noise	f = 10 kHz		15		nV/√Hz
Input Current Noise	f = 10 kHz		700		fA/√Hz
Differential Gain Error (NTSC, 100 IRE)	G = +2, R_L = 150 Ω		0.02	0.05	%
	G = +2, R_L = 75 Ω		0.02		%
Differential Phase Error (NTSC, 100 IRE)	G = +2, R_L = 150 Ω		0.04	0.10	Degrees
	G = +2, R_L = 75 Ω		0.12		Degrees
Worst-Case Crosstalk	f = 5 MHz, R_L = 150 Ω		−63		dB
DC PERFORMANCE					
Input Offset Voltage			3	9.8	mV
	T_{MIN} to T_{MAX}			14	mV
Offset Drift			12		µV/°C
Input Bias Current			1.2	3.2	µA
	T_{MIN} to T_{MAX}			4.8	µA
Input Offset Current			0.2	0.6	µA
Open-Loop Gain	R_L = 1 kΩ	90	94		dB
	T_{MIN} to T_{MAX}		86		dB
INPUT CHARACTERISTICS					
Input Resistance			300		kΩ
Input Capacitance			1.5		pF
Input Common-Mode Voltage Range			−5.2 to +4		V
Common-Mode Rejection Ratio	V_{CM} = −5 V to +3.5 V	66	74		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 10 kΩ		−4.97 to +4.97		V
	R_L = 1 kΩ	−4.8 to +4.8	−4.9 to +4.9		V
	R_L = 50 Ω	−4 to +3.2	−4.2 to +3.5		V
Output Current	T_{MIN} to T_{MAX}, V_{OUT} = −4.5 V to +4.5 V		50		mA
Short-Circuit Current	Sourcing		100		mA
	Sinking		100		mA
Capacitive Load Drive	G = +1		25		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current (Per Amplifier)			6	7	mA
Power Supply Rejection Ratio	V_{S-} = −5 V to −6 V, or V_{S+} = 5 V to 6 V	68	80		dB
OPERATING TEMPERATURE RANGE		−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	12.6 V
Internal Power Dissipation[1]	
8-Lead PDIP (N)	1.3 W
8-Lead SOIC_N (R)	0.9 W
Input Voltage (Common Mode)	$\pm V_S \pm 0.5$ V
Differential Input Voltage	±3.4 V
Output Short-Circuit Duration	Observe Power Derating Curves
Storage Temperature Range (N, R)	−65°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Specification is for the device in free air:
8-Lead PDIP: θ_{JA} = 90°C/W
8-Lead SOIC_N: θ_{JA} = 155°C/W.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8042 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily can cause a shift in parametric performance due to a change in the stresses exerted on the die by the package.

Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8042 is internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

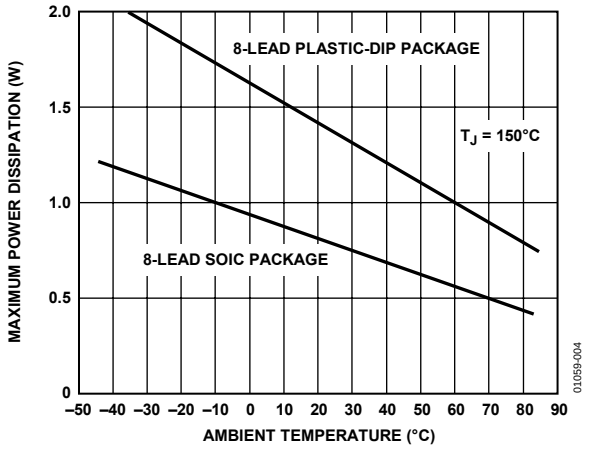


Figure 4. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

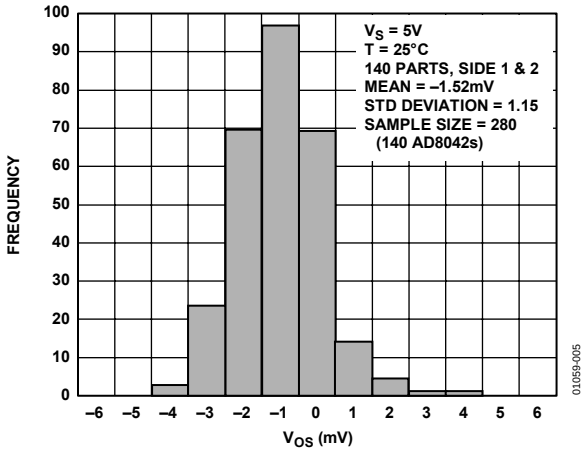


Figure 5. Typical Distribution of V_{OS}

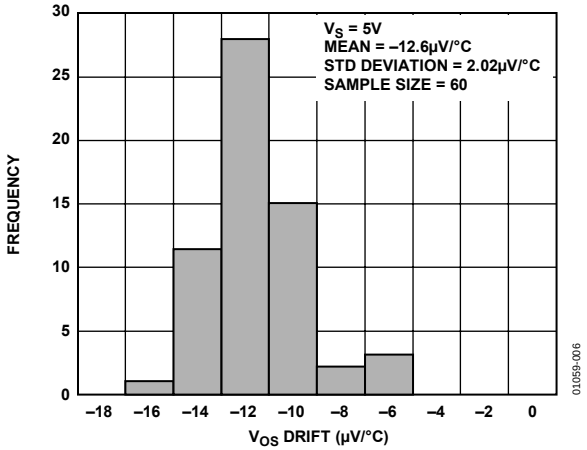


Figure 6. V_{OS} Drift Over –40°C to +85°C

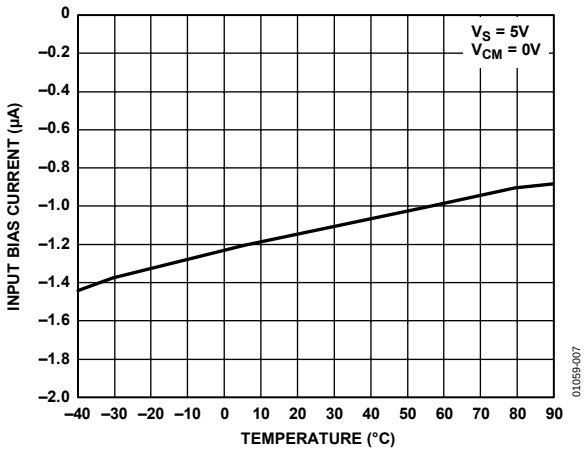


Figure 7. I_B vs. Temperature

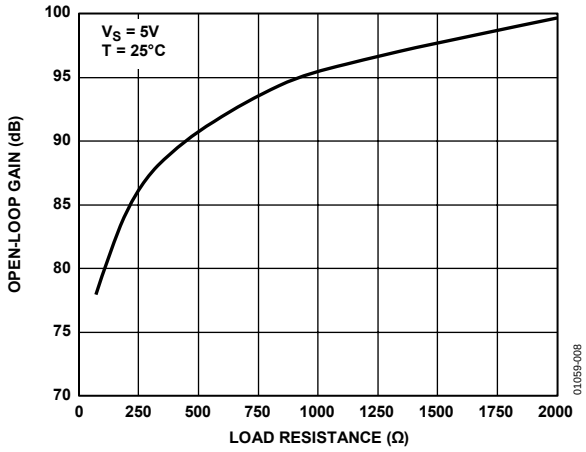


Figure 8. Open-Loop Gain vs. R_L to 2.5 V

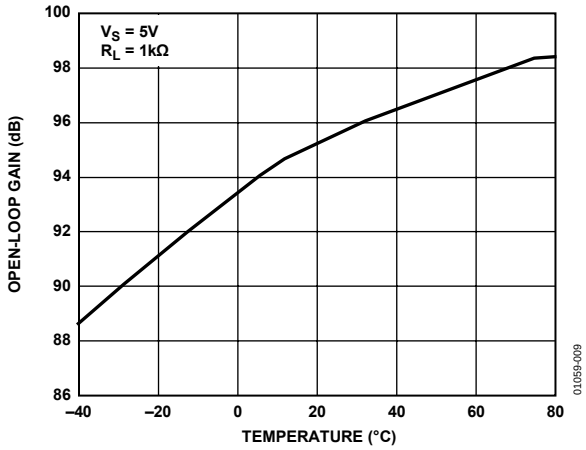


Figure 9. Open-Loop Gain vs. Temperature

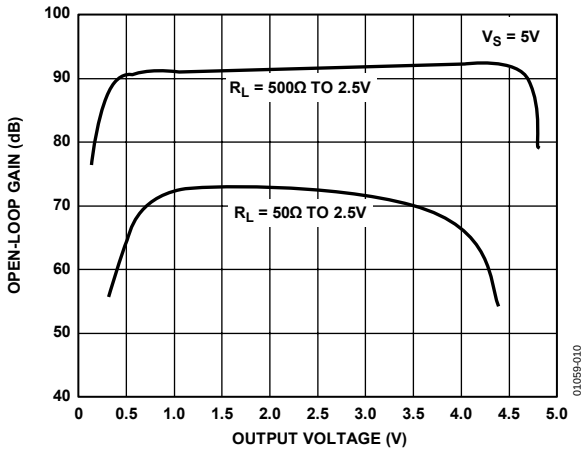


Figure 10. Open-Loop Gain vs. Output Voltage

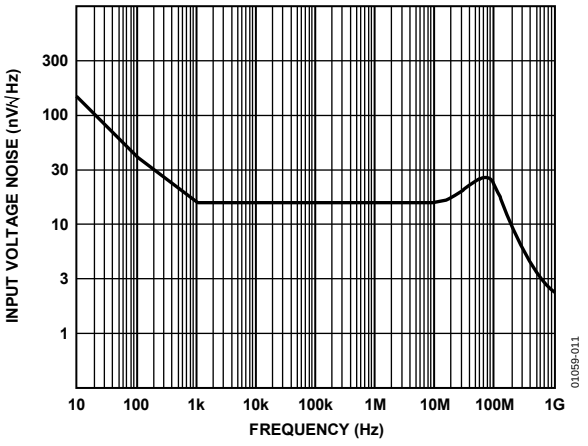


Figure 11. Input Voltage Noise vs. Frequency

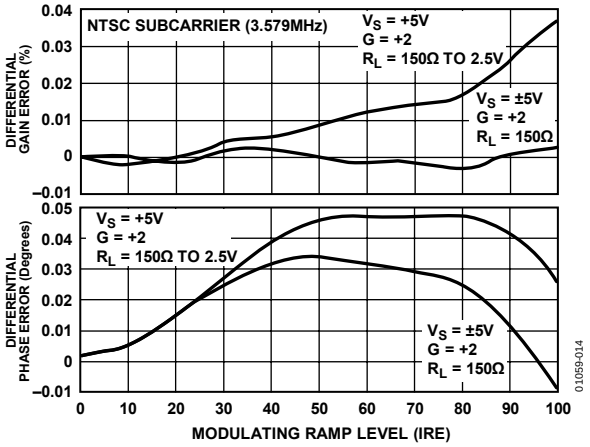


Figure 14. Differential Gain and Phase Errors

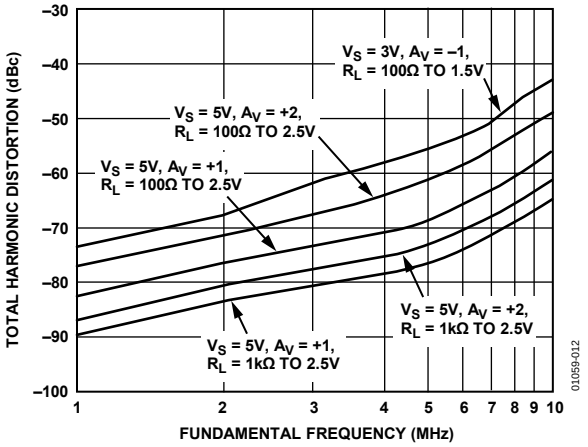


Figure 12. Total Harmonic Distortion vs. Frequency

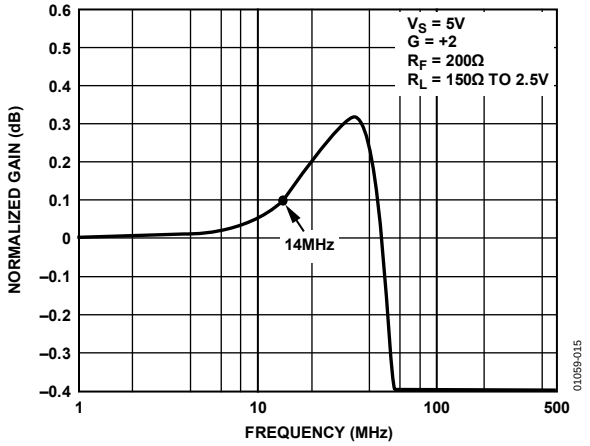


Figure 15. 0.1 dB Gain Flatness

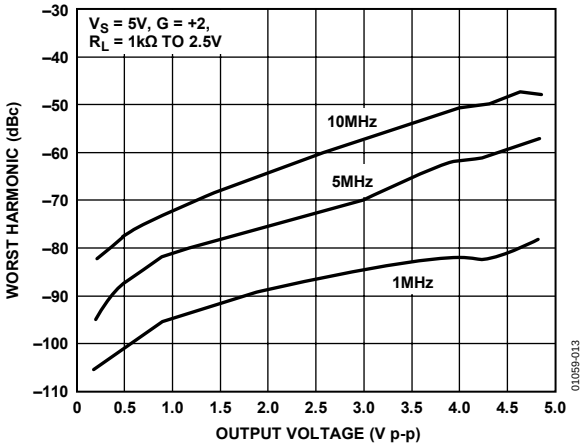


Figure 13. Worst Harmonic vs. Output Voltage

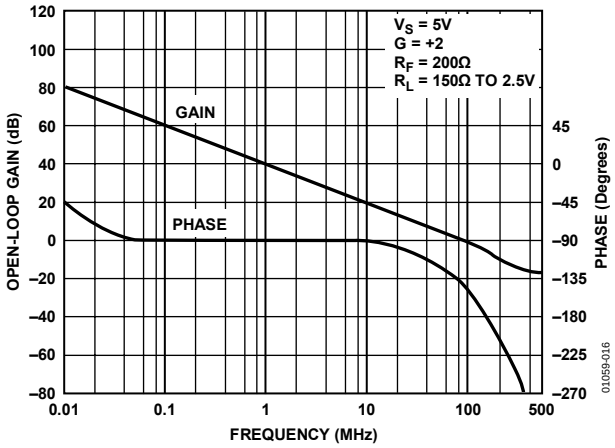


Figure 16. Open-Loop Gain and Phase vs. Frequency

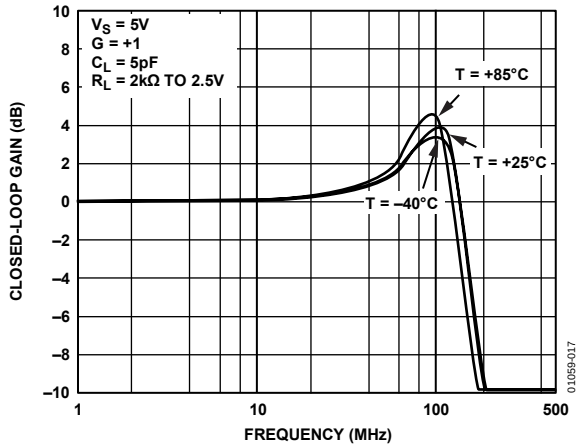


Figure 17. Closed-Loop Frequency Response vs. Temperature

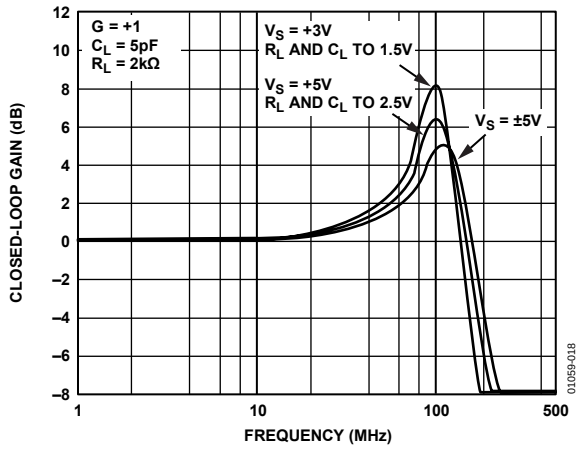


Figure 18. Closed-Loop Frequency Response vs. Supply

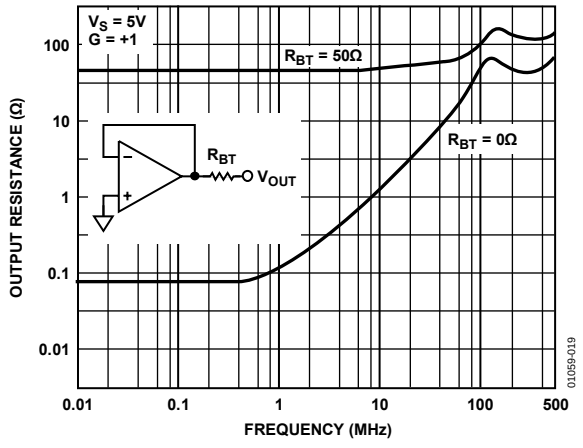


Figure 19. Output Resistance vs. Frequency

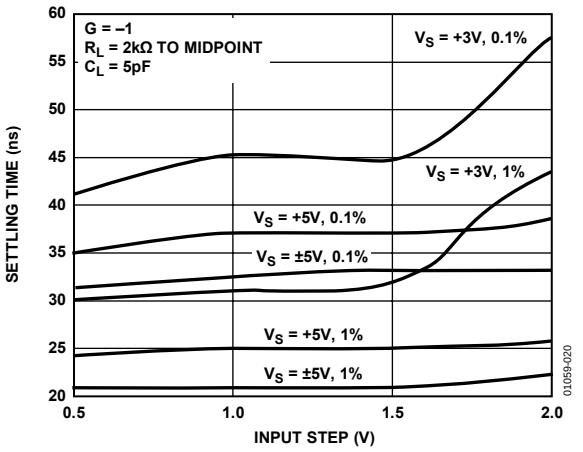


Figure 20. Settling Time vs. Input Voltage

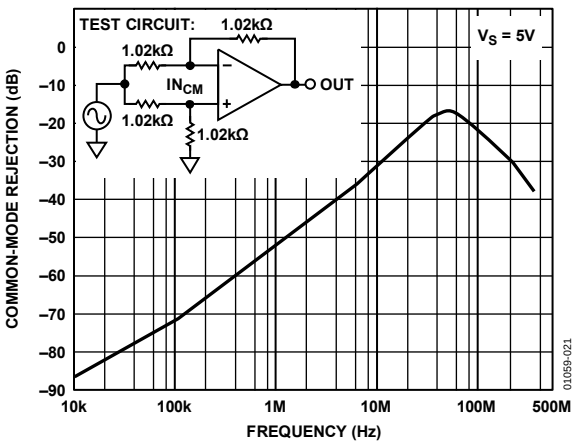


Figure 21. Common-Mode Rejection vs. Frequency

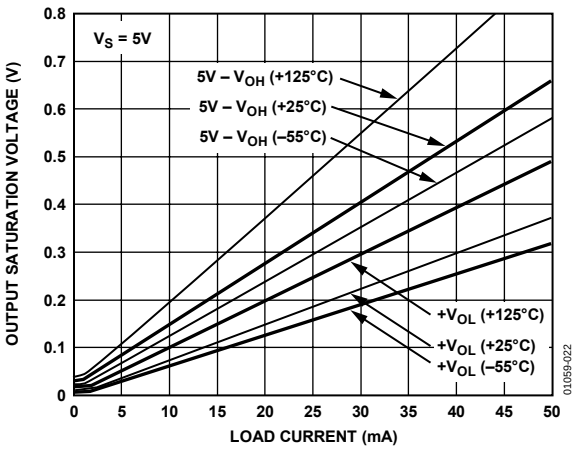


Figure 22. Output Saturation Voltage vs. Load Current

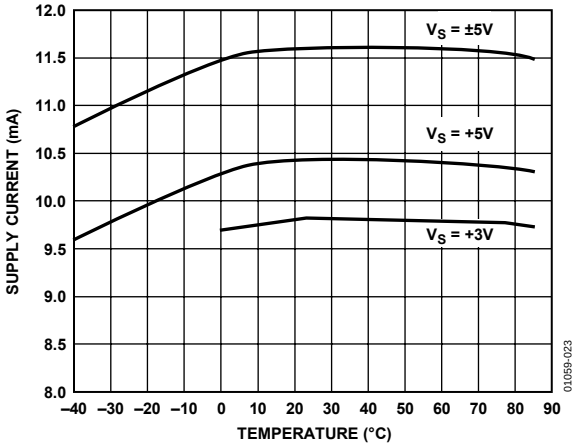


Figure 23. Supply Current vs. Temperature

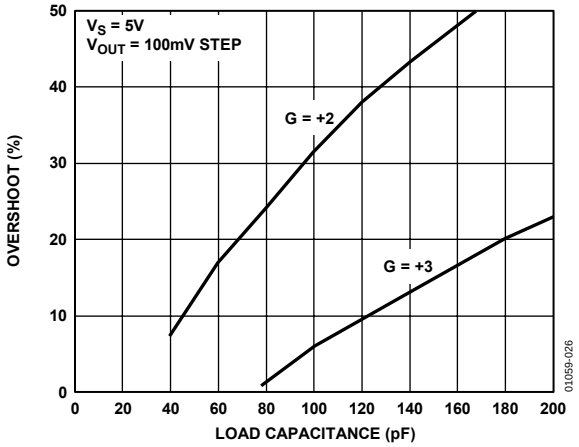


Figure 26. Overshoot vs. Load Capacitance

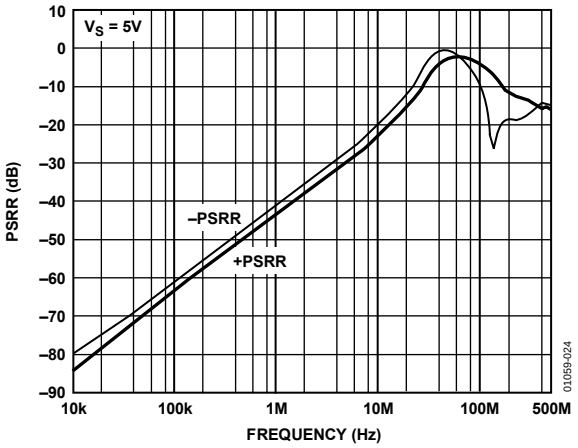


Figure 24. PSRR vs. Frequency

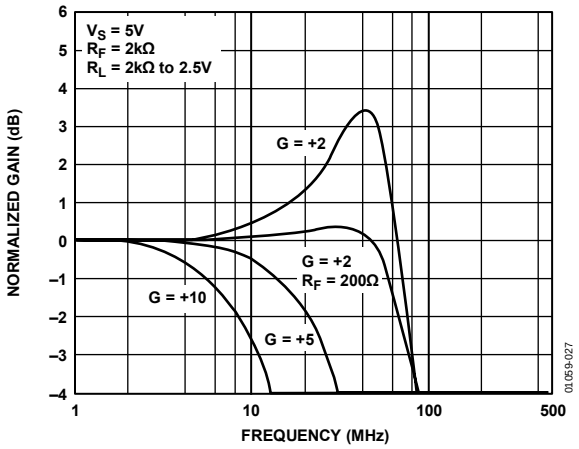


Figure 27. Closed-Loop Gain vs. Frequency Response

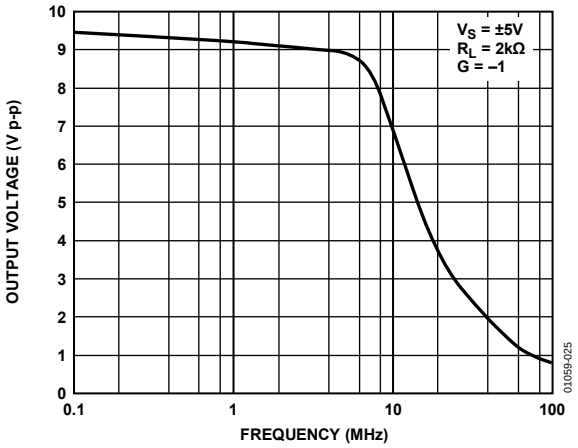


Figure 25. Output Voltage vs. Frequency

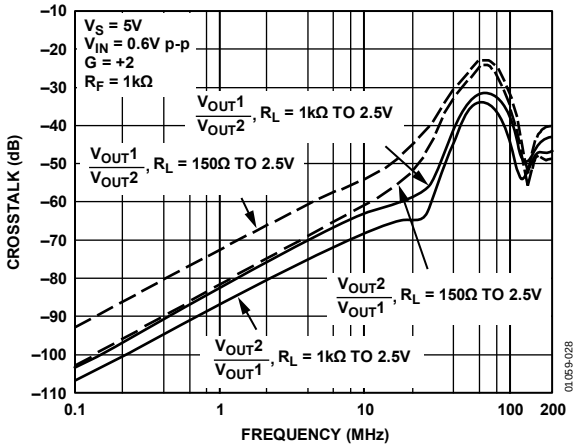


Figure 28. Crosstalk (Output-to-Output) vs. Frequency

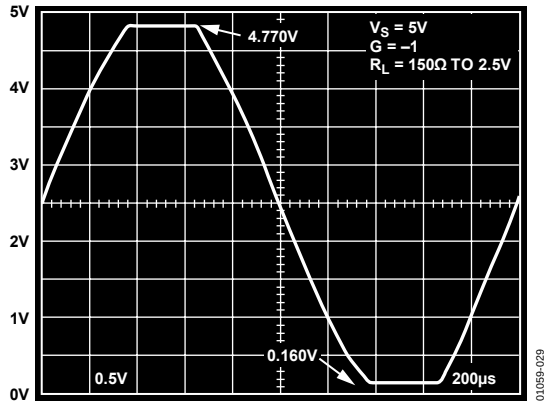


Figure 29. Output Swing with Load Reference to Supply Midpoint

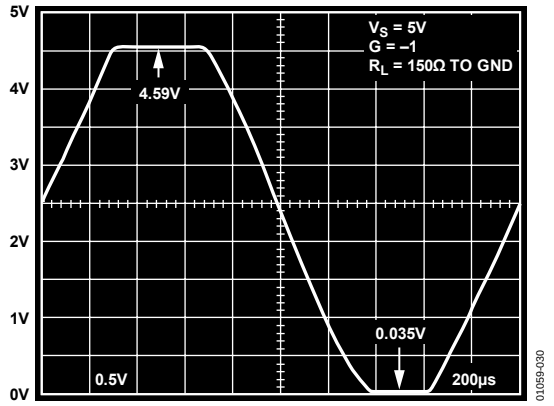


Figure 30. Output Swing with Load Reference to Negative to Supply

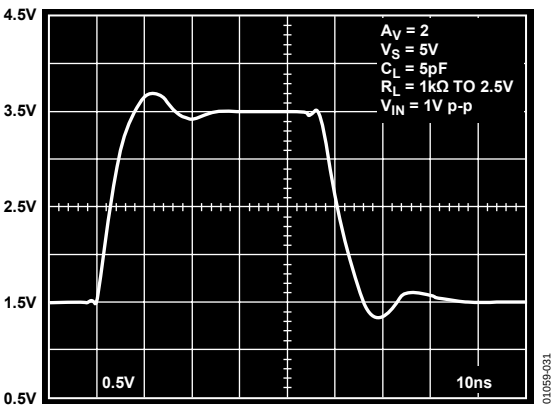


Figure 31. 1 V Pulse Response, V_S = 5 V

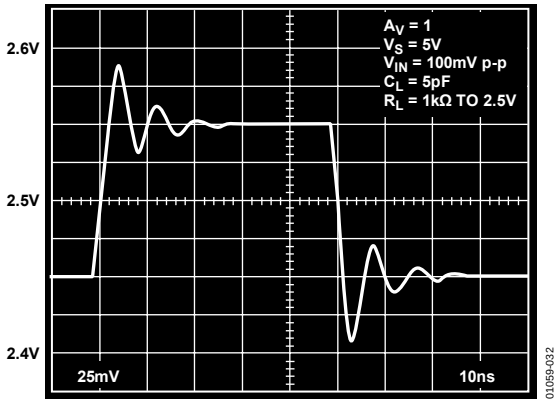


Figure 32. 100 mV Pulse Response, V_S = 5 V

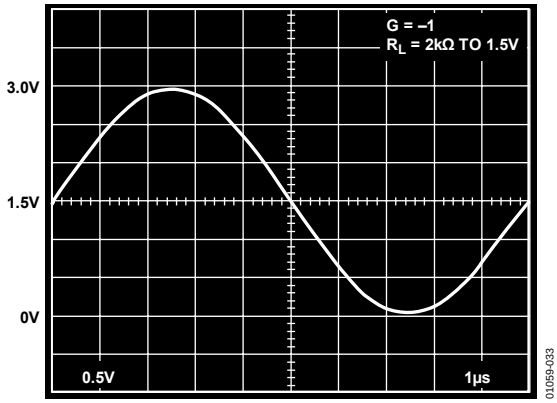


Figure 33. Rail-to-Rail Output Swing, V_S = 3 V

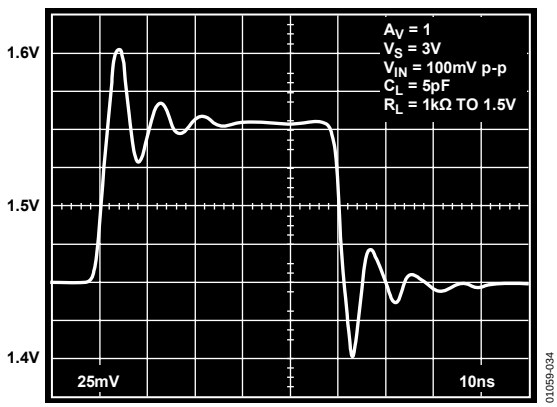


Figure 34. 100 mV Pulse Response, V_S = 3 V

APPLICATIONS INFORMATION

CIRCUIT DESCRIPTION

The AD8042 is fabricated on the Analog Devices, Inc., proprietary eXtra-Fast Complementary Bipolar (XFCB) process, which enables the construction of PNP and NPN transistors with similar f_ts in the 2 GHz to 4 GHz region. The process is dielectrically isolated to eliminate the parasitic and latch-up problems caused by junction isolation. These features allow the construction of high frequency, low distortion amplifiers with low supply currents. This design uses a differential output input stage to maximize bandwidth and headroom (see Figure 35). The smaller signal swings required on the first stage outputs (nodes SIP, SIN) reduce the effect of nonlinear currents due to junction capacitances and improve the distortion performance. With this design, harmonic distortion of better than −77 dB @ 1 MHz into 100 Ω with V_{OUT} = 2 V p-p (gain = +2) on a single 5 V supply is achieved.

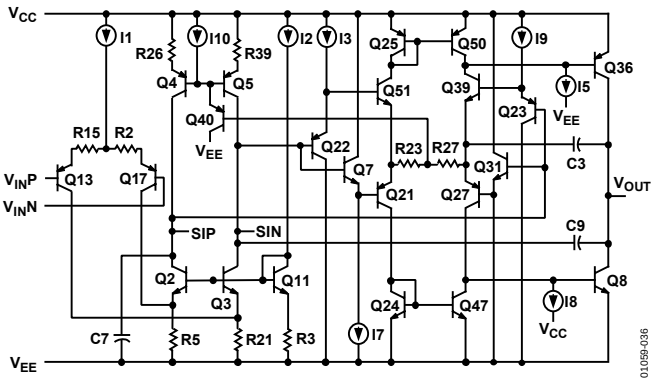


Figure 35. Simplified Schematic

The rail-to-rail output range of the AD8042 is provided by a complementary common-emitter output stage. High output drive capability is provided by injecting all output stage predriver currents directly into the bases of the output devices Q8 and Q36. Biasing of Q8 and Q36 is accomplished by I8 and I5, along with a common-mode feedback loop (not shown). This circuit topology allows the AD8042 to drive 40 mA of output current with the outputs within 0.5 V of the supply rails.

On the input side, the device can handle voltages from 0.2 V below the negative rail to within 1.2 V of the positive rail. Exceeding these values does not cause phase reversal; however, the input ESD devices do begin to conduct if the input voltages exceed the rails by greater than 0.5 V.

DRIVING CAPACITIVE LOADS

The capacitive load drive of the AD8042 can be increased by adding a low valued resistor in series with the load. Figure 36 shows the effects of a series resistor on capacitive drive for varying voltage gains. As the closed-loop gain is increased, the larger phase margin allows for larger capacitive loads with less overshoot. Adding a series resistor with lower closed-loop gains accomplishes the same effect. For large capacitive loads, the frequency response of the amplifier is dominated by the roll-off of the series resistor and capacitive load.

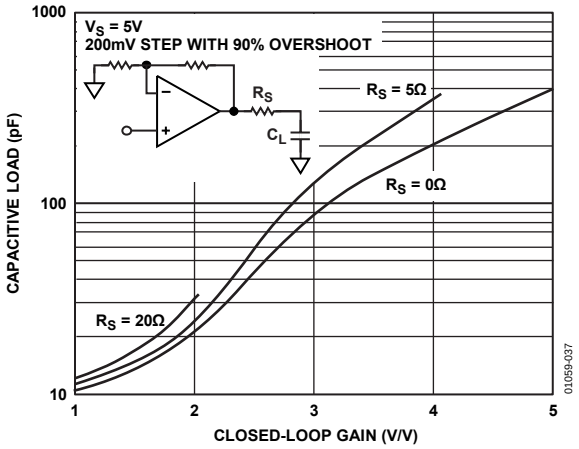


Figure 36. Capacitive Load Drive vs. Closed-Loop Gain

OVERDRIVE RECOVERY

Overdrive of an amplifier occurs when the output and/or input range are exceeded. The amplifier must recover from this overdrive condition. As shown in Figure 37, the AD8042 recovers within 30 ns from negative overdrive and within 25 ns from positive overdrive.

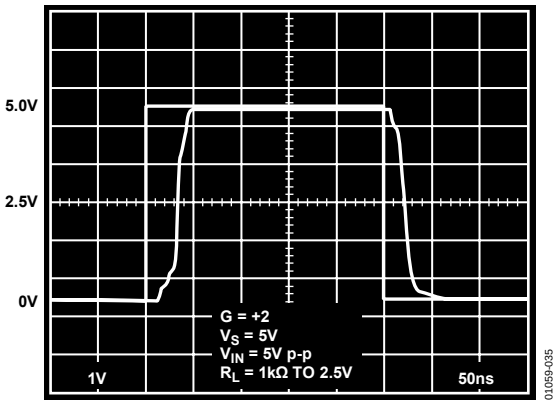


Figure 37. Overdrive Recovery

Single-Supply Composite Video Line Driver

The two op amps of an AD8042 can be configured as a single-supply dual line driver for composite video. The wide signal swing of the AD8042 enables this function to be performed without using any type of clamping or dc restore circuit, which can cause signal distortion.

Figure 38 shows a schematic for a circuit that is driven by a single composite video source that is ac-coupled, level-shifted and applied to both noninverting inputs of the two amplifiers. Each op amp provides a separate 75 Ω composite video output. To obtain single-supply operation, ac coupling is used throughout. The large capacitor values are required to ensure that there is minimal tilting of the video signals due to their low frequency (30 Hz) signal content. The circuit shown was measured to have a differential gain of 0.06% and a differential phase of 0.06°.

The input is terminated in 75 Ω and ac-coupled via C_{IN} to a voltage divider that provides the dc bias point to the input. Setting the optimal bias point requires some understanding of the nature of composite video signals and the video performance of the AD8042.

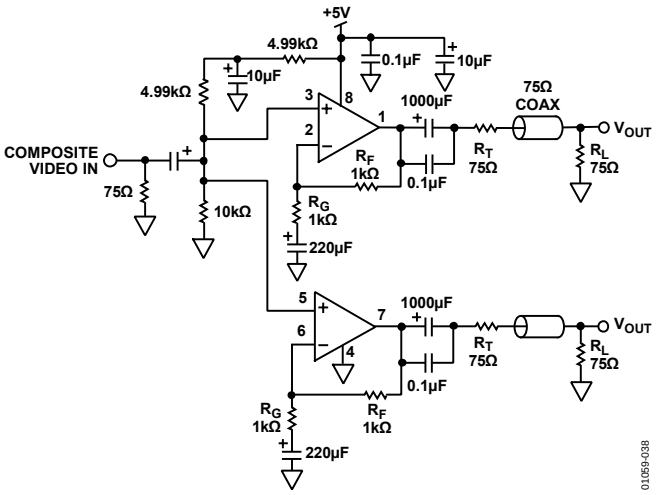


Figure 38. Single-Supply Composite Video Line Driver Using AD8042

Signals of bounded peak-to-peak amplitude that vary in duty cycle require larger dynamic swing capability than their peak-to-peak amplitude after ac coupling. As a worst case, the dynamic signal swing required approaches twice the peak-to-peak value. The two bounding cases are for a duty cycle that is mostly low, but occasionally goes high at a fraction of a percent duty cycle, and vice versa.

Composite video is not quite this demanding. One bounding extreme is for a signal that is mostly black for an entire frame but has a white (full intensity), minimum width spike at least once per frame.

The other extreme is for a video signal that is full white everywhere. The blanking intervals and sync tips of such a signal have negative going excursions in compliance with composite video specifications. The combination of horizontal and vertical blanking intervals limit such a signal to being at its highest level (white) for only about 75% of the time.

As a result of the duty cycle variations between the two extremes presented, a 1 V p-p composite video signal that is multiplied by a gain of 2 requires about 3.2 V p-p of dynamic voltage swing at the output for an op amp to pass a composite video signal of arbitrary duty cycle without distortion.

Some circuits use a sync tip clamp along with ac coupling to hold the sync tips at a relatively constant level, which lowers the amount of dynamic signal swing required. However, these circuits can have artifacts, such as sync tip compression, unless they are driven by sources with very low output impedance.

The AD8042 not only has ample signal swing capability to handle the dynamic range required without using a sync tip clamp but also has good video specifications such as differential gain and differential phase when buffering these signals in an ac-coupled configuration.

To test the dynamic range, the differential gain and differential phase were measured for the AD8042 while the supplies were varied. As the lower supply is raised to approach the video signal, the first effect observed is that the sync tips become compressed before the differential gain and differential phase are adversely affected. Therefore, there must be adequate swing in the negative direction to pass the sync tips without compression.

As the upper supply is lowered to approach the video, the differential gain and differential phase was not significantly affected until the difference between the peak video output and the supply reached 0.6 V. Therefore, the highest video level should be kept at least 0.6 V below the positive supply rail.

Therefore, it was found that the optimal point to bias the noninverting input is at 2.2 V dc. Operating at this point, the worst-case differential gain is measured at 0.06% and the worst-case differential phase is 0.06°.

The ac-coupling capacitors used in the circuit at first glance appear quite large. A composite video signal has a lower frequency band edge of 30 Hz. The resistances at the various ac coupling points, especially at the output, are quite small. To minimize phase shifts and baseline tilt, the large value capacitors are required. For video system performance that is not to be of the highest quality, the value of these capacitors can be reduced by a factor of up to five with only a slightly observable change in the picture quality.

Single-Ended-to-Differential Driver

Using a cross-coupled, single-ended-to-differential converter (SEDC), the AD8042 makes a good general-purpose differential line driver. This SEDC can be used for applications such as driving Category-5 (CAT-5) twisted pair wires. Figure 39 shows a configuration for a circuit that performs this function that can be used for video transmission over a differential pair or various data communication purposes.

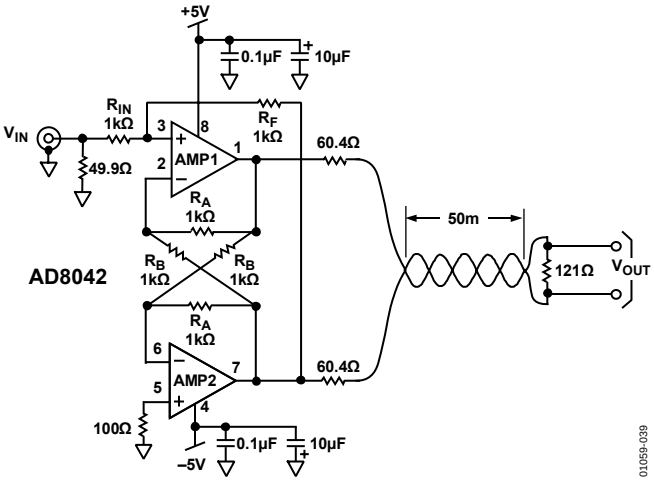


Figure 39. Single-Ended-to-Differential Twisted Pair Line Driver

Each of the op amps of the AD8042 is configured as a unity gain follower by the feedback resistors (R_A). Each op amp output also drives the other as a unity gain inverter via R_B, creating a totally symmetrical circuit.

If the noninverting input of AMP2 is grounded and a small positive signal is applied to the noninverting input of AMP1, the output of AMP1 is driven to saturation in the positive direction and the input of AMP2 is driven to saturation in the negative direction. This is similar to the way a conventional op amp behaves without any feedback.

If a resistor (R_F) is connected from the output of AMP2 to the noninverting input of AMP1, negative feedback is provided, which closes the loop. An input resistor (R_{IN}) makes the circuit look like a conventional inverting op amp configuration with differential outputs.

The gain of this circuit from input to either output is $\pm R_F/R_{IN}$, or the single-ended-to-differential gain is $2 \times R_F/R_{IN}$. This gives the circuit the advantage of being able to adjust its gain by changing a single resistor.

The cable has a characteristic impedance of about 120 Ω. Each driver output is back terminated with a pair of 60.4 Ω resistors to make the source look like 120 Ω. The receive end is terminated with 121 Ω, and the signal is measured differentially with a pair of scope probes. One channel on the oscilloscope is inverted and then the signals are added.

Figure 40 shows the results of the circuit in Figure 39 driving 50 meters of CAT-5 cable.

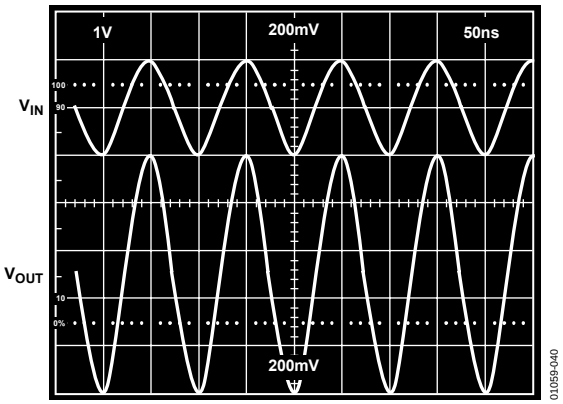


Figure 40. Differential Driver Frequency Response

Single-Supply Differential A/D Driver

The single-ended-to-differential converter circuit is also useful as a differential driver for video speed, single-ended, differential input ADCs. Figure 41 is a schematic that shows such a circuit differentially driving an AD9220, a 12-bit, 10 MSPS ADC.

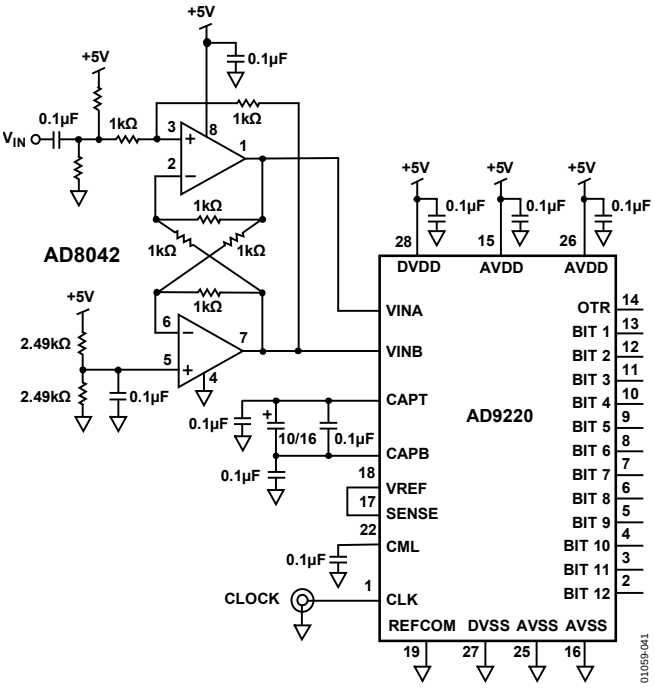


Figure 41. AD8042 Differential Driver for the AD9220 12-Bit, 10 MSPS ADC

The circuit was tested with a 1 MHz input signal and clocked at 10 MHz. An FFT response of the digital output is shown in Figure 42.

Pin 5 is biased at 2.5 V by the voltage divider and bypassed. This biases each output at 2.5 V. V_{IN} is ac-coupled such that V_{IN} going positive makes VINA go positive and VINB go in the negative direction. The opposite happens for a negative going V_{IN}.

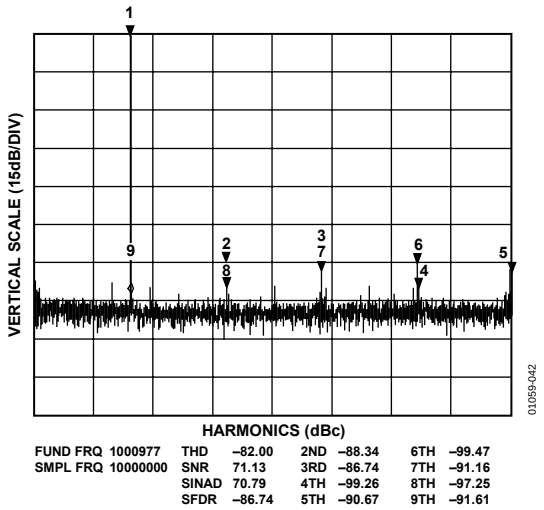


Figure 42. FFT of the AD9220 Output When Driven by the AD8042

HDSL Line Driver

High bit rate digital subscriber line (HDSL) is a popular means of providing data communication at DS1 rates (1.544 Mbps) over moderate distances via conventional telephone twisted pair wires. In these systems, the transceiver at the customer's end is powered sometimes via the twisted pair from a power source at the central office. Sometimes, it is required to raise the dc voltage of the power source to compensate for IR drops in long lines or lines with narrow gauge wires.

Because of the IR drop, it is highly desirable to keep the power consumption of the customer's transceiver as low as possible. One means to realize significant power savings is to run the transceiver from a ±5 V supply instead of the more conventional ±12 V.

The high output swing and current drive capability of the AD8042 make it ideally suited to this application. Figure 43 shows a circuit for the analog portion of an HDSL transceiver using the AD8042 as the line driver.

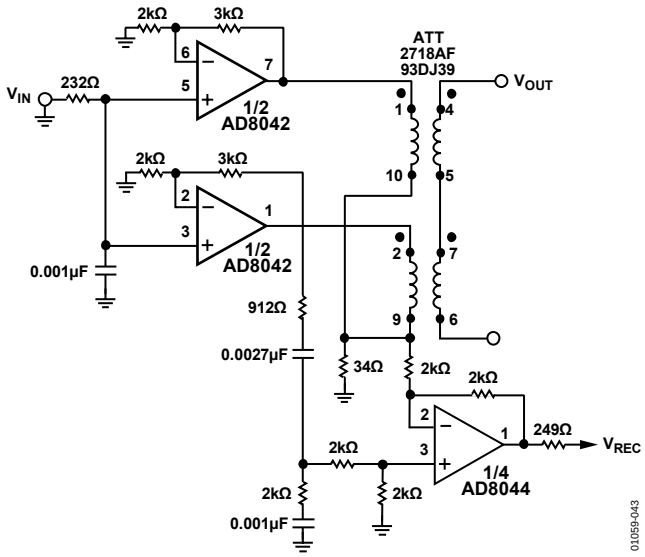


Figure 43. HDSL Line Driver

LAYOUT CONSIDERATIONS

The specified high speed performance of the AD8042 requires careful attention to board layout and component selection. Proper RF design techniques and low-pass parasitic component selection are necessary.

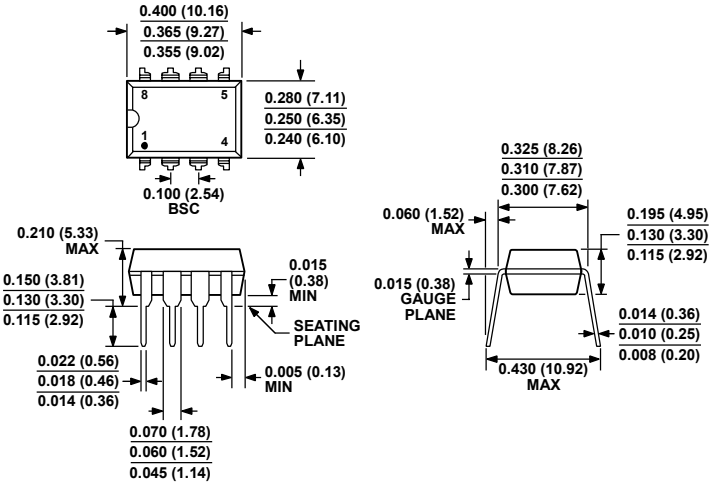
The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path. The ground plane should be removed from the area near the input pins to reduce the stray capacitance.

Chip capacitors should be used for the supply bypassing. One end should be connected to the ground plane and the other within ⅛-inch of each power pin. An additional large (0.47 µF to 10 µF) tantalum electrolytic capacitor should be connected in parallel, but not necessarily so close to supply current, for fast, large signal changes at the output.

The feedback resistor should be located close to the inverting input pin to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input significantly affect high speed performance.

Stripline design techniques should be used for long signal traces (greater than approximately one inch). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.

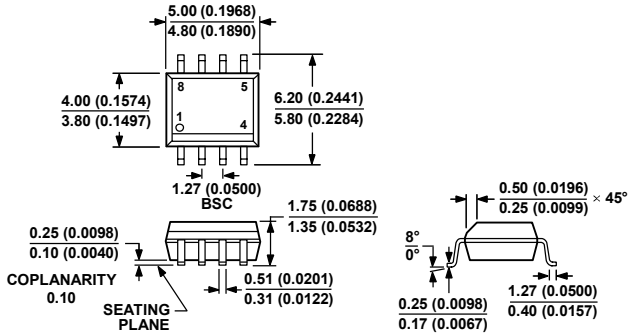
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 44. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body (N-8)—Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 45. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)—Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8042AN	–40°C to +85°C	8-Lead PDIP	N-8
AD8042AR	–40°C to +85°C	8-Lead SOIC_N	R-8
AD8042AR-REEL	–40°C to +85°C	8-Lead SOIC_N, 13" Reel	R-8
AD8042AR-REEL7	–40°C to +85°C	8-Lead SOIC_N, 7" Reel	R-8
AD8042ARZ[1]	–40°C to +85°C	8-Lead SOIC_N	R-8
AD8042ARZ-REEL[1]	–40°C to +85°C	8-Lead SOIC_N, 13" Reel	R-8
AD8042ARZ-REEL7[1]	–40°C to +85°C	8-Lead SOIC_N, 7" Reel	R-8
AD8042ACHIPS		DIE	

[1] Z = RoHS Compliant Part.

D01059-0-12/07(E)

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