Functional Diagram

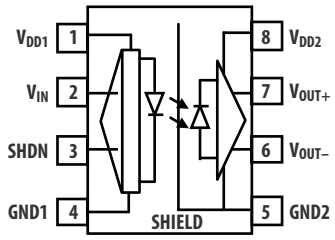


Figure 1.

NOTE: A 0.1 µF bypass capacitor must be connected between pins 1 and 4 and between pins 5 and 8.

Table 1. Pin Description

Pin No.	Symbol	Description
1	V_{DD1}	Supply voltage for input side (4.5 V to 5.5 V), relative to GND1
2	V_{IN}	Voltage input
3	SHDN	Shutdown pin (Active High)
4	GND1	Input side ground
5	GND2	Output side ground
6	V_{OUT-}	Negative output
7	V_{OUT+}	Positive output
8	V_{DD2}	Supply voltage for output side (3 V to 5.5 V), referenced to GND2

Ordering Information

ACPL-C87B/C87A/C870 is UL recognized with 5000 Vrms/1 minute rating per UL 1577.

Table 2.

Part number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-C87B	-000E	Stetched SO-8	X		X	80 per tube
ACPL-C87A ACPL-C870	-500E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

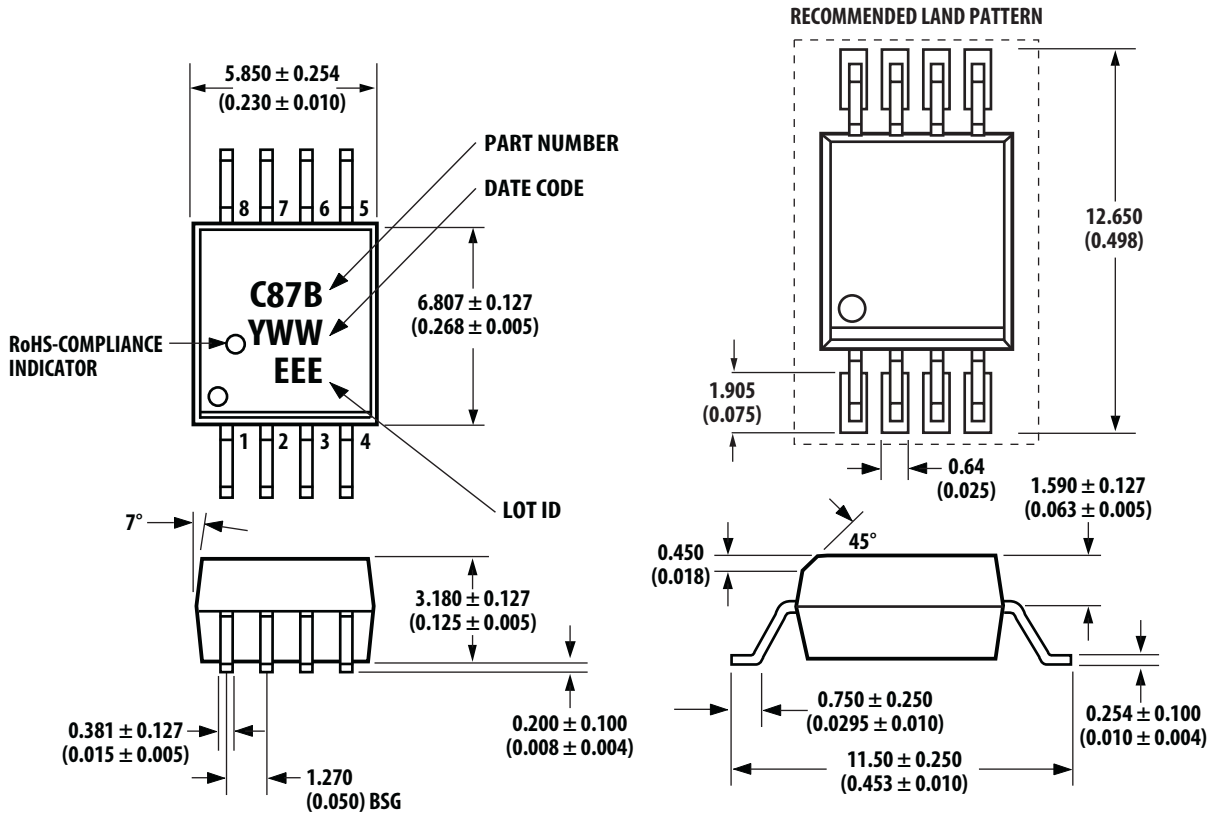
Example:

ACPL-C87A-500E to order product of Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and RoHS compliance.

Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawing

Stretched SO-8 Package (SSO-8)



Dimensions in millimeters and (inches).

Note:
Lead coplanarity = 0.1 mm (0.004 inches).
Floating lead protrusion = 0.25mm (10mils) max.

Figure 2. SSO-8 Package

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-C87B/C87A/C870 is approved by the following organizations:

IEC/EN/DIN EN 60747-5-5

Approval with Maximum Working Insulation Voltage V_{IORM} = 1414 V_{peak}.

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{rms}/1 min. File 55361.

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324

Table 3. Insulation and Safety Related Specifications

Parameter	Symbol	Value	Unit	Conditions
Minimum External Air Gap (External Clearance)	L(101)	8.0	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (External Creepage)	L(102)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 4. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics [1]

Description	Symbol	Value	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150 Vrms		I-IV	
for rated mains voltage ≤ 300 Vrms		I-IV	
for rated mains voltage ≤ 450 V rms		I-IV	
for rated mains voltage ≤ 600 Vrms		I-IV	
for rated mains voltage ≤ 1000 Vrms		I-III	
Climatic Classification		55/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage (Pending Qualification)	V_{IORM}	1414	Vpeak
Input to Output Test Voltage, Method b V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652	Vpeak
Input to Output Test Voltage, Method a V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	2262	Vpeak
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60 sec)	V_{IOTM}	8000	Vpeak
Safety-limiting values (Maximum values allowed in the event of a failure)			
Case Temperature	T_S	175	°C
Input Current [2]	$I_{S,INPUT}$	230	mA
Output Power [2]	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

Notes:
1. Insulation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits within the application.

Table 5. Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	+125	°C
Ambient Operating Temperature	T_A	-40	+105	°C
Supply Voltage	V_{DD1}, V_{DD2}	-0.5	6.0	V
Steady-State Input Voltage [1, 3]	V_{IN}	-2	V_{DD1} + 0.5	V
Two-Second Transient Input Voltage [2]	V_{IN}	-6	V_{DD1} + 0.5	V
Logic Input	V_{SD}	-0.5	V_{DD1} + 0.5	V
Output Voltages	V_{OUT+}, V_{OUT-}	-0.5	V_{DD2} + 0.5	V
Lead Solder Temperature	260° C for 10 sec., 1.6 mm below seating plane			

Notes:
1. DC voltage of up to -2 V on the inputs does not cause latch-up or damage to the device.
2. Transient voltage of 2 seconds up to -6 V on the inputs does not cause latch-up or damage to the device.
3. Absolute maximum DC current on the inputs = 100 mA, no latch-up or device damage occurs.

Table 6. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	-40	+105	°C
V_{DD1} Supply Voltage	V_{DD1}	4.5	5.5	V
V_{DD2} Supply Voltage	V_{DD2}	3.0	5.5	V
Input Voltage Range[1]	V_{IN}	0	2.0	V
Shutdown Enable Voltage	V_{SD}	V_{DD1} – 0.5	V_{DD1}	V

Notes:
1. 2 V is the nominal input range. Full scale input range (FSR) is 2.46 V.

Table 7. Electrical Specifications

Unless otherwise noted, T_A = -40° C to +105° C, V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3.3 V to 5.5 V, V_{IN} = 0 – 2 V, and V_{SD} = 0 V.

Parameter	Symbol	Min.	Typ.[1]	Max.	Unit	Test Conditions/Notes	Fig.
DC CHARACTERISTICS							
Input Offset Voltage	V_{OS}	-9.9	-0.3	9.9	mV	T_A = 25° C	3, 4
Magnitude of Input Offset Change vs. Temperature	$\lvert dV_{OS}/dT_A \rvert$		21		µV/°C	T_A = –40° C to +105° C ; Direct short across inputs.	5
Gain (ACPL-C87B, ±0.5%)	G0	0.995	1	1.005	V/V	T_A = 25° C; V_{DD2} = 5 V; Note 2.	6, 7
		0.994	0.999	1.004	V/V	T_A = 25° C; V_{DD2} = 3.3 V; Note 2.	6, 7
Gain (ACPL-C87A, ±1%)	G1	0.99	1	1.01	V/V	T_A = 25° C; Note 2.	6, 7
Gain (ACPL-C870, ±3%)	G3	0.97	1	1.03	V/V	T_A = 25° C; Note 2.	6, 7
Magnitude of Gain Change vs. Temperature	dG/dT_A		-35		ppm/°C	T_A = -40° C to +105° C	8
Nonlinearity	NL		0.05	0.1	%	V_{IN} = 0 to 2 V, T_A = 25° C	9, 10
Magnitude of NL Change vs. Temperature	$\lvert dNL/dT_A \rvert$		0.0002		%/°C	T_A = -40° C to +105° C	11
INPUTS AND OUTPUTS							
Recommended Input Range	VINR		2		V	Referenced to GND1	
Full-Scale Differential Voltage Input Range	FSR		2.46		V	Referenced to GND1	
Shutdown Logic Low Input Voltage	V_{IL}		0.8			T_A = 25° C	
Shutdown Logic High Input Voltage	V_{IH}	V_{DD} – 0.5	5			T_A = 25° C	
Input Bias Current	I_{IN}	-0.1	-0.0015		µA	V_{IN} = 0 V	
Magnitude of I_{IN} Change vs. Temperature	dI_{IN}/dT_A		1		nA/°C		
Equivalent Input Impedance	R_{IN}		1000		MΩ		
Output Common-Mode Voltage	V_{OCM}		1.23		V	V_{OUT+} or $V_{OUT–}$	
Output Voltage Range	VOUTR		Vocm ± 1.23		V	V_{SD} = 0 V. Note 4.	13
Output Short-Circuit Current	$\lvert I_{OSC} \rvert$		30		mA	V_{OUT+} or $V_{OUT–}$, shorted to GND2 or V_{DD2}	
Output Resistance	R_{OUT}		36		Ω	V_{OUT+} or $V_{OUT–}$	

Table 7. Electrical Specifications (continued)

Unless otherwise noted, T_A = -40° C to +105° C, V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3.3 V to 5.5 V, V_{IN} = 0 – 2 V, and V_{SD} = 0 V.

Parameter		Symbol	Min.	Typ.[1]	Max.	Unit	Test Conditions/Notes	Fig.
AC CHARACTERISTICS								
Vout Noise		N_{out}		0.013		mV_{rms}	Vin = 0 V; Output low-pass filtered to 180 KHz. Note 3.	12
Small-Signal Bandwidth (-3 dB)		$f_{-3\ dB}$	70	100		kHz	Guaranteed by design	
Input to Output Propagation Delay	50%-10%	t_{PD10}		2.2	3.0	µs	Step input.	18
	50%-50%	t_{PD50}		3.7	5.5	µs	Step input.	18
	50%-90%	t_{PD90}		5.3	6.5	µs	Step input.	18
Output Rise/Fall Time (10%-90%)		$t_{R/F}$		2.7	4.0	µs	Step input (t_{PD90} - t_{PD10})	
Shutdown Delay		t_{SD}		25	40	µs	Vin = 2 V	17
Enable Delay		t_{ON}		150	200	µs		
Common Mode Transient Immunity		CMTI	10	15		kV/µs	V_{CM} = 1 kV, T_A = 25° C	
Power Supply Rejection		PSR		-78		dB	1 Vpp 1 kHz sine wave ripple on V_{DD1}, differential output	
POWER SUPPLIES								
Input Side Supply Current		I_{DD1}		10.5	15	mA	V_{SD} = 0 V	
				15		µA	V_{SD} = 5 V	
		I_{DD2}		6.5	12	mA	5 V supply	
				6.1	11	mA	3.3 V supply	

Notes:
1. All Typical values are under Typical Operating Conditions at T_A = 25° C, V_{DD1} = 5 V, V_{DD2} = 5 V.
2. Gain is defined as the slope of the best-fit line of differential output voltage ($V_{OUT+} - V_{OUT-}$) versus input voltage over the nominal range, with offset error adjusted.
3. Noise is measured at the output of the differential to single ended post amplifier.
4. When is V_{SD} = 5 V or when shutdown is enabled, V_{out+} is close to 0V and V_{out-} is at close to 2.46 V. This is similar to when VDD1 is not supplied.

Table 8. Package Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			Vrms	RH < 50%, t = 1 min., T_A = 25° C	1, 2
Resistance (Input-Output)	R_{I-O}		$> 10^{12}$		Ω	V_{I-O} = 500 V_{DC}	3
Capacitance (Input-Output)	C_{I-O}		0.5		pF	f = 1 MHz	3

Notes:
1. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA). This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table.
2. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the IEC/EN/DIN EN 60747-5-5 insulation characteristics table and your equipment level safety specification.
3. This is a two-terminal measurement: pins 1–4 are shorted together and pins 5–8 are shorted together.

Typical Performance Plots

All ±3(sigma symbol) plots are based on characterization test result at the point of product release. For guaranteed specification, refer to the respective Electrical Specifications section.

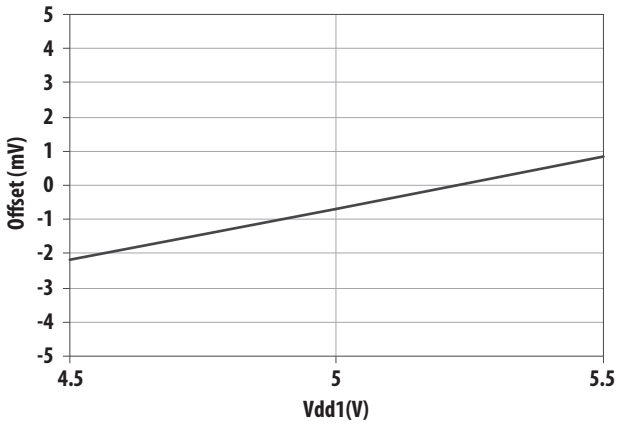


Figure 3. Input Offset vs Supply VDD1

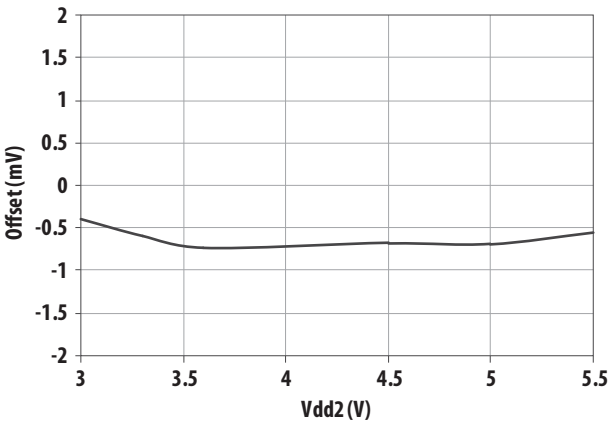


Figure 4. Input Offset vs Supply VDD2

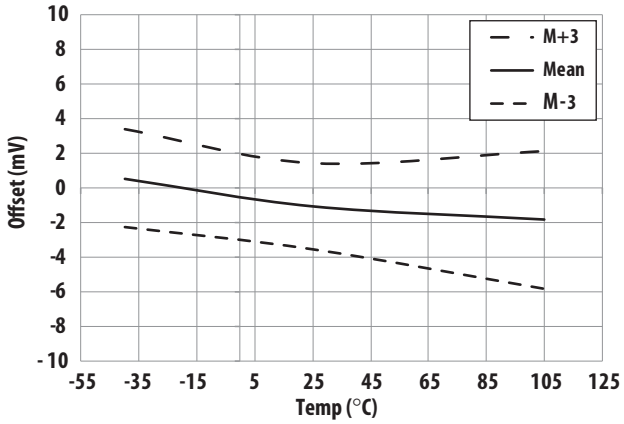


Figure 5. Input Offset vs Temperature

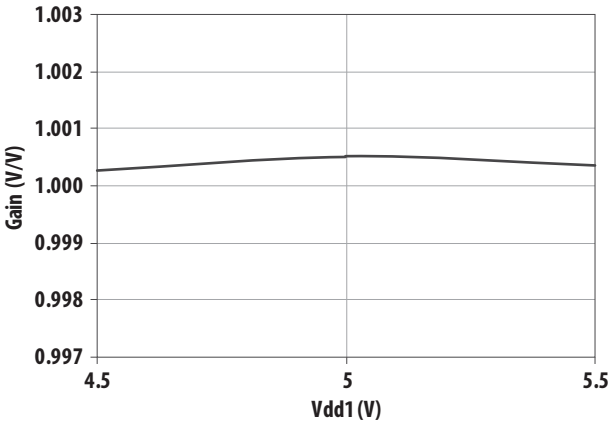


Figure 6. Gain vs Supply VDD1

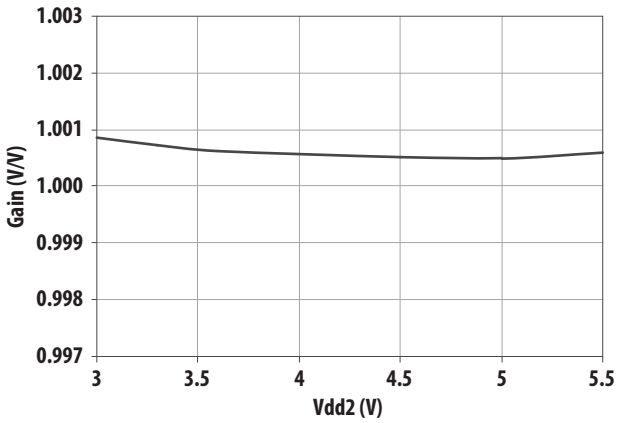


Figure 7. Gain vs Supply VDD2

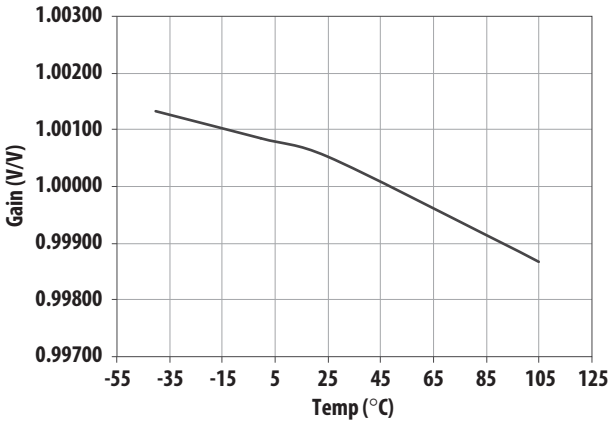


Figure 8. Gain vs Temperature

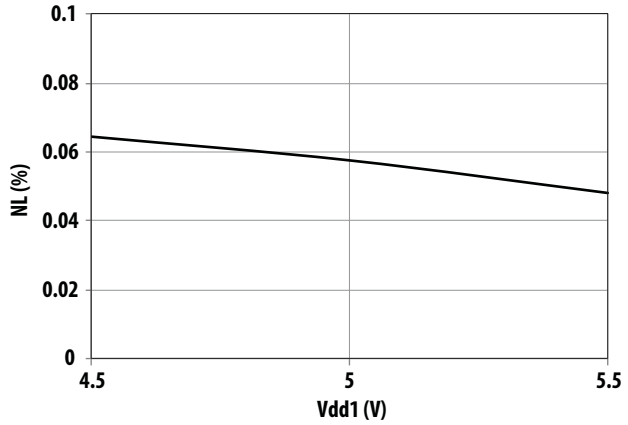


Figure 9. Non-Linearity vs Supply VDD1

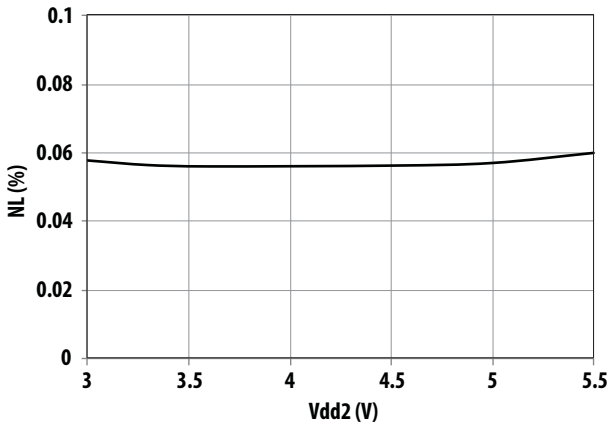


Figure 10. Non-Linearity vs Supply VDD2

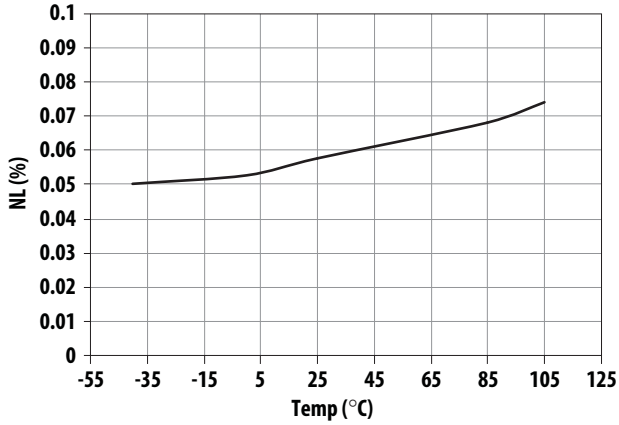


Figure 11. Non-Linearity vs Temperature

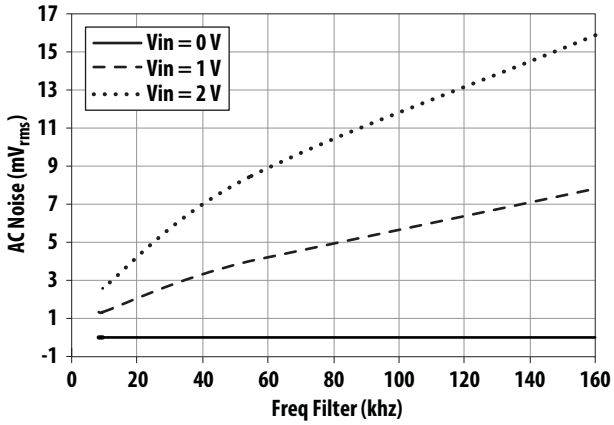


Figure 12. AC noise vs Filter Freq vs Vin

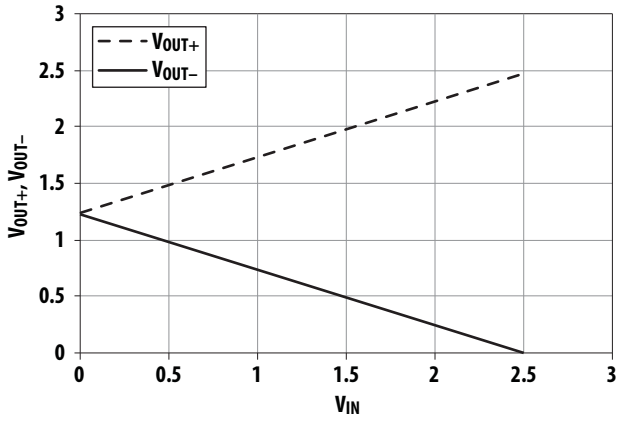


Figure 13 V_{IN} vs V_{OUT+}, V_{OUT-}

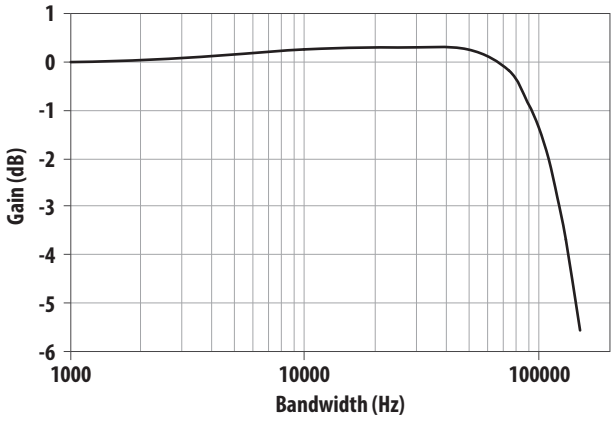


Figure 14. Frequency Response

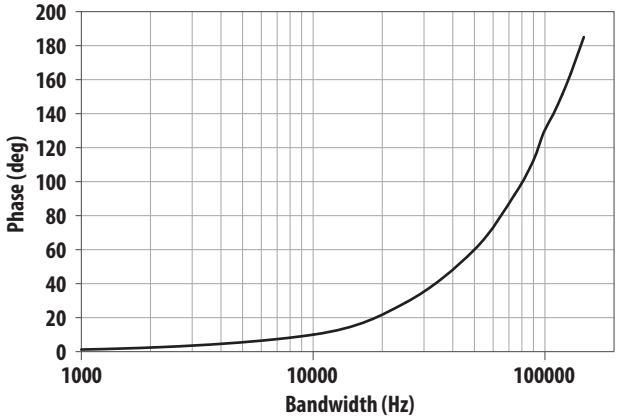


Figure 15. Phase Response

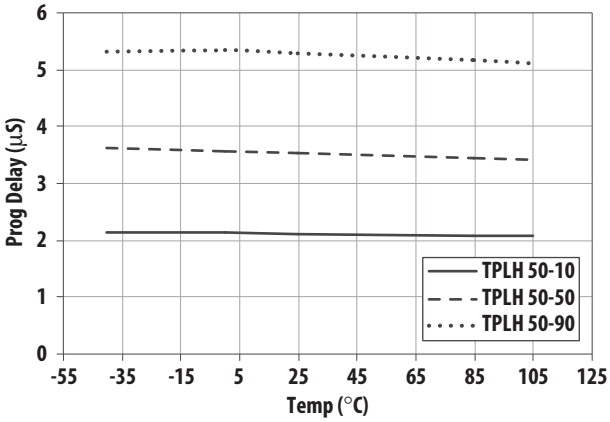


Figure 16. Propagation Delay vs Temperature

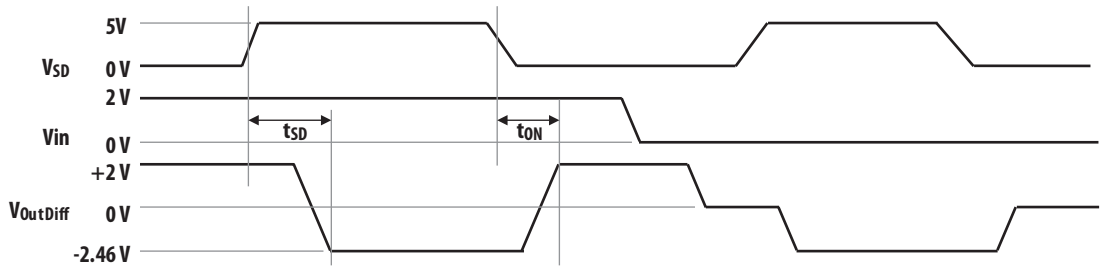


Figure 17. Shutdown And Wakeup Input To Output Timing Diagram. $V_{Out\ Diff} = V_{Out+} - V_{Out-}$

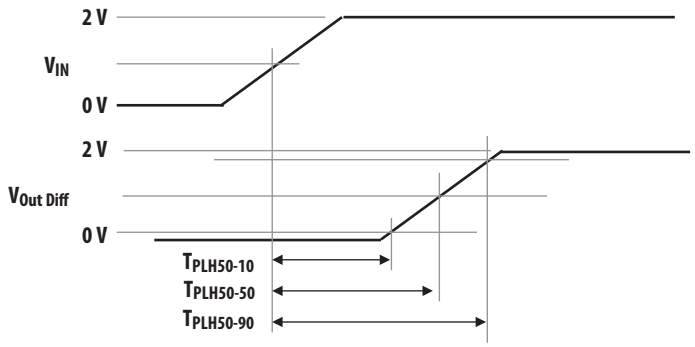


Figure 18. Input to Output Propagation Delay Timing Diagram. $V_{Out\ Diff} = V_{Out+} - V_{Out-}$

Definitions

Gain

Gain is defined as the slope of the best-fit line of differential output voltage ($V_{OUT+} - V_{OUT-}$) over the nominal input range, with offset error adjusted out.

Nonlinearity

Nonlinearity is defined as half of the peak-to-peak output deviation from the best-fit gain line, expressed as a percentage of the full-scale differential output voltage.

Common Mode Transient Immunity, CMTI, also known as Common Mode Rejection

CMTI is tested by applying an exponentially rising/falling voltage step on pin 4 (GND1) with respect to pin 5 (GND2). The rise time of the test waveform is set to approximately 50 ns. The amplitude of the step is adjusted until the differential output ($V_{OUT+} - V_{OUT-}$) exhibits more than a 200 mV deviation from the average output voltage for more than 1µs. The ACPL-C87x will continue to function if more than 10 kV/µs common mode slopes are applied, as long as the breakdown voltage limitations are observed.

Power Supply Rejection, PSR

PSRR is the ratio of differential amplitude of the ripple outputs over power supply ripple voltage, referred to the input, expressed in dB.

Application Information

Application Circuit

The typical application circuit is shown in Figure 19. The ACPL-C87X voltage sensor is often used in photovoltaic (PV) panel voltage measurement and tracking in PV inverters, and DC bus voltage monitoring in motor drivers. The high voltage across rails needs to be scaled down to fit the input range of the iso-amp by choosing R1 and R2 values according to appropriate ratio.

The ACPL-C87X senses the single-ended input signal and produces differential outputs across the galvanic isolation barrier. The differential outputs (Vout+, Vout-) can be connected to an op-amp to convert to a single-ended signal or directly to two ADCs. The op-amp used in the external post-amplifier circuit should be of sufficiently high precision so that it does not contribute a significant amount of offset or offset drift relative to the contribution from the isolation amplifier. Generally, op-amps with bipolar input stages exhibit better offset performance than op-amps with JFET or MOSFET input stages.

In addition, the op-amp should also have enough bandwidth and slew rate so that it does not adversely affect the response speed of the overall circuit. The post-amplifier circuit includes a pair of capacitors (C4 and C5) that form a single-pole low-pass filter; these capacitors allow the bandwidth of the post-amp to be adjusted independently of the gain and are useful for reducing the output noise from the isolation amplifier.

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate CMRR and adequate gain tolerance for the overall circuit. Resistor networks can be used that have much better ratio tolerances than can be achieved using discrete resistors. A resistor network also reduces the total number of components for the circuit as well as the required board space.

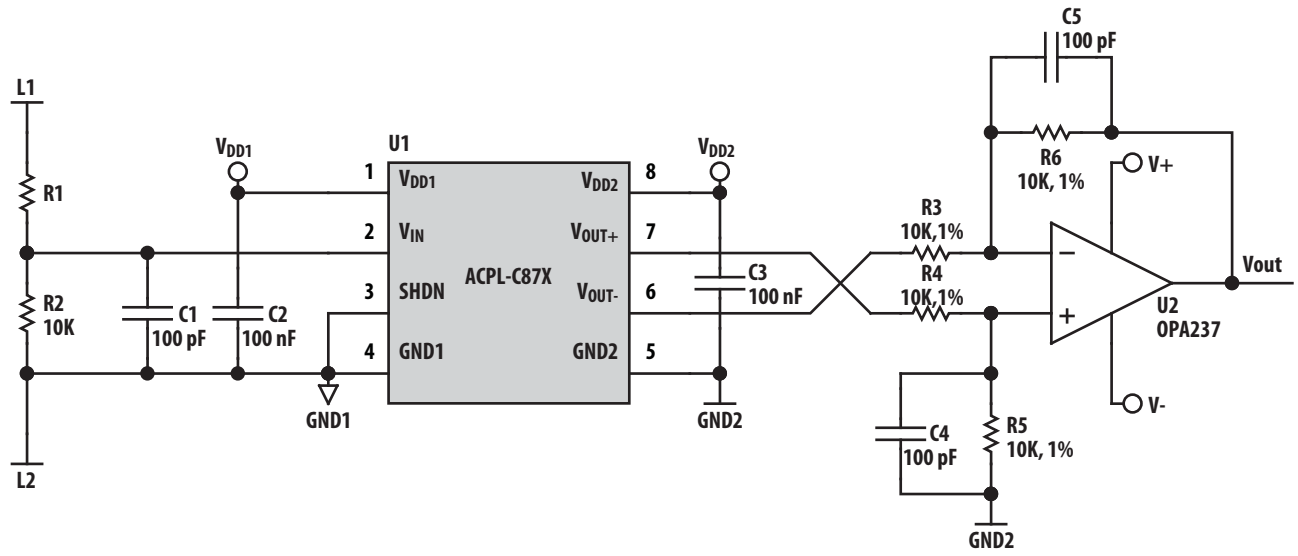


Figure 19. Typical application circuit.

Measurement Accuracy and Power Dissipation of the Resistive Divider

The input stage of the typical application circuit in Figure 19 can be simplified as the diagram shown in Figure 20. R2 and R_{IN}, input resistance of the ACPL-C87X, create a current divider that results in an additional measurement error component that will add on to the tot on top of the device gain error. With the assumption that R1 and R_{IN} have a much higher value than R2, the resulting error can be estimated to be $R2/R_{IN}$.

With R_{IN} of 1 GΩ for the ACPL-C87X, this additional measurement error is negligible with R2 up to 1 MΩ, where the error is approximately 0.1%. Though small, it can be further reduced by reducing the R2 to 100 kΩ (error of 0.01% approximately), or 10 kΩ (error of 0.001% approximately). However with lower R2, a drawback of higher power dissipation in the resistive divider string needs to be considered, especially in higher voltage sensing applications. For example, with 600 V DC across L1 and L2 and R2 of 100 kΩ for 0.01% measurement error, the resistive divider string consumes about 12 mW, assuming V_{IN} is set at 2 V. If the R2 is reduced to 10 kΩ to reduce error to 0.001%, the power consumption will increase to about 120 mW. In energy efficiency critical applications such as PV inverters and battery-powered applications, this trade-off between measurement accuracy and power dissipation in the resistive string provides flexibility in design priority.

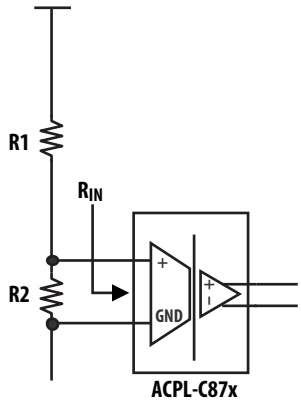


Figure 20. Simplified Input Stage.

Isolated Temperature Sensing using Thermistor

IGBTs are an integral part of a motor or servo drive system and because of the high power that they usually handle, it is essential that they have proper thermal management and are sufficiently cooled. Long term overload conditions could raise the IGBT module temperature permanently or failure of the thermal management system could subject the module to package overstress and lead to catastrophic failures. One common way to monitor the temperature of the module is through using a NTC type thermistor mounted onto the IGBT module. Some IGBT module manufacturers also have IGBTs that comes with the thermistor integrated inside the module. In some cases, it is necessary to isolate this thermistor to provide added isolation and insulation due to the high power nature of the IGBTs. The ACPL-C87x voltage sensor can be used to easily meet such a requirement, while providing good accuracy and non-linearity. Figure. 21 shows an example of such an implementation. The ACPL-C87x is used to isolate the thermistor voltage which is later fed by the post amp stage to an ADC onboard the microcontroller (MCU) to determine the module temperature. The thermistor needs to be biased in way that its voltage output will optimize the 2 V input range of the ACPL-C87x across the intended temperature measurement range.

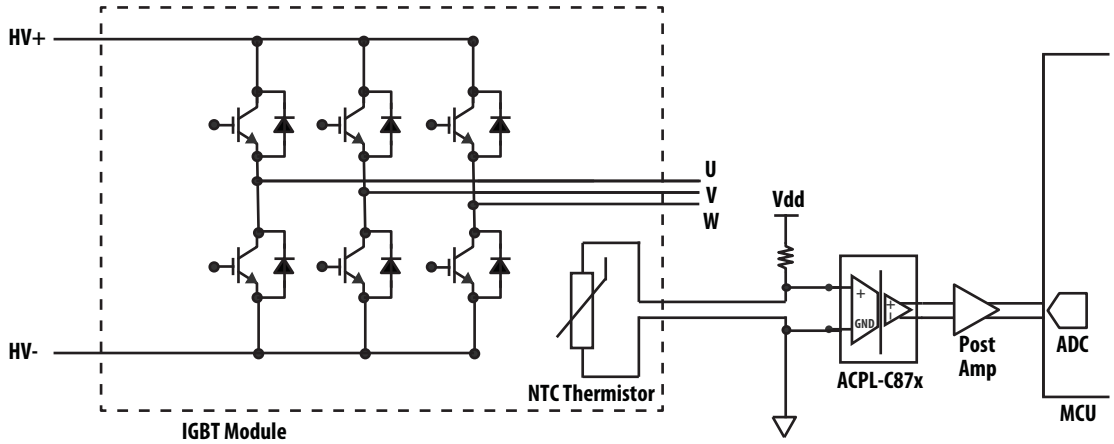


Figure 21. Thermistor sensing in IGBT Module

Power Supplies and Bypassing

A power supply of 5 V is required to power the ACPL-C87x input side VDD1. In many motor drive DC bus voltage sensing applications, this 5 V supply is most often obtained from the same supply used to power the power transistor gate drive circuit using an inexpensive 78L05 three-terminal regulator. To help attenuate high frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

In some other applications a dedicated supply might be required to supply the VDD1. These applications include photovoltaic (PV) inverter voltage tracking and measurement, temperature sensor signal isolation. In these cases it is possible to add an additional winding on an existing transformer. Otherwise, some sort of simple isolated supply can be used, such as a line powered transformer or a high-frequency DC-DC converter module.

As shown in Figure 22, 100 nF bypass capacitors (C2, C3) should be located as close as possible to the pins of the isolation amplifier. The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolation amplifier. A 100 pF bypass capacitor (Cin) is also recommended at the input pins due to the switched-capacitor nature of the input circuit. The input bypass capacitor Cin also forms part of the anti-aliasing filter, which is recommended to prevent high-frequency noise from aliasing down to lower frequencies and interfering with the input signal. When R1 is far greater than R2, the low-pass anti-aliasing filter corner frequency can be calculated by $1/(2\pi R2Cin)$. The input filter also performs an important reliability function – it reduces transient spikes from ESD events flowing through the high voltage rails.

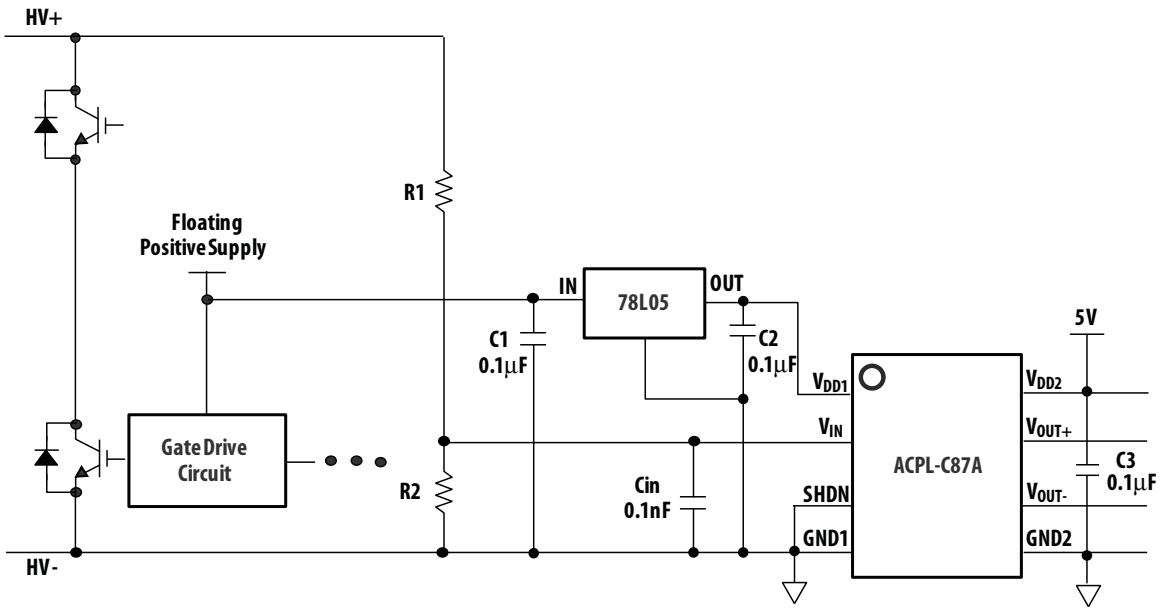


Figure 22. Recommended Power Supply and Bypassing

PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, the use of ground and power planes, etc. In addition, the layout of the PCB can also affect the isolation transient immunity (CMTI) of the ACPL-C87x, primarily due to stray capacitive coupling between the input and the output circuits. To obtain optimal CMTI performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the ACPL-C87A. The placement of the input capacitor which forms part of the anti-aliasing filter together with the resistor network should also be placed as close as possible to the Vin pin.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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