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## Pin Diagram

The device is packaged in a 6 x 6 mm 40-pin QFN.
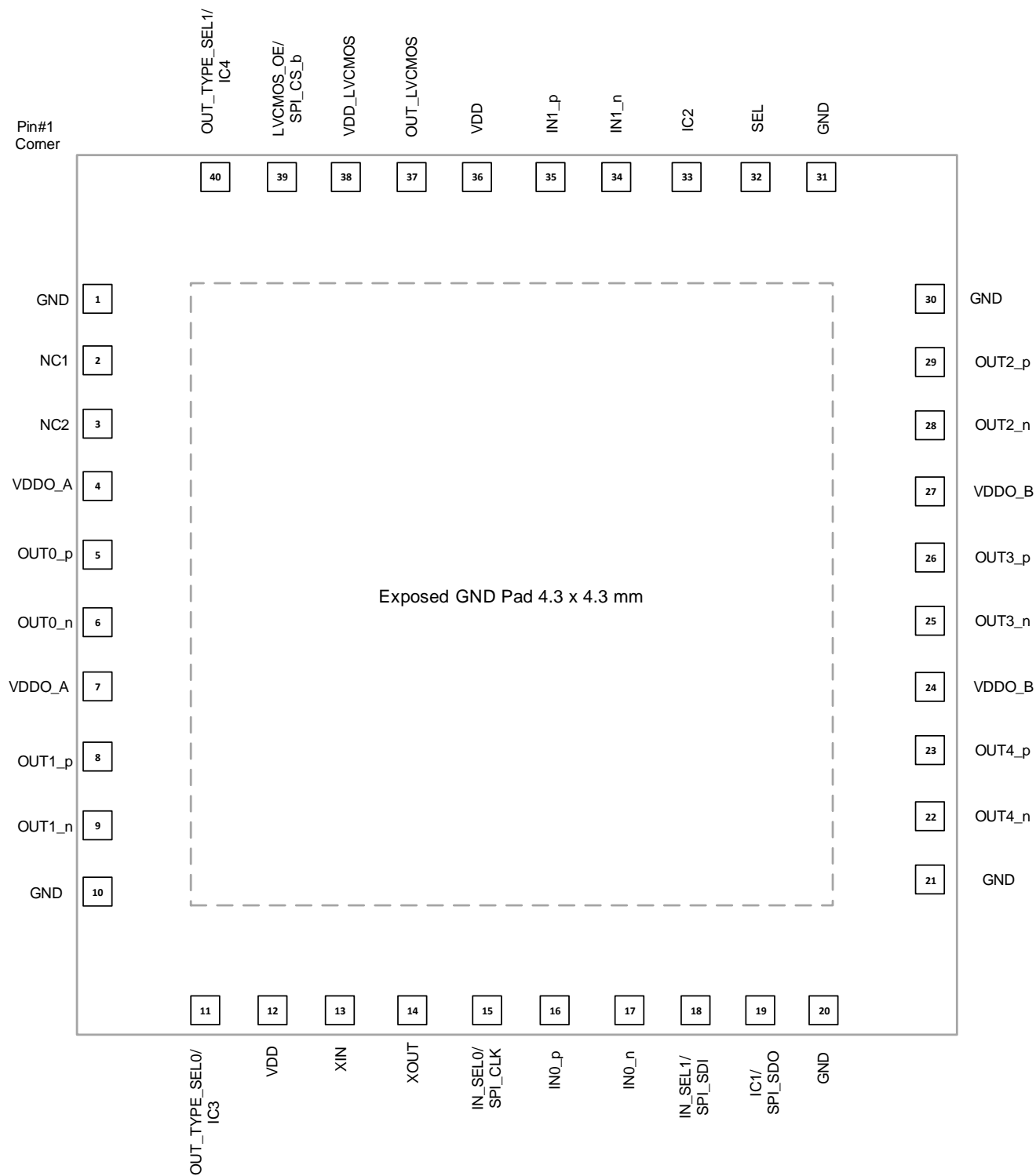


**Figure 2. Pin Diagram**

## Pin Descriptions

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, $I_{PU}$ – input with 300k$\Omega$ internal pull-up resistor, $I_{PD}$ – input with 300k$\Omega$ internal pull-down resistor, $I_{APU}$ – input with 31k$\Omega$ internal pull-up resistor, $I_{APD}$ – input with 30k$\Omega$ internal pull-down resistor, $I_{APU/APD}$ – input with 60k$\Omega$ internal pull-up and pull-down resistors (30 k$\Omega$ equivalent), O – output, I/O – Input/Output pin, NC – No connect, P – power supply pin.

### Table 1 Pin Description

| # | Name | I/O | Description |
|---|------|-----|-------------|
| **Input Reference** | | | |
| 16<br>17<br>35<br>34 | IN0_p<br>IN0_n<br>IN1_p<br>IN1_n | $I_{APD}$<br>$I_{APU/APD}$<br>$I_{APD}$<br>$I_{APU/APD}$ | **Input Differential or Single Ended References 0 and 1**<br><br>Input frequency range 0Hz to 1.6GHz.<br><br>Non inverting inputs (_p) are pulled down with internal 30k$\Omega$ pull-down resistors. Inverting inputs (_n) are biased at VDD/2 with 60k$\Omega$ pull-up and pull-down resistors to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference). |
| **Output Clocks** | | | |
| 5<br>6<br>8<br>9<br>29<br>28<br>26<br>25<br>23<br>22 | OUT0_p<br>OUT0_n<br>OUT1_p<br>OUT1_n<br>OUT2_p<br>OUT2_n<br>OUT3_p<br>OUT3_n<br>OUT4_p<br>OUT4_n | O | **Ultra Low Additive Jitter Differential LVPECL/HCSL/LVDS Outputs 0 to 4**<br><br>Output frequency range 0 to 1.6GHz<br><br>In SPI bus controlled mode (SEL pin pulled high on the power up) type (LVPECL/HCSL/LVDS/High-Z) of each output is programmable via SPI bus<br><br>In Hardware control mode (SEL pin pulled low on the power up) type (LVPECL/HCSL/LVDS/High-Z) of each output bank is controlled via OUTA/B_TYPE_SEL0/1 pins |
| 37 | OUT_LVCMOS | O | **Ultra Low Additive Jitter LVCMOS Output**<br><br>Output frequency range 0 to 250MHz |
| **Control** | | | |
| 32 | SEL | $I_{PD}$ | **Select control.**<br>When this pin is low, the device is controlled via hardware pins, IN_SEL0/1 and OE. When this pin is high, the device is controlled via SPI port.<br><br>Any change of SEL pin value requires power cycle. Hence, SEL pin cannot be changed on the fly. |

| 15 | IN_SEL0/SPI_CLK | I$_{PD}$ or I$_{PU}$ | **Input Select 0 or Clock for Serial Interface.** When SEL pin is low this pin is Input Select 0 hardware control input pin and it is pulled-down with 300 kΩ resistor. When SEL pin is high this pin provides clock for serial micro-port interface and it is pulled-up with 300 kΩ resistor. |
|---|---|---|---|

| IN_SEL1 | IN_SEL0 | OUTN |
|---|---|---|
| 0 | 0 | Input 0 (IN0) |
| 0 | 1 | Input 1 (IN1) |
| 1 | 0 | Crystal Oscillator or overdrive |
| 1 | 1 | Crystal Bypass |

| 18 | IN_SEL1/SPI_SDI | I$_{PD}$ or I$_{PU}$ | **Input Select 1 or Serial Interface Input.** When SEL pin is low this pin is Input Select 1 hardware control pin and it is pulled-down with 300 kΩ resistor. When SEL pin is high this pin is serial interface input stream and it is pulled-up with 300 kΩ resistor. The serial data stream holds the access command, the address and the write data bits. |
|---|---|---|---|
| 19 | IC1/SPI_SDO | I/O | **Internal Connection 1 or Serial Interface Output.**<br>When SEL pin is low this pin in an internal connection. Leave open.<br>When SEL pin is high this pin is Serial interface output stream. As an output the serial stream holds the read data bits. |
| 33 | IC2 | I$_{PD}$ | **Internal Connection 2**. This pin should be left open. |
| 39 | LVCMOS_OE/ SPI_CS_b | I$_{PD}$ or I$_{PU}$ | **LVCMOS Output Enable or Chip Select for Serial Interface.**<br>When SEL pin is low this pin is LVCMOS Output Enable hardware control input and it is pulled-down with 300 kΩ resistor.<br>When SEL pin is high this pin is serial interface chip select and it is pulled-up with 300 kΩ resistor--this is an active low signal. |
| 11 40 | OUT_TYPE_SEL0/ IC3 OUT_TYPE_SEL1/ IC4 | I$_{PD}$ | **Output Signal Type:**<br>When SEL pin is low these two pins Selects Type for all outputs |

| OUT_TYPE_SEL1 | OUT_TYPE_SEL0 | Output 0 to 4 |
|---|---|---|
| 0 | 0 | LVPECL |
| 0 | 1 | LVDS |
| 1 | 0 | HCSL |
| 1 | 1 | High-Z (Disabled) |

When SEL pin is high these two pins are unused and should be left unconnected.

| | | | |
|---|---|---|---|
| **Crystal Oscillator** | | | |
| 13 | XIN | I | **Crystal Oscillator Input or crystal bypass mode or crystal overdrive mode** |
| 14 | XOUT | O | **Crystal Oscillator Output** |
| **No Connect** | | | |
| 2<br>3 | NC1<br>NC2 | NC | **No Connect (not connected to the die)** Leave unconnected or connect to GND for mechanical support |
| **Power and Ground** | | | |
| 12<br>36 | VDD | P | **Positive Supply Voltage.** Connect to 3.3V or 2.5V supply. |
| 4<br>7 | VDDO_A | P | **Positive Supply Voltage for Differential Outputs Bank A** Connect 3.3V or 2.5V power supply. VDDO_A does not have to be connected to the same voltage level as VDD or VDDO_B.<br>These pins power up differential outputs OUT0_p/n and OUT1_p/n. |
| 24<br>27 | VDDO_B | P | **Positive Supply Voltage for Differential Outputs Bank B** Connect 3.3V or 2.5V power supply. VDDO_B does not have to be connected to the same voltage level as VDD or VDDO_A.<br>These pins power up differential outputs OUT2_p/n, OUT3_p/n and OUT4_p/n. |
| 38 | VDD_LVCMOS | P | **Positive Supply Voltage for LVCMOS Output** Connect 3.3V, 2.5V, 1.8V or 1.5V power supply |
| 1<br>10<br>20<br>21<br>30<br>31 | GND | P | **Ground** Connect to the ground |
| E-Pad | GND | P | **Ground.** Connect to the ground |

## Functional Description

The ZL40235 is a programmable or hardware pin controlled low additive jitter, low power 3 x 5 LVPECL/HCSL/LVDS fanout buffer.

Two inputs can accept signal in differential (LVPECL, SSTL, LVDS, HSTL, CML ) or single ended (LVPECL or LVCMOS) format and the third input can accept a single ended signal or it can be used to build a crystal oscillator by connecting an external crystal resonator between its XIN and XOUT pins. All the other components for building crystal oscillator are built in device such as load capacitance, series and shunt resistors.

The ZL40235 has five LVPECL/HCSL/LVDS outputs which can be powered from 3.3V or 2.5V supply. Each output can be independently enabled/disabled via SPI bus. The type of each output driver can be programmed to be LVPECL, HCSL or LVDS. Hence, the device can be configured to support application where different signal formats are needed.

The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

## Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40235 inputs.

Figure 3 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100$\Omega$ each and Ro + Rs should be 50$\Omega$ so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor $R_S$ should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Table 8). The source resistors of Rs = 270$\Omega$ could be used for standard LVCMOS driver. This will provide 516mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) *(1/(270$\Omega$ + 50$\Omega$)) = 5.16mA.

For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.
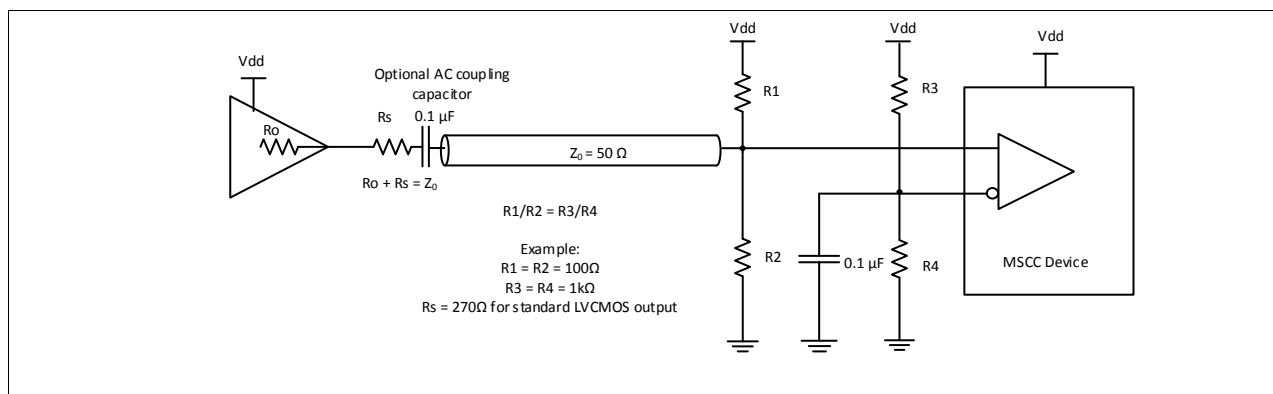


**Figure 3. Input driven by a single ended output**
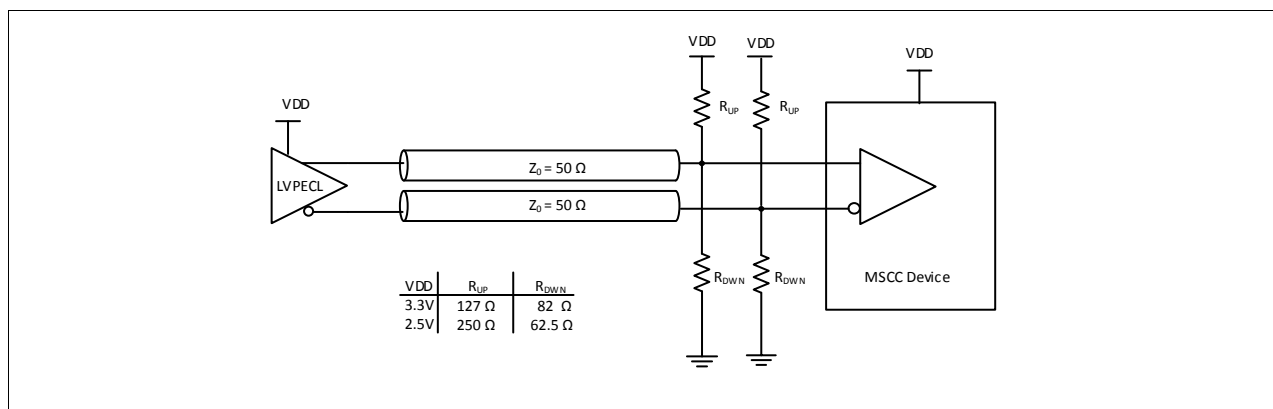


**Figure 4. Input driven by DC coupled LVPECL output**
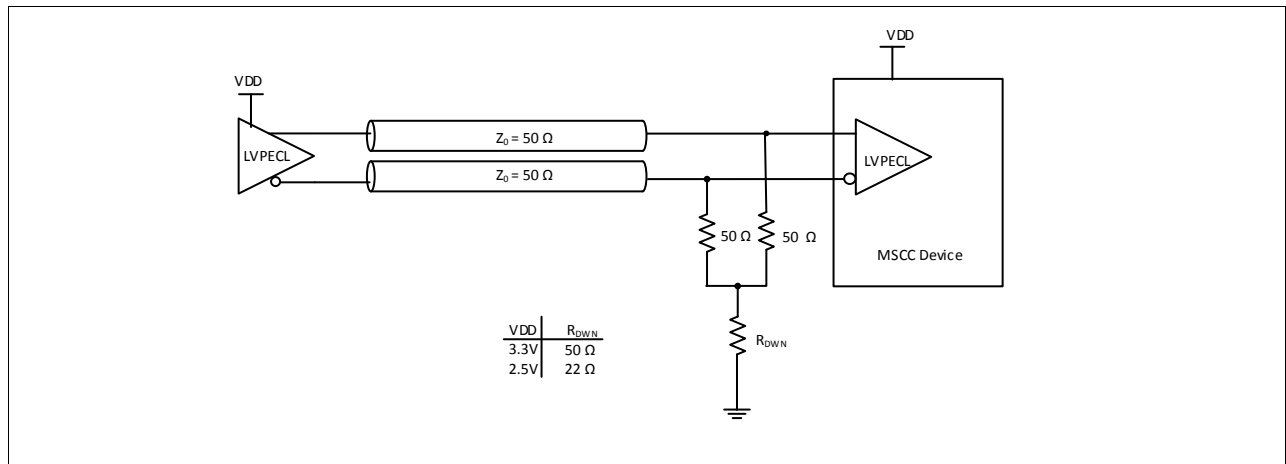
**Figure 5. Input driven by DC coupled LVPECL output (alternative termination)**
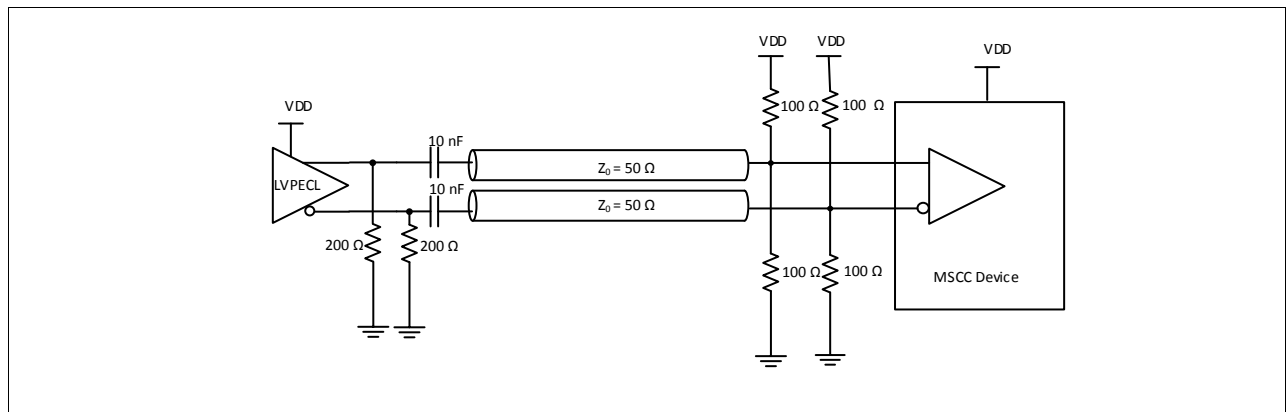


**Figure 6. Input driven by AC coupled LVPECL output**
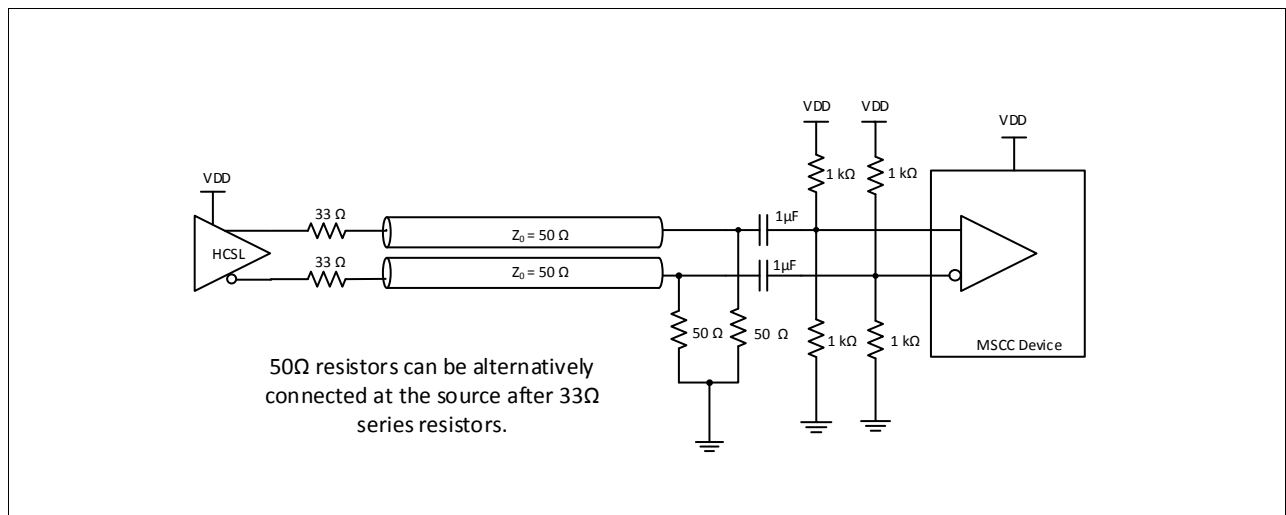


**Figure 7. Input driven by HCSL output**
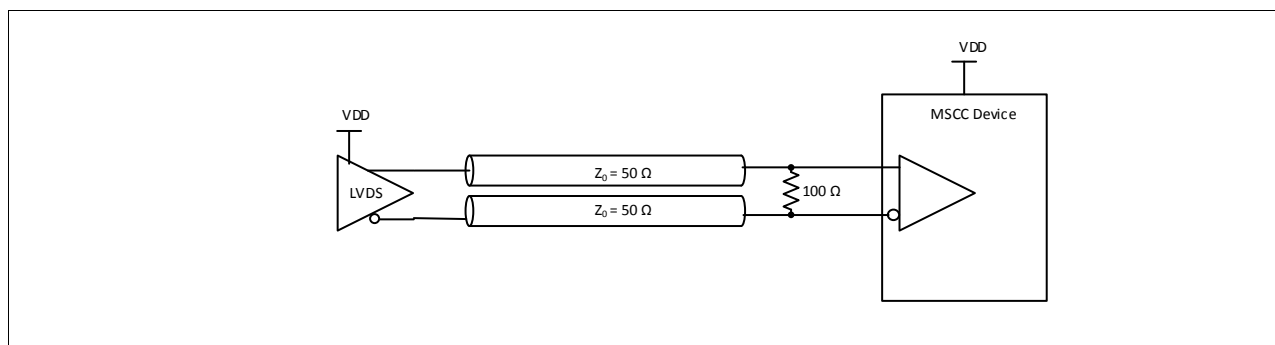
**Figure 8. Input driven by LVDS output**
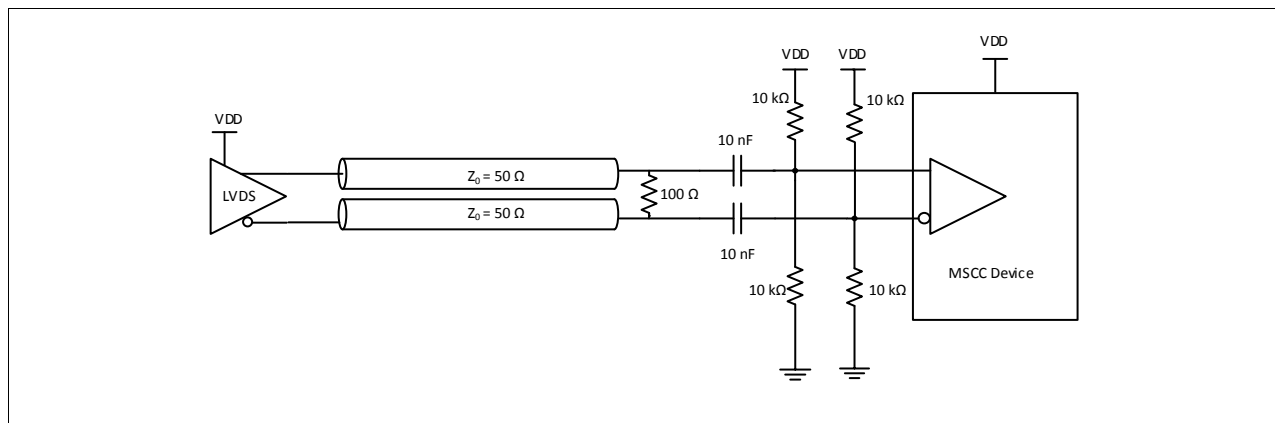


**Figure 9. Input driven by AC coupled LVDS**



Input driven by SSTL driver
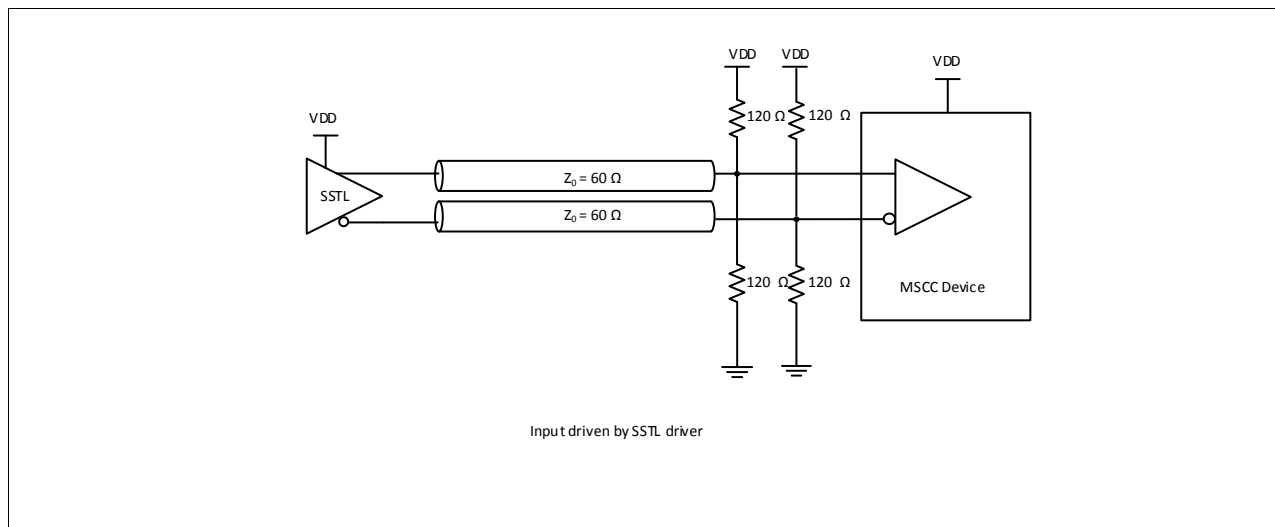
**Figure 10.    Input driven by an SSTL output**

## Clock Outputs

LVCMOS output OUT10 require only series termination resistor whose value is depending on LVCMOS output voltage as shown in Figure 11.



| VDDO | Rs |
|------|------|
| 3.3V | 35Ω |
| 2.5V | 30Ω |
| 1.8V | 20Ω |
| 1.5V | 10Ω |
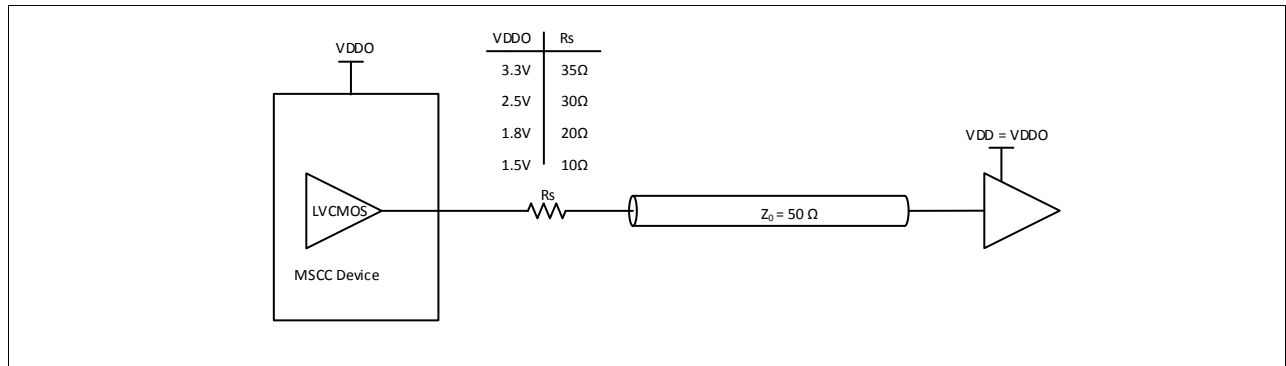
**Figure 11.      Termination for LVCMOS outputs**

Differential outputs LVPECL and LVDS should have same termination as corresponding outputs described in previous section. HCSL outputs should be terminated with 33Ω series resistors at the source and 50Ω shunt resistors at the source or at the end on the transmission line. AC coupling and re-biasing is not required at the outputs when driving native HCSL receivers.

The device is designed to drive differential input of semiconductor devices. In applications that use a transformer to convert from the differential to the single ended output (for example driving an oscilloscope 50Ω input), a resistor larger than 10Ω should be added at the center tap of the primary winding to achieve optimum jitter performance as shown in Figure 12. This is to provide a nominal common mode impedance of 10Ω or higher which is typical for differential terminations.
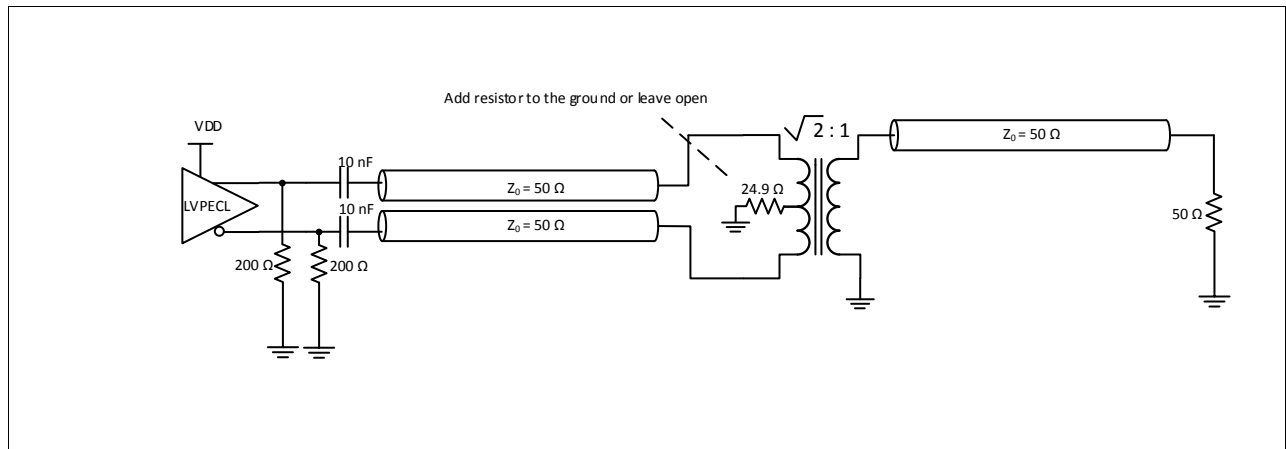


**Figure 12.      Driving a load via transformer**

## Crystal Oscillator Input

The crystal oscillator circuit can work with crystal resonators from 8MHz to 160MHz. As can be seen in the following figure only crystal resonator is required and all the other components are built-in the device. To be able support crystal resonators with different characteristics all internal components are programmable.
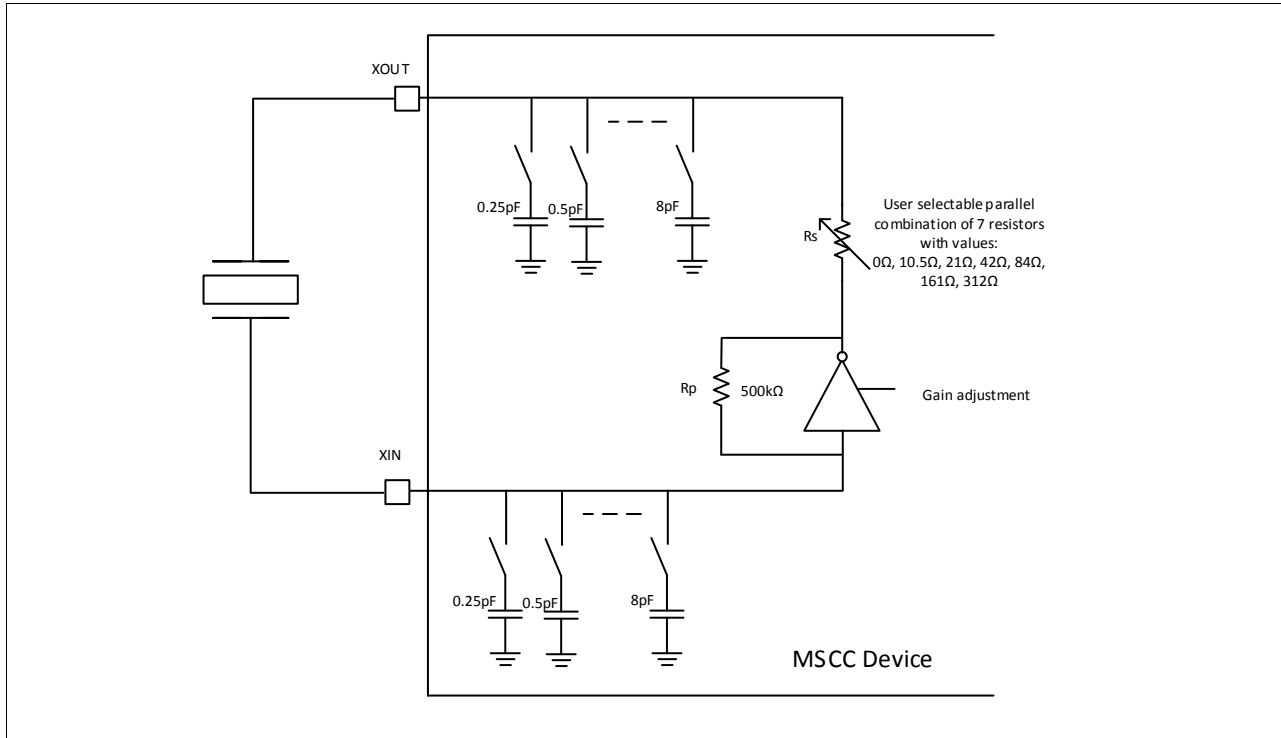


**Figure 13.     Crystal Oscillator Circuit**

The load capacitors can be programmed from 0 to 21.75 pF (4pF default) with resolution of 0.25pF which not only meets load requirement for most crystal resonator but also allows for fine tuning of the crystal resonator frequency. The amplifier gain can be adjusted in five steps and series resistor can be adjusted as parallel combination of seven different resistors: $0\Omega$, $10.5\Omega$, $21\Omega$, $42\Omega$, $84\Omega$, $161\Omega$ and $312\Omega$ ($84\Omega$ default). Although the first resistor is $0\Omega$ the series resistance Rs will be slightly higher than $0\Omega$ due to parasitic resistance of the switch which connects resistor. Hence the minimum series resistance is achieved when all seven resistors are connected in parallel. The shunt resistor is fixed and its value is $500k\Omega$.

In Hardware Controlled mode the capacitive load is set at 4pF, internal series resistance to $84\Omega$ and they cannot be changed. For Crystal requiring higher load or series resistance additional capacitance and/or series resistance can be added externally as shown in the Figure 14.
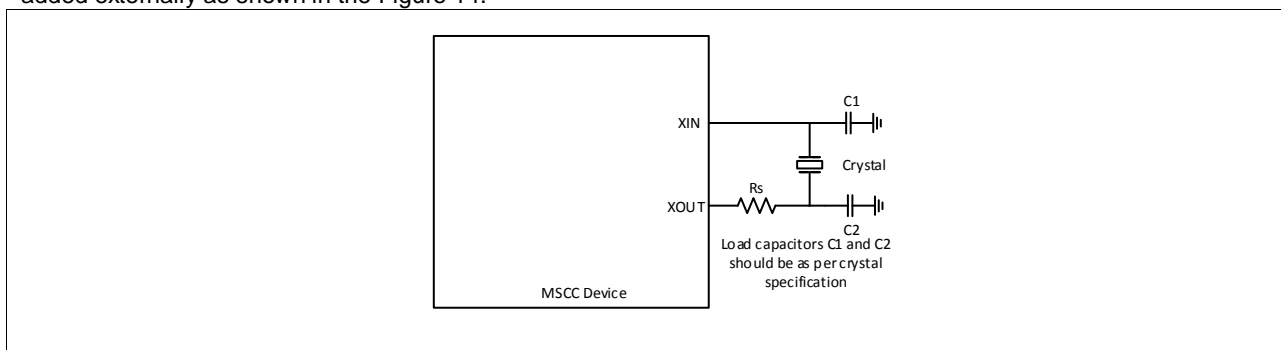


**Figure 14.     Crystal Oscillator Circuit in Hardware Controlled Mode**

## Termination of unused inputs and outputs

Unused inputs can be left unconnected or alternatively IN_0/1 can be pulled-down by $1k\Omega$ resistor. Unused outputs should be left unconnected.

## Power Consumption

The device total power consumption can be calculated as:

$$P_T = P_S + P_{XTAL} + P_C + P_{O\_DIF} + P_{O\_LVCMOS}$$

Where:

$$P_S = V_{DD} \times I_S$$

The core power when XTAL is not used. The current is specified in Table 7. .If XTAL is running this power should be set to zero.

$$P_{XTAL} = V_{DD} \times I_{DD\_XTAL}$$

The core power when XTAL is used. The current is provided in Table 7. If XTAL is not used this power should be set to zero.

$$P_C = V_{DDO} \times I_{DD\_CM}$$

Common output power shared among all ten outputs. The current $I_{DD\_CM}$ is specified in Table 7.

$$P_{O\_DIF} = V_{DDO} \times (I_{DD\_LVDS} \times N_1 + I_{DD\_LVPECL} \times N_2 + I_{DD\_HCSL} \times N_3)$$

Output power where output currents are specified in Table 7.
$N_1$, $N_2$ and $N_3$ are number of enabled LVPECL, LVDS and HSCL outputs respectively and $N_1+N_2+N_3$ is less or equal to 5.

$$P_{O\_LVCMOS} = V_{DD\_LVCMOS} \times (I_{DD} \times f / 100MHz + V_{DD\_LVCMOS} \times C_{LOAD} \times f)$$

Dynamic LVCMOS output power. $I_{DD}$ is specified in Table 7. If LVCMOS output is disabled this term is equal to zero.

Power dissipated inside the device can be calculated by subtracting power dissipated in termination/biasing resistors from the power consumption.

$$P_D = P_T - N_1 \times P_{LVPECL} - N_2 \times P_{LVDS} - N_3 \times P_{HCSL}$$

Where $N_1$, $N_2$ and $N_3$ are number of enabled LVPECL, LVDS and HSCL outputs respectively. Since there are five differential outputs $N_1 + N_2 + N_3$ is less or equal to 5.

$$P_{LVPECL} = (V_{OH} - V_B)^2 / 50\Omega + (V_{OL} - V_B)^2 / 50\Omega + (V_{OH} - V_B) \times V_B / 50\Omega + (V_{OL} - V_B) \times V_B / 50\Omega$$

$V_{OH}$ and $V_{OL}$ are the output high and low voltages respectively for LVPECL output
$V_B$ is LVPECL bias voltage equal to $V_{DD} - 2V$

$$P_{LVDS} = V_{SW}^2 / 100\Omega$$

$V_{SW}$ is voltage swing of LVDS output.

$$P_{HCSL} = (V_{SW} / 50\Omega)^2 \times (33\Omega + 50\Omega)$$

$V_{SW}$ is voltage swing of HCSL output. 50Ω is termination resistance and 33Ω is series resistance of the HCSL output.

## Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with 0.1µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce

the power noise from adjacent digital components on the board each power supply could be further insulated with low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Following figure shows recommended decoupling for each power pin.
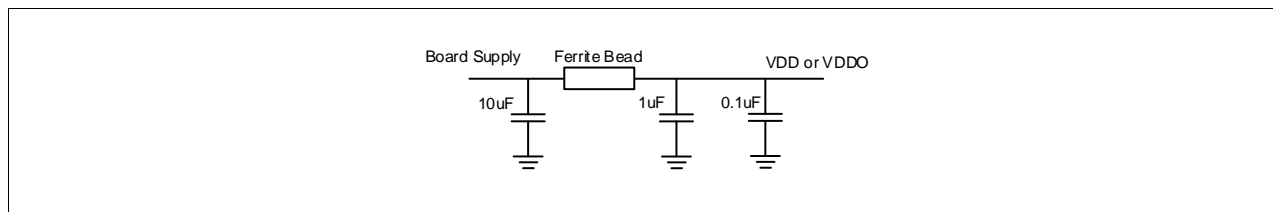


**Figure 15. Power Supply Filtering**

## Power Supplies and Power-up Sequence

The device has four different power supplies: VDD, VDDO_A, VDDO_B and VDD_LVCMOS which are mutually independent. Voltages supported by each of these power supplies are specified in Table 1.

The device is not sensitive to the power-up sequence. For example commonly used sequence where higher voltage comes up before or at the same time as the lower voltages can be used (or any other sequence)

## Host Interface

ZL30235 can be controlled via hardware pins (SEL pin tied low) or via SPI port (SEL pin tied high). The mode shall be selected during power up and it cannot be changed on the fly.

### Hardware Control Mode

In this mode, ZL40235 is controlled via Input Select (IN_SEL0/1) pins which select which one of three inputs is fed to the output and show in Table 2 and OUT_TYPE_SEL0/1 pins which select signal level (LVPECL, LVDS, HCSL or Hi-Z) as shown in Table 3.

All input control pins have low input threshold voltage so they can be driven from the device with low output voltage (FPGA/CPLD). Supported voltages are between 1.2V and VDD (2.5V or 3.3V).

**Table 2 Input clock selection**

| IN_SEL1 | IN_SEL0 | Selected Input |
|---------|---------|----------------|
| 0 | 0 | IN0_p, IN0_n |
| 0 | 1 | IN1_p, IN1_n |
| 1 | X | XIN |

**Table 3 Output Type Selection**

| OUT_TYPE_SEL1 | OUT_TYPE_SEL0 | Output |
|---------------|---------------|--------|
| 0 | 0 | LVPECL |
| 1 | 1 | LVDS |
| 1 | 0 | HCSL |
| 1 | 1 | High-Z (Output Disabled) |

Output is disabled synchronously on the falling edge of the input ($t_2$) as shown in Figure 16.
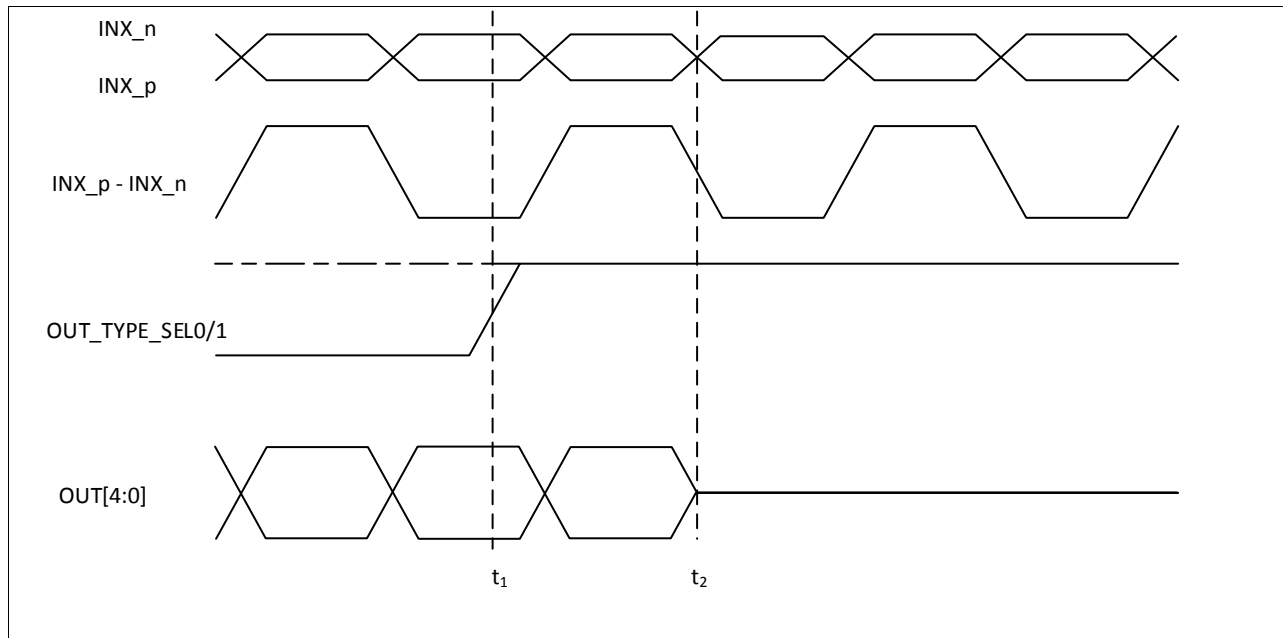


**Figure 16.    Output Disable**

Outputs can be enabled by toggling one or both OUT_TYPE_SEL0/1 pins low depending on which type of interface needs to be enabled. As soon as one or both OUT_TYPE_SEL0/1 pins go low ($t_1$) the outputs will go from high-Z to low (OUTX_p = low, OUTx_n = high) and will start to track the input after the first falling edge ($t_2$) of the input signal as shown in Figure 17.
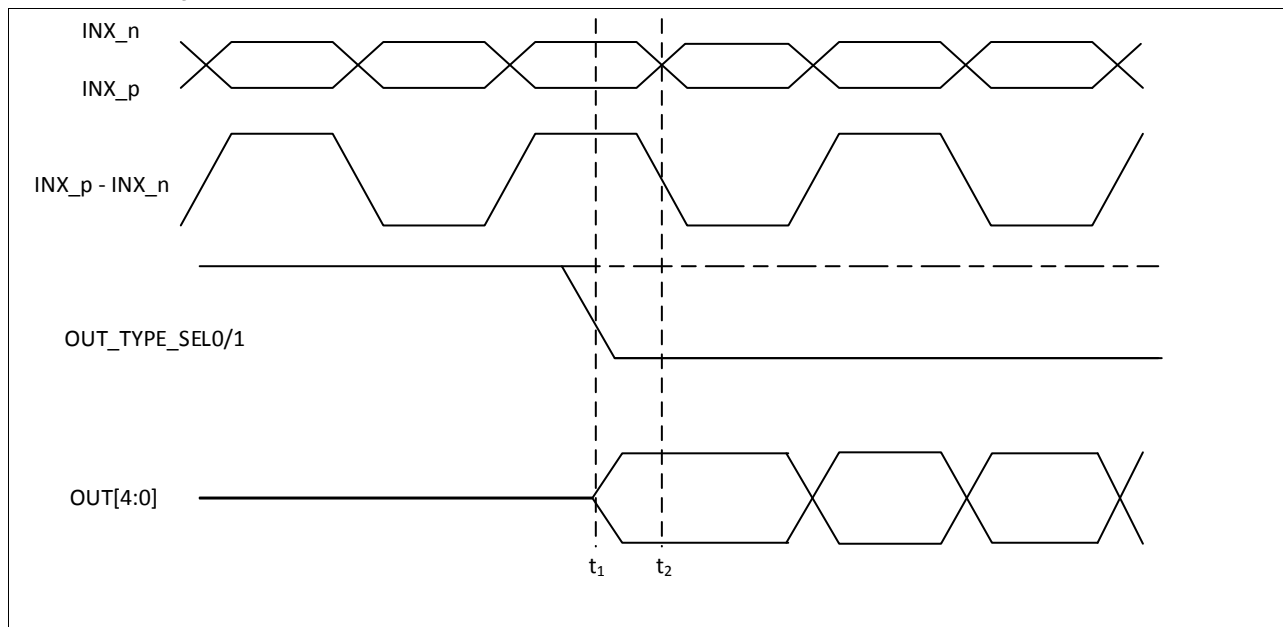


**Figure 17.    Output Enable**

**SPI Control Mode**

ZL40235 is controlled via four pin SPI slave interface as shown in the following figure.
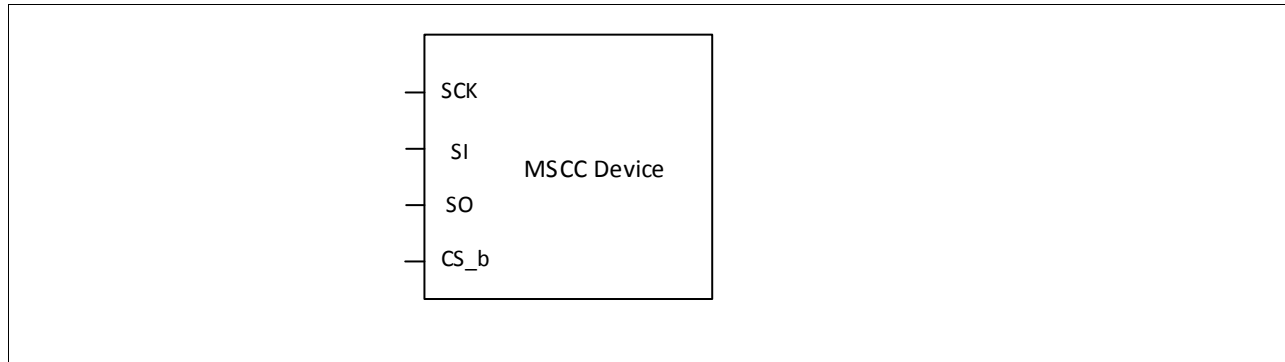


**Figure 18.      SPI slave interface**

All SPI input pins have low threshold voltage so they can be driven from low output voltage SPI master device. Supported voltages are between 1.2V and VDD (2.5V or 3.3V). This allows device to be controlled from an FPGA with low voltage I/O supply.

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the device, output data from the **SO** pin must be ignored. Similarly, the input data on the **SI** pin is ignored by the device during a read cycle.

The SPI interface supports two modes of access: Most Significant bit (MSb) first transmission or Least Significant bit (LSb) first transmission. The mode is automatically selected based on the state of **SCK** pin when the **CS_b** pin is active. If the **SCK** pin is low during **CS_b** activation, then MSb first timing is selected. If the **SCK** pin is high during **CS_b** activation, then LSb first timing is assumed.

The SPI port expects 1-bit to differentiate between read and write operation followed by 7-bit addressing and 8-bit data transmission. During SPI access, the **CS_b** pin must be held low until the operation is complete. Burst read/write mode is also supported by leaving the chip select signal **CS_b** is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

Functional waveforms for the LSb and MSb first mode, and burst mode are shown in Figure 19 and Figure 20 respectively. Figure 21 shows an example of burst mode operation which allows user to read or write consecutive location in the register map.
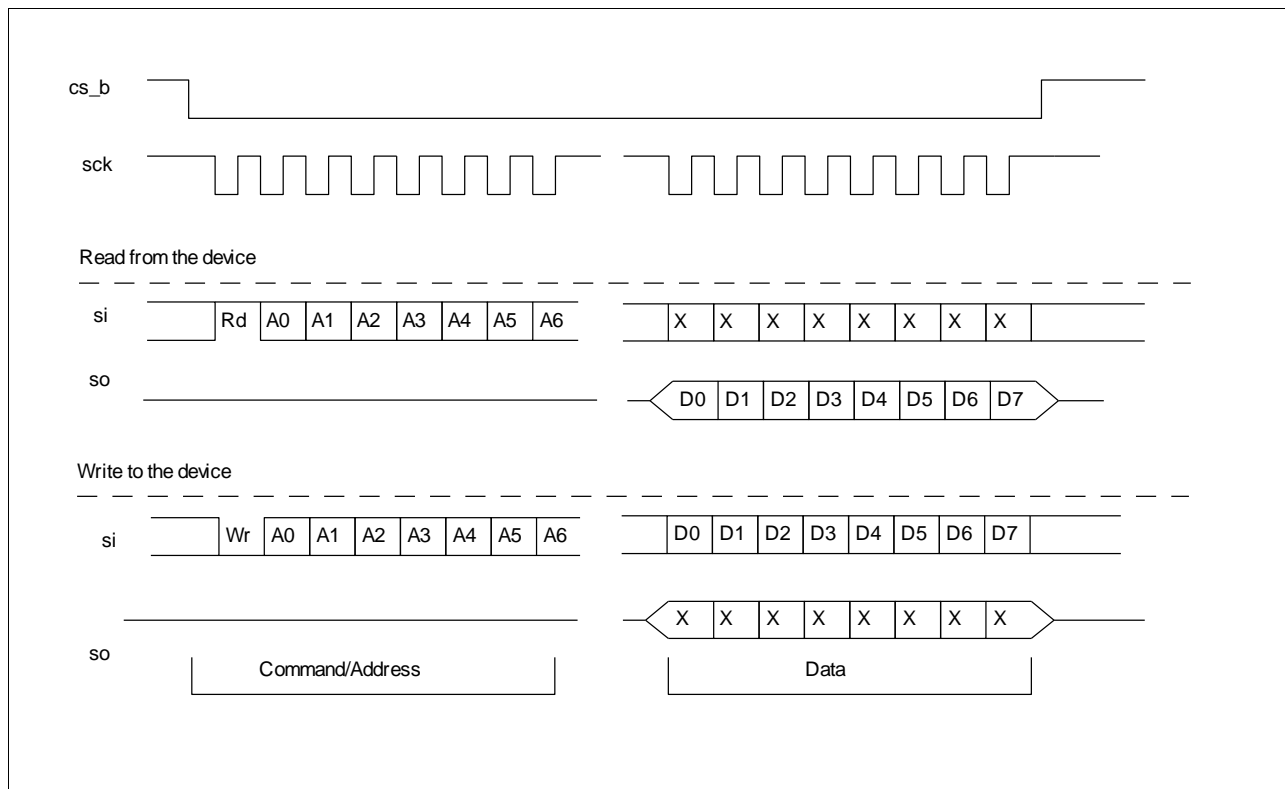
**Figure 19.      Serial Peripheral Interface Functional Waveform – LSB First Mode**
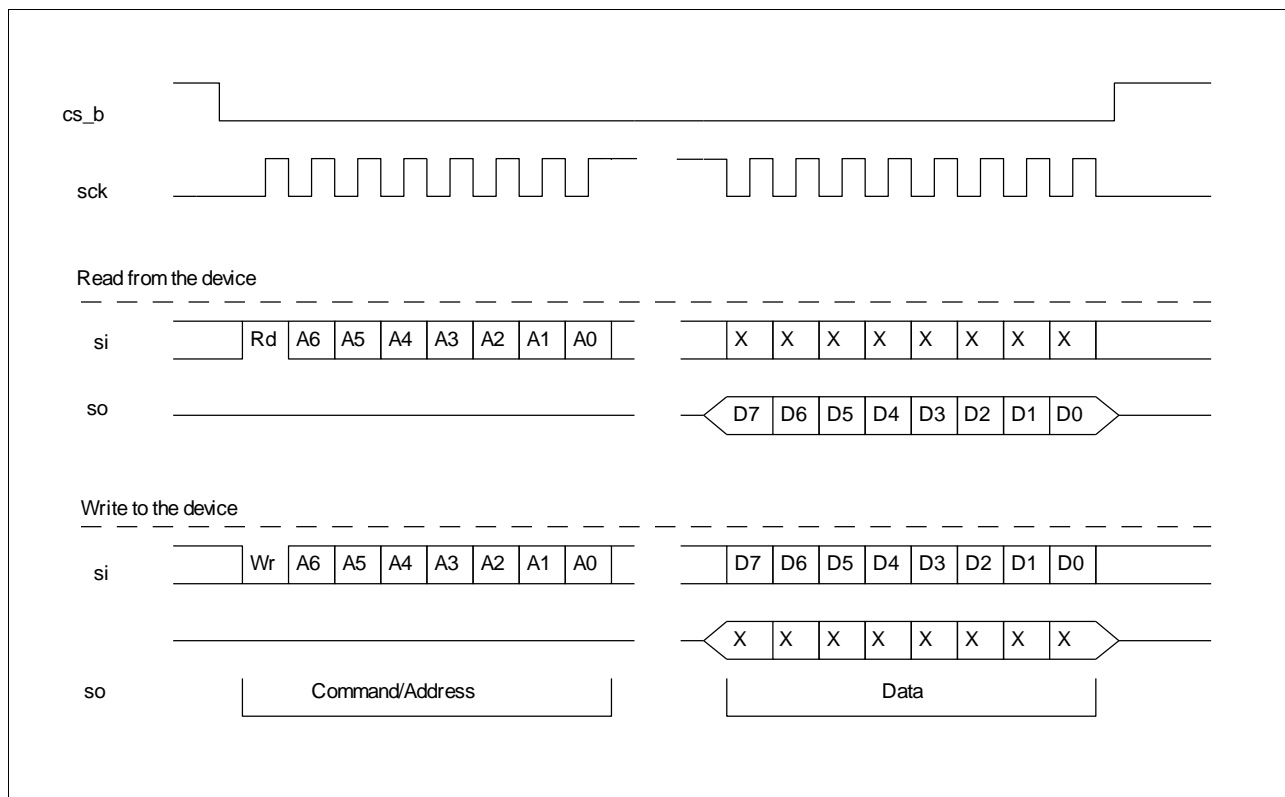


**Figure 20.      Serial Peripheral Interface Functional Waveform – MSB First Mode**
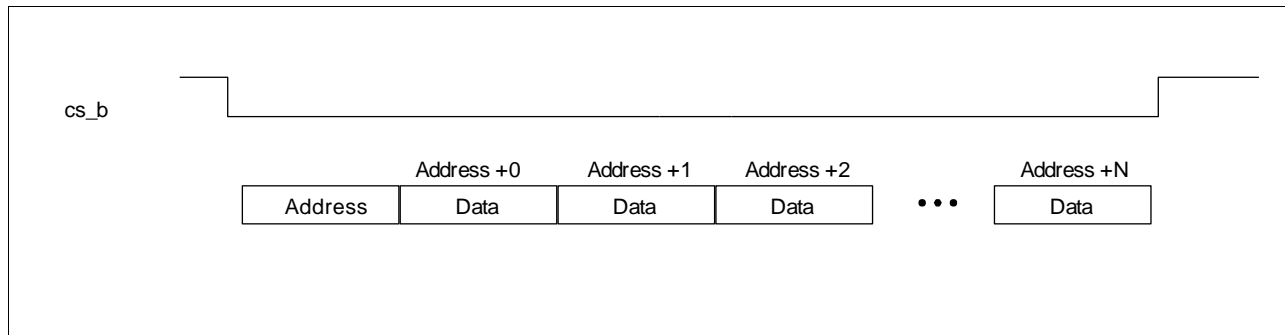
**Figure 21.    Example of the Burst Mode Operation**

## Typical device performance

The following plots show typical device performances
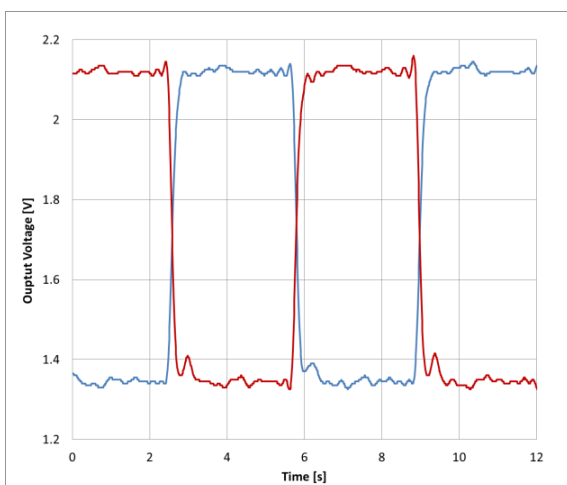


**Figure 22.      156.25MHz LVPECL**
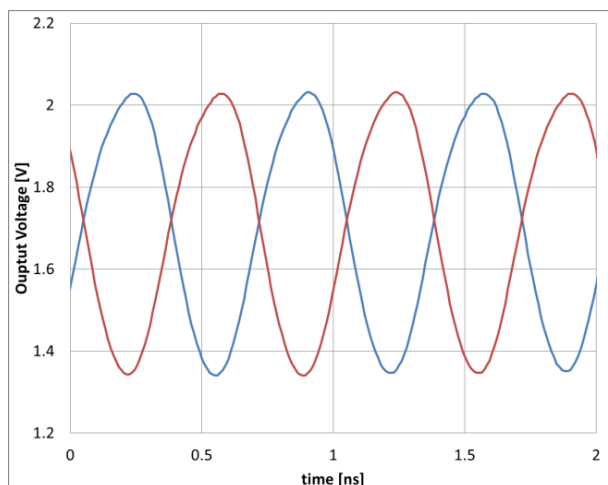


**Figure 23.      1.5GHz LVPECL**
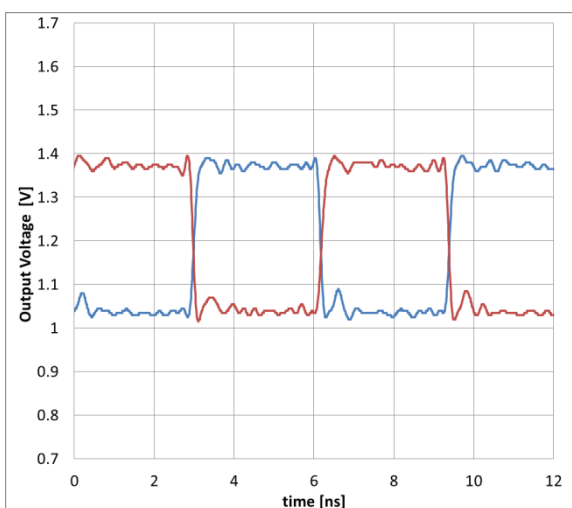


**Figure 24.      156.25MHz LVDS**
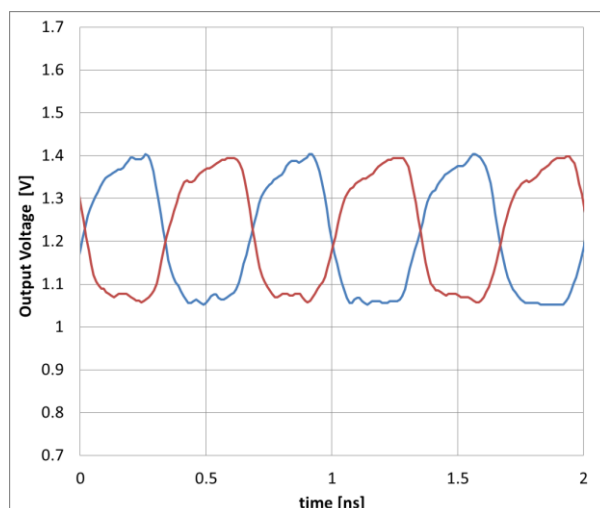


**Figure 25.      1.5GHz LVDS**
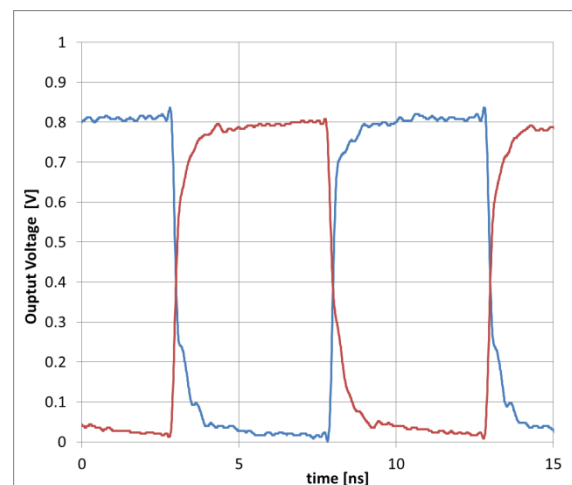


**Figure 26.      100MHz HCSL**



**Figure 27.      250MHz HCSL**

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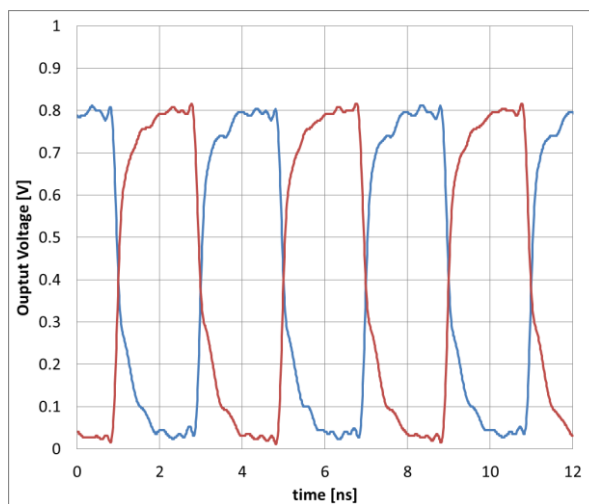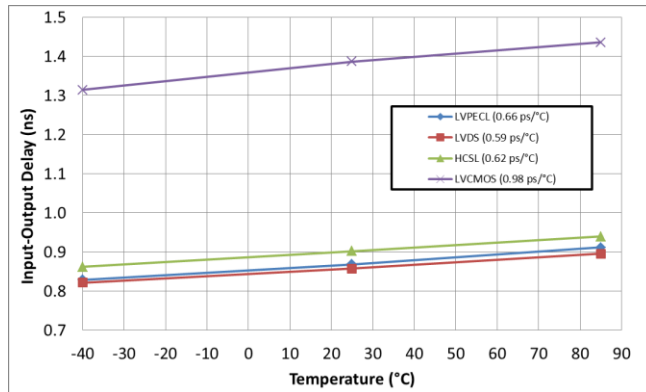
Figure 28.    I/O delay vs temperature
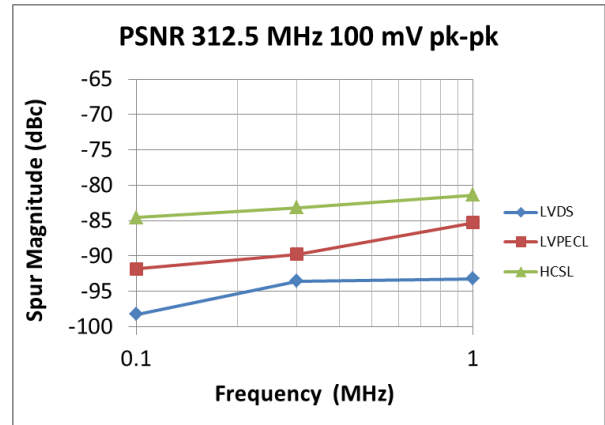


Figure 29.    PSNR vs noise frequency
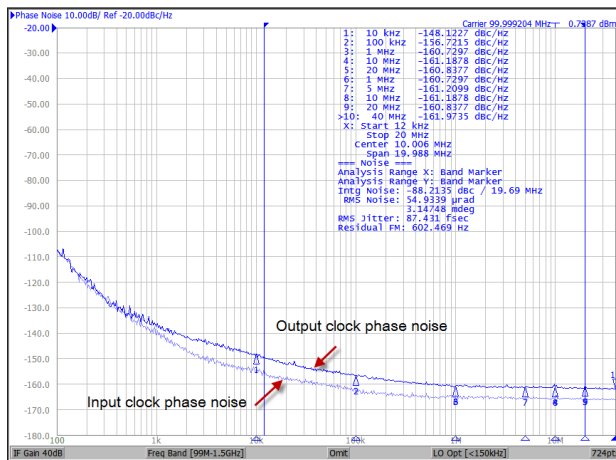


Figure 30.    100MHz LVPECL Phase Noise
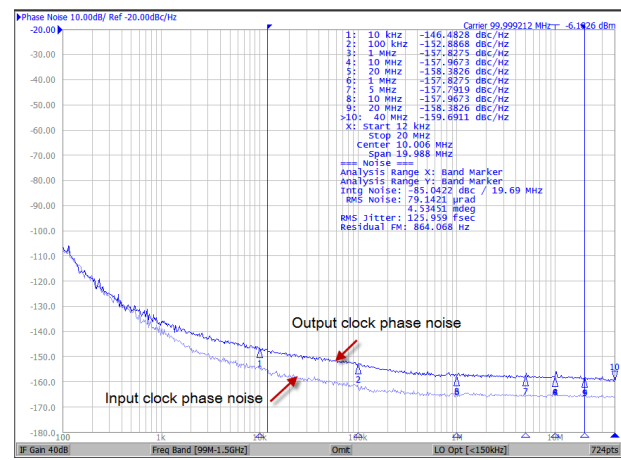


Figure 31.    100MHz LVDS Phase Noise
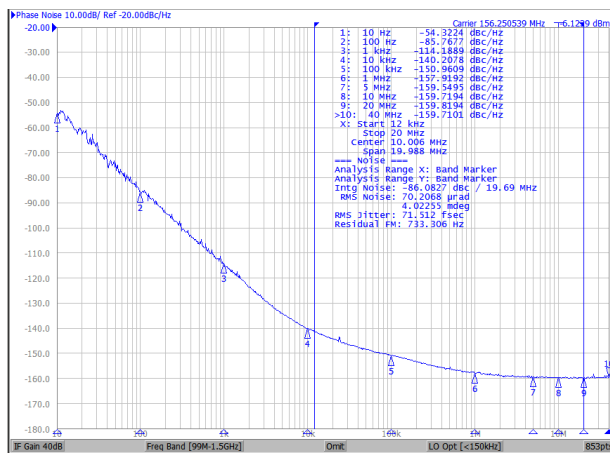


Figure 32.    156.25MHz LVDS Phase Noise in Xtal mode
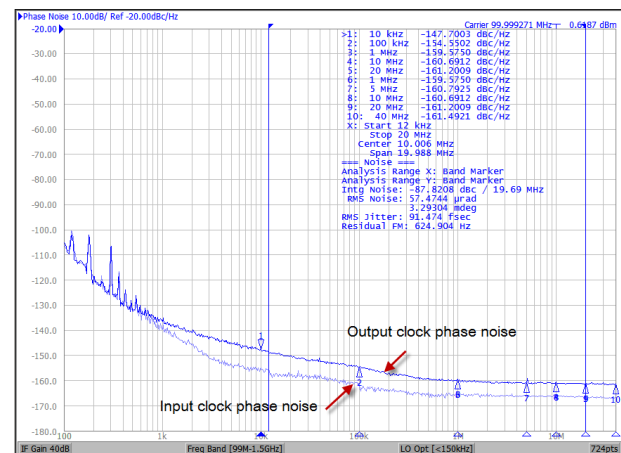


Figure 33.    100MHz HCSL Phase Noise
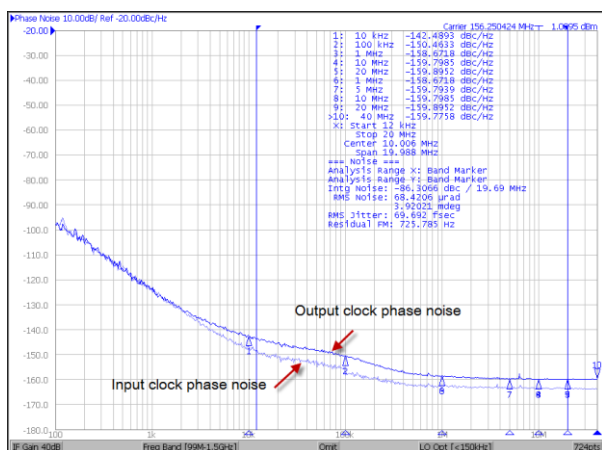
Figure 34.    156.25MHz LVPECL Phase Noise
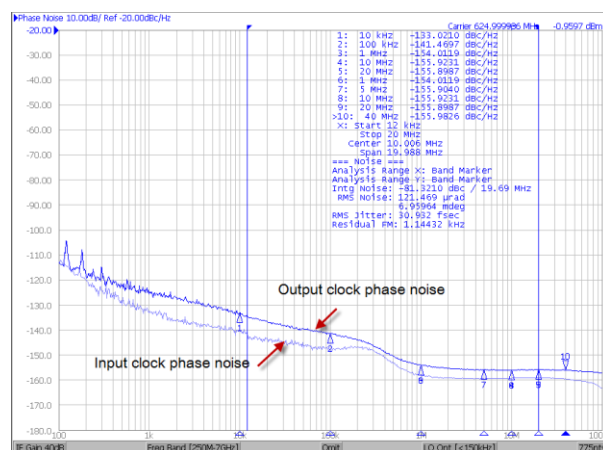


Figure 35.    625MHz LVPECL Phase Noise
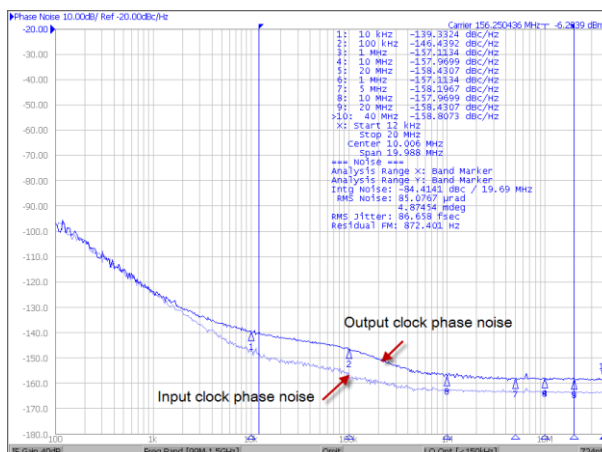


Figure 36.    156.25MHz LVDS Phase Noise
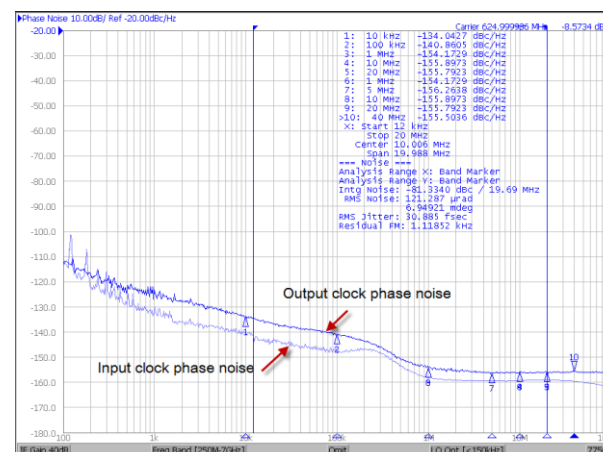


Figure 37.    625MHz LVDS Phase Noise
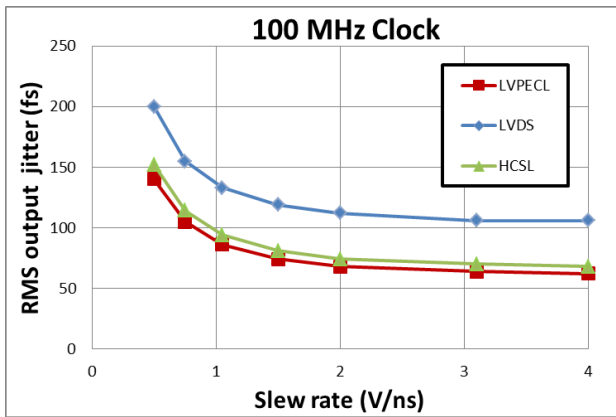
**Figure 38.     Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate**
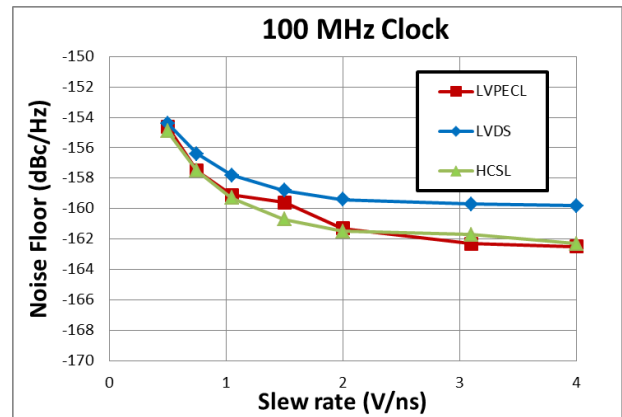


**Figure 39.     Output clock noise floor vs input clock slew-rate**
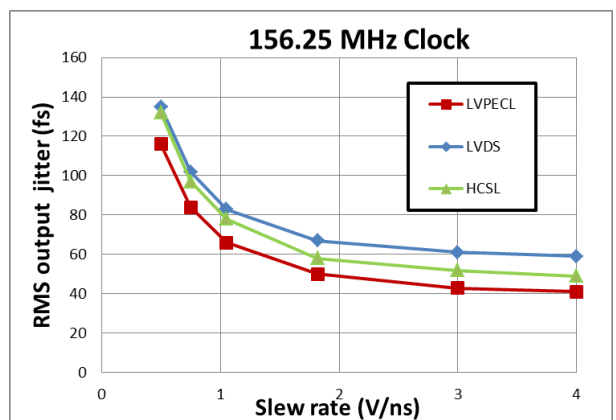


**Figure 40.     Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate**
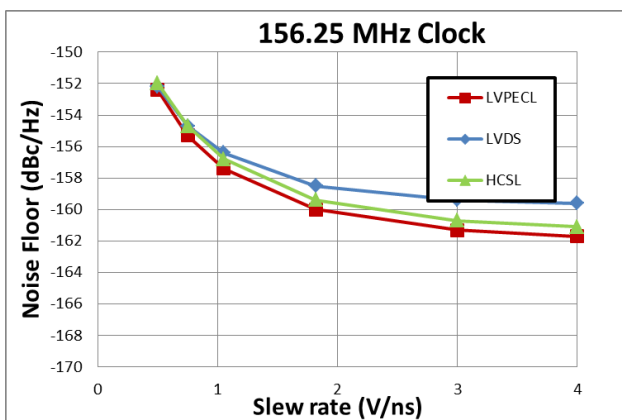


**Figure 41.     Output clock noise floor vs input clock slew-rate**
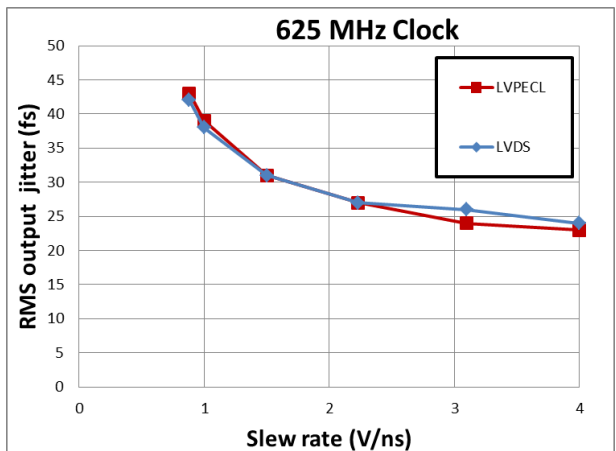


**Figure 42.     Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate**
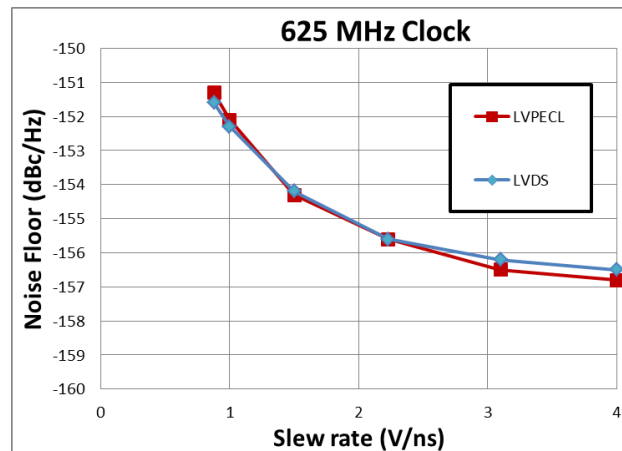


**Figure 43.     Output clock noise floor vs input clock slew-rate**

## Register Map

The device is controlled by accessing registers through the serial interface. The following table provides a summary of the registers available for the configuration of the device.

**Table 4 Register Map**

| Address SPI A[6:0] Hex (0x) | Name | Data D[7:0] |
|---|---|---|
| 00 | XTALBG | xtal_buf_gain[7:0] |
| 01 | XTALDL | xtal_drive_level[7:0] |
| 02 | XTALLC | xtal_load_cap[7:0] |
| 03 | XTALNR | xtal_normal_run |
| 04 | - | Not used |
| 05 | INSEL | input_select[1:0] |
| 06 | OUTLOW | output_drive_low |
| 07 | DRVTYPEA | {driver_type[5:4], 4'bxxxx} (differential output 1 and 0) |
| 08 | - | Not used |
| 09 | DRVTYPEB | {driver_type[17:12], 2'bxx} (differential output 4, 3, and 2) |
| 0A | - | Not used |
| 0B | CMOSDIV | cmos_div[2:0] (cmos) |
| 0C | CMOSOUTEN | output_enable (cmos) |
| 0D | CMOSDRVSTR | driver_strength (cmos) |
| 0E | - | Not used |
| 0F/11 | Reserved | Leave as default |
| 11 | DEVID | Device ID |
| 12 to 1F | Reserved | Leave as default |

| Address | 0x00 | | | | Hex |
|---------|------|---|---|---|-----|
| **XTALBG** | | **XTAL Buffer Gain** | | | |
| **Bit** | **Name** | **Description** | | **Type** | **Reset** |
| 7:0 | xtal_buf_gain[7:0] | Programs crystal buffer (inverting amplifier) gain.<br>Every bit pair (bits: 01, 23, 45, 67) of this register correspond to additional equal gain block which can be added (bits set) or removed (bits cleared).<br>Minimum gain is 0x00 (default) and 0xFF is maximum gain<br>When reference input mode is "bypass XTAL mode" or "differential input modes" with HIGH xtal_normal_run bit, the buffer is disabled and follows "Input Selection".<br>When xtal_normal_run bit is LOW, XTAL buffer is in the "xtal forced run" mode and keep running.<br><br>**8'b0000_0000: default crystal buffer strength.**<br>8'b0000_0011: enable additional buffer strength<br>8'b0000_1100: enable additional buffer strength<br>8'b0011_0000: enable additional buffer strength<br>8'b1100_0000: enable additional buffer strength | | RW | FF |

| Address | 0x01 | | | | Hex |
|---------|------|---|---|---|-----|
| **XTALDL** | | **XTAL Drive Level** | | | |
| **Bit** | **Name** | **Description** | | **Type** | **Reset** |
| 7:0 | xtal_drive_level[7:0] | Internal damping resistance of crystal circuit to limit external crystal's drive level uW.<br>The value of damping resistor is determined by crystal's motion resistance of crystal's equivalent circuit.<br>Drive level should be lower than crystal manufacturer's specification.<br>Crystal's equivalent values should be requested to the manufacturer, (motion resistance and shunt capacitance).<br>The selected resistors are connected to XOUT.<br>Multiple bit combinations available by 7-bit control.<br>Because they use parallel connections, 0xFF is the smallest resistance and 0x01 is the highest resistance.<br><br>8'b0000_0000: disable all resistors<br>8'b0000_0001: 312 Ohm resistor<br>8'b0000_0010: 161 Ohm resistor<br>8'b0000_0100: 84 Ohm resistor<br>8'b0000_1000: 42 Ohm resistor<br>8'b0001_0000: 21 Ohm resistor<br>8'b0010_0000: 10.5 Ohm resistor<br>8'b0100_0000: 0 Ohm connection<br>8'b1000_0000: not used | | RW | 04 |

| Address | 0x02 | | | Hex |
|---------|------|---|---|-----|
| **XTALLC** | | **XTAL Load Capacitance 0** | | |
| **Bit** | **Name** | **Description** | **Type** | **Reset** |
| 7:0 | xtal_load_cap[7:0] | Internal load capacitance of crystal circuit (0 pF to 21.75 pF with the resolution of 0.25 pF). XIN and XOUT have each capacitor connected to GND. Multiple bit combinations available between 8 capacitors. <br><br> 8'b0000_0000: disable all xtal load capacitors <br> 8'b0000_0001: enable capacitor 0.25 pF <br> 8'b0000_0010: enable capacitor 0.5 pF <br> 8'b0000_0100: enable capacitor 1 pF <br> 8'b0000_1000: enable capacitor 2 pF <br> 8'b0001_0000: enable capacitor 2 pF <br> 8'b0010_0000: enable capacitor 4 pF <br> 8'b0100_0000: enable capacitor 4 pF <br> 8'b1000_0000: enable capacitor 8 pF | RW | 40 |

| Address | 0x03 | | | Bin |
|---------|------|---|---|-----|
| **XTALNR** | | **XTAL Normal Run** | | |
| **Bit** | **Name** | **Description** | **Type** | **Reset** |
| 7:1 | Reserved | Reserved | R | 1111111 |
| 0 | xtal_normal_run | When this bit is set high crystal oscillator circuit is running only if input_select[1:0] register at address 0x05 selects crystal mode (2'b10). This value is recommended because it provides best jitter performance--XO circuit is running only when it is needed. <br><br> When this bit is set low the crystal oscillator will keep running even if crystal oscillator is not selected in input_select[1:0] register at address 0x05. This mode should only be used when fast switching between input references and crystal oscillator is required. | RW | 1 |

| Address | 0x05 | | | Bin |
|---|---|---|---|---|
| INSEL | | Input Select Register | | |
| Bit | Name | Description | Type | Reset |
| 7:2 | Reserved | Reserved | R | 111111 |
| 1:0 | input_select[1:0] | Input reference clock selection. Proper external coupling and termination are required. 2'b00: differential input from IN0_p and IN0_n 2'b01: differential input from IN1_p and IN1_n 2'b10: fundamental XTAL mode with XIN and XOUT (Use internal crystal oscillator circuits) or XTAL overdrive mode (single-ended clock signal fed to XIN) 2'b11: XTAL bypass mode (single-ended clock signal with XIN and disabled internal crystal buffer circuit in the analog block) | RW | 00 |

| Address | 0x06 | | | Hex |
|---|---|---|---|---|
| OUTLOW | | Output Drive Low | | |
| Bit | Name | Description | Type | Reset |
| 7:1 | Reserved | Reserved | R | 1111111 |
| 0 | output_drive_low | Forces all disabled outputs to drive low in LVPECL mode. 1'b1: All differential outputs that are disabled in DRVTYPE registers (addresses 0x07, 0x08, 0x09 and 0x0A) will drive low in LVPECL mode. Hence, LVPECL biasing/termination resistors are required for proper functionality of this feature. 1'b0: This feature is ignored and all outputs that are disabled in DRVTYPE registers (addresses 0x07, 0x08, 0x09 and 0x0A) will stay in disabled (high-Z) mode. | RW | 0 |

| Address | 0x07 | | | Bin |
|---|---|---|---|---|
| DRVTYPEA | | Output Type Select Bank-A | | |
| Bit | Name | Description | Type | Reset |
| 7:6 | driver_type[7:6] | Output driver type of differential OUT1. The same description as for OUT0. | RW | 11 |
| 4:3 | driver_type[5:4] | Output driver type of differential OUT0. 2'b00: LVPECL outputs 2'b01: LVDS outputs 2'b10: HCSL outputs 2'b11: outputs disabled (Disabled state is dependent on "out_drive_low" control bit of register OUTLOW.") | RW | 11 |
| 3:0 | Reserved | Reserved | RO | X |

| Address | 0x09 | | | Bin |
|---------|------|---|------|-------|
| DRVTYPEB | | Output Type Select Bank-B | | |
| Bit | Name | Description | Type | Reset |
| 7:6 | driver_type[17:16] | Output driver type of differential OUT4.<br><br>The same description as for OUT0. | RW | 11 |
| 5:4 | driver_type[15:14] | Output driver type of differential OUT3.<br><br>The same description as for OUT0. | RW | 11 |
| 3:2 | driver_type[13:12] | Output driver type of differential OUT2.<br><br>The same description as for OUT0. | RW | 11 |
| 1:0 | Reserved | Reserved | RO | X |

| Address | 0x0B | | | Bin |
|---------|------|---|------|-------|
| CMOSDIV | | CMOS Output Divider | | |
| Bit | Name | Description | Type | Reset |
| 7:3 | Reserved | Reserved | R | 11111 |
| 2:0 | cmos_div[2:0] | Integer divider from a selected input reference clock for OUT_LVCMOS (1 to 8).<br><br>**3'b000: division ratio = 1**<br>3'b001: division ratio = 2<br>3'b010: division ratio = 3<br>3'b011: division ratio = 4<br>3'b100: division ratio = 5<br>3'b101: division ratio = 6<br>3'b110: division ratio = 7<br>3'b111: division ratio = 8 | RW | 000 |

| Address | 0x0C | | | Bin |
|---------|------|---|------|-------|
| CMOSOUTEN | | LVCMOS Output Enable | | |
| Bit | Name | Description | Type | Reset |
| 7:1 | Reserved | Reserved | R | 1111111 |
| 0 | output_enable | Output enable of OUT_LVCMOS.<br>Disabled state is dependent on "out_drive_low" control bit.<br><br>1'b0: Disable OUT_LVCMOS output<br>1'b1: Enable OUT_LVCMOS output | RW | 1 |

| Address | 0x0D | | | Bin |
|---------|------|---|------|-------|
| CMOSDRVSTR | | CMOS Driver Strength | | |
| Bit | Name | Description | Type | Reset |
| 7:1 | Reserved | Reserved | R | 1111111 |
| 0 | driver_strength | OUT_LVCMOS output strength.<br><br>1'b0: low strength<br>1'b1: high strength | RW | 0 |

| Address | 0x11 | | | Bin |
|---------|------|---------------|------|-------|
| DEVID | | **Device Identification** | | |
| **Bit** | **Name** | **Description** | **Type** | **Reset** |
| 7 | Unused | Unused | R | 0 |
| 6:5 | Reserved | Reserved | R | 11 |
| 4:0 | dev_id | Device ID<br><br>5'h02: ZL40235 | RO | 00010 |

# AC and DC Electrical Characteristics

## Absolute Maximum Ratings

### Table 5 Absolute Maximum Ratings*

| | Parameter | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Supply voltage (3.3V) | $V_{DD}$ /$V_{DDO}$ | -0.5 | | 4.6 | V | |
| 2 | Supply voltage (2.5V) | $V_{DD}$ /$V_{DDO}$ | -0.5 | | 3.5 | V | |
| 3 | Storage temperature | $T_{ST}$ | -55 | | 125 | °C | |

* Exceeding these values may cause permanent damage
* Functional operation under these conditions is not implied
* Voltages are with respect to ground (GND) unless otherwise stated

## Recommended Operating Conditions

### Table 6 Recommended Operating Conditions*

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Supply voltage 3.3V | $V_{DD}$ /$V_{DDO}$/$V_{DD\_LVCMOS}$ | 3.135 | 3.30 | 3.465 | V | |
| 2 | Supply voltage 2.5V | $V_{DD}$ /$V_{DDO}$/$V_{DD\_LVCMOS}$ | 2.375 | 2.50 | 2.625 | V | |
| 3 | Supply voltage 1.8V | $V_{DD\_LVCMOS}$ | 1.6 | 1.8V | 2 | V | |
| 4 | Supply voltage 1.5V | $V_{DD\_LVCMOS}$ | 1.35 | 1.5 | 1.65 | V | |
| 5 | Operating temperature | $T_A$ | -40 | 25 | 85 | °C | |
| 6 | Input voltage | $V_{DD-IN}$ | - 0.3 | | $V_{DD}$ + 0.3 | V | |

* Voltages are with respect to ground (GND) unless otherwise stated
* The device core supports two power supply modes (3.3V and  2.5V)

### Table 7 Current consumption

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Core device current (all outputs and XTAL disabled) | $I_{s\_3.3V}$ | | 163 | 197 | mA | VDD= 3.3V+5% |
| | | $I_{s\_2.5V}$ | | 153 | 187 | mA | VDD = 2.5V+5% |
| 2 | Core device current (all outputs disabled) XTAL circuit enabled with 25MHz Crystal connected between XIN and XOUT | $I_{DD\_XTAL\_3.3V}$ | | 128 | 154 | mA | VDD= 3.3V+5% |
| | | $I_{DD\_XTAL\_2.5V}$ | | 124 | 150 | mA | VDD= 2.5V+5% |
| 3 | Common output current | $I_{DD\_CM\_3.3V}$ | | 13.44 | 15.05 | mA | VDDO= 3.3V+5% |
| | | $I_{DD\_CM\_2.5V}$ | | 12.18 | 13.65 | mA | VDDO= 2.5V+5% |
| 4 | Dynamic LVCMOS current for high strength output (f = 100MHz) Needs to be scaled for different frequencies by f/100MHz | $I_{DD\_3.3V}$ | | 4.08 | 4.74 | mA | VDDO= 3.3V+5% |
| | | $I_{DD\_2.5V}$ | | 2.90 | 3.29 | mA | VDDO= 2.5V+5% |
| 5 | Dynamic LVCMOS current for low strength output (f = 100MHz) Needs to be scaled for different frequencies by f/100MHz | $I_{DD\_3.3V}$ | | 2.38 | 2.68 | mA | VDDO= 3.3V+5% |
| | | $I_{DD\_2.5V}$ | | 1.74 | 1.96 | mA | VDDO= 2.5V+5% |
| 6 | Current dissipation per LVPECL output | $I_{DD\_LVPECL\_3.3V}$ | | 19.36 | 23.26 | mA | VDDO= 3.3V+5% |
| | | $I_{DD\_LVPECL\_2.5V}$ | | 19.38 | 22.17 | mA | VDDO= 2.5V+5% |
| 7 | Current dissipation per LVDS output | $I_{DD\_LVDS\_3.3V}$ | | 6.73 | 8.00 | mA | VDDO= 3.3V+5% |
| | | $I_{DD\_LVDS\_2.5V}$ | | 6.87 | 7.83 | mA | VDDO= 2.5V+5% |
| 8 | Current dissipation per HCSL output | $I_{DD\_HCSL\_3.3V}$ | | 16.43 | 19.87 | mA | VDDO= 3.3V+5% |
| | | $I_{DD\_HCSL\_2.5V}$ | | 17.14 | 19.18 | mA | VDDO= 2.5V+5% |

## Table 8 Input Characteristics*

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | CMOS high-level input voltage for control inputs | $V_{CIH}$ | 1.05 | | | V | |
| 2 | CMOS low-level input voltage for control inputs | $V_{CIL}$ | | | 0.45 | V | |
| 3 | CMOS input leakage current for control inputs (includes current due to pull down resistors) | $I_{IL}$ | -25 | | 50 | µA | $V_I = V_{DD}$ or 0 V |
| 4 | Differential input common mode voltage for IN0_p/n and IN1_p/n | $V_{CM}$ | 1 | | 2 | V | |
| 5 | Differential input voltage difference for IN0_p/n and IN1_p/n f ≤ 1GHz ** | $V_{ID}$ | 0.15 | | 1.3 | V | |
| 6 | Differential input voltage difference for IN0_p/n and IN1_p/n for 1GHz < f ≤ 1.6GHz ** | $V_{ID}$ | 0.35 | | 1.3 | V | |
| 7 | Differential input leakage current for IN0_p/n and IN1_p/n (includes current due to pull-up and pull-down resistors) | $I_{IL}$ | -150 | | 150 | µA | $V_I = 2V$ or 0V |
| 8 | Single ended input voltage for IN0_p and IN1_p | $V_{SI}$ | -0.3 | | 2.7 | V | VDD = 3.3V or 2.5V |
| 9 | Single ended input common mode voltage (IN0_p/n and IN1_p/n) | $V_{SIC}$ | 1 | | 2 | V | VDD = 3.3V or 2.5V |
| 10 | Single ended input voltage swing for IN0_p and IN1_p | $V_{SID}$ | 0.3 | | 1.3 | V | VDD = 3.3V or 2.5V |
| 11 | Input frequency (differential) | $f_{IN}$ | 0 | | 1600 | MHz | |
| 12 | Input frequency (LVCMOS) | $f_{IN\_CMOS}$ | 0 | | 250 | MHz | |
| 13 | Input duty cycle | dc | 35% | | 65% | | |
| 14 | Input slew rate | slew | | 2 | | V/ns | |
| 15 | Input pull-up/ pull-down resistance | $R_{PU}/R_{PD}$ | | 60kΩ | | | |
| 16 | Input pull-down resistance for INx_p | $R_{PD}$ | | 30kΩ | | | |
| 17 | Input multiplexer isolation IN0_p/n to IN1_p/n and vice versa Power on both inputs 0dBm, $f_{OFFSET}$ > 50kHz | Iso | | -84 | | dBc | $f_{IN}$ = 100 MHz |
| | | | | -82 | | | $f_{IN}$ = 200 MHz |
| | | | | -71 | | | $f_{IN}$ = 400 MHz |
| | | | | -67 | | | $f_{IN}$ = 800 MHz |

\* Values are over Recommended Operating Conditions
\* Values are over all two power supply modes ($V_{DD}$ = 3.3V and $V_{DD}$ = 2.5V)
\* Input mux isolation is measured as amplitude of $f_{OFFSET}$ spur in dBc on the output clock phase noise plot
\*\*Input differential voltage is calculated as $V_{ID} = V_{IH} - V_{IL}$ where $V_{IH}$ and $V_{IL}$ are input voltage high and low respectively. It should not be confused with $V_{ID} = 2 * (V_{IH} - V_{IL})$ used in some datasheets. Please refer to Figure 44.
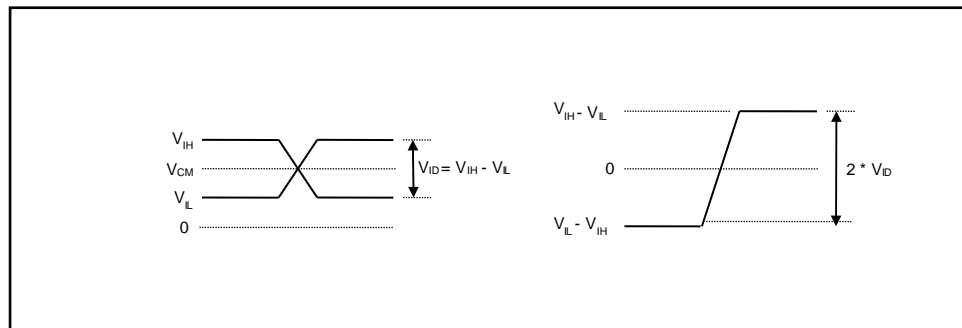


**Figure 44.      Differential Input Voltage Levels**

### Table 9 Crystal Oscillator Characteristics*

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Mode of oscillation | mode | | Fundamental | | | |
| 2 | Frequency | f | 8 | | 160 | MHz | |
| 3 | On chip load capacitance in SPI controlled mode | $C_L$ | 0 | | 21.75 | pF | Programmable |
| 4 | On chip load capacitance in pin controlled mode | | | 4 | | pF | Fixed |
| 5 | On chip series resistor in SPI controlled mode | $R_S$ | 0 | | 312 | Ω | Programmable |
| 6 | On chip series resistor in pin controlled mode | | | 84 | | Ω | Fixed |
| 7 | On chip shunt resistor | R | | 500 | | kΩ | |
| 8 | Frequency in overdrive mode[1] | $f_{OV}$ | 0.1 | | 250 | MHz | Functional but may not meet AC parameters Minimum depends on AC coupling Capacitor (0.1uF assumed) |
| 9 | Frequency in bypass mode[2] | $f_{BP}$ | 0 | | 250 | MHz | Functional but may not meet AC parameters |

\* Values are over Recommended Operating Conditions
\* Values are over all two power supply modes ($V_{DD}$ = 3.3V and $V_{DD}$ = 2.5V)

(1)     Maximum input level is 2V
(2)     Maximum output level is VDD

### Table 10 Power Supply Rejection Ratio for VDD = VDDO = 3.3V*

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | PSRR for LVPECL output | $PSRR_{LVPECL}$ | | -71.75 | | dBc | $f_{IN}$ = 156.25 MHz |
| | | | | -84.45 | | | $f_{IN}$ = 312.5 MHz |
| | | | | -82.11 | | | $f_{IN}$ = 625 MHz |
| 2 | PSRR for LVDS output | $PSRR_{LVDS}$ | | -95.16 | | dBc | $f_{IN}$ = 156.25 MHz |
| | | | | -97.77 | | | $f_{IN}$ = 312.5 MHz |
| | | | | -79.23 | | | $f_{IN}$ = 625 MHz |
| 3 | PSRR for HCSL output | $PSRR_{HCSL}$ | | -77.15 | | dBc | $f_{IN}$ = 100 MHz |
| | | | | -76.75 | | | $f_{IN}$ = 156.25 MHz |
| | | | | -80.44 | | | $f_{IN}$ = 312.5 MHz |

\* Values are over Recommended Operating Conditions
\* Noise injected to VDDO power supply with frequency 100 kHz and amplitude 100 mVpp
\* PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot

## Table 11 Power Supply Rejection Ratio for VDD = VDDO = 2.5V*

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | PSRR for LVPECL output | PSRR$_{LVPECL}$ | | -73.68 | | dBc | $f_{IN}$ = 156.25 MHz |
| | | | | -78.88 | | | $f_{IN}$ = 312.5 MHz |
| | | | | -71.82 | | | $f_{IN}$ = 625 MHz |
| 2 | PSRR for LVDS output | PSRR$_{LVDS}$ | | -90.04 | | dBc | $f_{IN}$ = 156.25 MHz |
| | | | | -79.99 | | | $f_{IN}$ = 312.5 MHz |
| | | | | -73.45 | | | $f_{IN}$ = 625 MHz |
| 3 | PSRR for HCSL output | PSRR$_{HCSL}$ | | -92.16 | | dBc | $f_{IN}$ = 100 MHz |
| | | | | -74.08 | | | $f_{IN}$ = 156.25 MHz |
| | | | | -91.88 | | | $f_{IN}$ = 312.5 MHz |

\* Values are over Recommended Operating Conditions
\* Noise injected to VDDO power supply with frequency 100 kHz and amplitude 100 mVpp
\* PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot

## Table 12 LVCMOS Output Characteristics for VDDO = 3.3V*

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Output high voltage (1mA load) | V$_{OH}$ | VDDO-0.1 | | | V | DC Measurement |
| 2 | Output low voltage (1mA load) | V$_{OL}$ | | | 0.1 | V | DC Measurement |
| 3 | Output High Current (Load adjusted to Vout = VDDO/2) | I$_{OH}$ | | 30 | | mA | DC Measurement |
| 4 | Output Low Current (Load adjusted to Vout = VDDO/2) | I$_{OL}$ | | 34 | | mA | DC Measurement |
| 5 | Output impedance | R$_O$ | | 15 | | Ω | DC Measurement |
| 6 | Rise time (20% to 80%) | t$_r$ | | 220 | 310 | ps | |
| 7 | Fall time (20% to 80%) | t$_f$ | | 320 | 365 | ps | |
| 8 | Output frequency | F$_O$ | 0 | | 250 | MHz | |
| 9 | Input to output delay | t$_{IOD}$ | 1.07 | 1.28 | 2.07 | ns | |
| 10 | Output enable time | t$_{EN}$ | | | 3 | cycles | |
| 11 | Output disable time | T$_{DIS}$ | | | 3 | cycles | |
| 12 | Additive RMS jitter in 1MHz to 5MHz band | T$_{j\_1M\_5M}$ | | 46 | 80 | fs | Input Clock 25MHz |
| 13 | Additive RMS jitter in 12kHz to 5MHz band | T$_{j\_12K\_5M}$ | | 56 | 90 | fs | Input Clock 25MHz |
| 14 | Additive RMS jitter in 1MHz to 20MHz band | T$_{j\_1M\_20M}$ | | 60 | 79 | fs | Input Clock 125MHz |
| 15 | Additive RMS jitter in 12kHz to 20MHz band | T$_{j\_12k\_20M}$ | | 65 | 86 | fs | Input Clock 125MHz |
| 16 | Additive RMS jitter in 1MHz to 20MHz band | T$_{j\_1M\_20M}$ | | 61 | 94 | fs | Input Clock 156.25MHz |
| 17 | Additive RMS jitter in 12kHz to 20MHz band | T$_{j\_12k\_20M}$ | | 66 | 100 | fs | Input Clock 156.25MHz |
| 18 | Noise floor | N$_F$ | | -165 | -162 | dBc/Hz | Input clock: 25 MHz |
| 19 | | | | -160 | -156 | dBc/Hz | Input clock: 125 MHz |
| 20 | | | | -158 | -153 | dBc/Hz | Input clock: 156.25 MHz |

\* Values are over Recommended Operating Conditions

## Table 13 LVCMOS Output Characteristics for VDDO = 2.5V*

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Output high voltage (1 mA load) | $V_{OH}$ | VDDO-0.1 | | | V | DC Measurement |
| 2 | Output low voltage (1 mA load) | $V_{OL}$ | | | 0.1 | V | DC Measurement |
| 3 | Output High Current (Load adjusted to Vout = VDDO/2) | $I_{OH}$ | | 21 | | mA | DC Measurement |
| 4 | Output Low Current (Load adjusted to Vout = VDDO/2) | $I_{OL}$ | | 25 | | mA | DC Measurement |
| 5 | Output impedance | $R_O$ | | 15 | | Ω | DC Measurement |
| 6 | Rise time (20% to 80%) | $t_r$ | | 225 | 310 | ps | |
| 7 | Fall time (20% to 80%) | $t_f$ | | 320 | 365 | ps | |
| 8 | Output frequency | $F_O$ | 0 | | 250 | MHz | |
| 9 | Input to output delay | $t_{IOD}$ | 1.10 | 1.41 | 2.30 | ns | |
| 10 | Output enable time | $t_{EN}$ | | | 3 | cycles | |
| 11 | Output disable time | $T_{DIS}$ | | | 3 | cycles | |
| 12 | Additive RMS jitter in 1MHz to 5MHz band | $T_{j\_1M\_5M}$ | | 51 | 104 | fs | Input Clock 25MHz |
| 13 | Additive RMS jitter in 12kHz to 5MHz band | $T_{j\_12k\_5M}$ | | 62 | 111 | fs | Input Clock 25MHz |
| 14 | Additive RMS jitter in 1MHz to 20MHz band | $T_{j\_1M\_20M}$ | | 64 | 81 | fs | Input Clock 125MHz |
| 15 | Additive RMS jitter in 12kHz to 20MHz band | $T_{j\_12k\_20M}$ | | 70 | 88 | fs | Input Clock 125MHz |
| 16 | Additive RMS jitter in 1MHz to 20MHz band | $T_{j\_1M\_20M}$ | | 62 | 94 | fs | Input Clock 156.25MHz |
| 17 | Additive RMS jitter in 12kHz to 20MHz band | $T_{j\_12k\_20M}$ | | 68 | 100 | fs | Input Clock 156.25MHz |
| 18 | | | | -164 | -161 | dBc/Hz | Input clock: 25 MHz |
| 19 | Noise floor | $N_F$ | | -159 | -155 | dBc/Hz | Input clock: 125 MHz |
| 20 | | | | -158 | -153 | dBc/Hz | Input clock: 156.25 MHz |

* Values are over Recommended Operating Conditions

**Table 14 LVPECL Output Characteristics for VDDO = 3.3V\***

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Output high voltage | $V_{LVPECL\_OH}$ | 1.9 | 2.08 | 2.4 | V | DC Measurement |
| 2 | Output low voltage | $V_{LVPECL\_OL}$ | 1.2 | 1.36 | 1.7 | V | DC Measurement |
| 3 | Output differential swing\*\* | $V_{LVPECL\_SW}$ | 0.6 | 0.72 | 0.9 | V | DC Measurement |
| 4 | Variation of $V_{LVPECL\_SW}$ for complementary output states | $\Delta V_{LVPECL\_SW}$ | 0 | 0.02 | 0.07 | V | |
| 5 | Common mode output | $V_{CM}$ | 1.6 | 1.72 | 2.1 | V | |
| 7 | Output frequency when $V_{LVPECL\_SW} \geq 0.6V$ | $F_{MAX\_0.6VSW}$ | | | 800 | MHz | |
| 8 | Output frequency when $V_{LVPECL\_SW} \geq 0.4V$ | $F_{MAX\_0.4VSW}$ | | | 1600 | MHz | |
| 9 | Rise or fall time (20% to 80%) | $t_r, t_f$ | | 110 | 170 | ps | |
| 10 | Output frequency | $F_O$ | 0 | | 1600 | MHz | |
| 11 | Output to output skew | $t_{OOSK}$ | | | 40 | ps | |
| 12 | Device to device output skew | $t_{DOOSK}$ | | | 120 | ps | |
| 13 | Input to output delay | $t_{IOD}$ | 0.73 | 0.87 | 1.1 | ns | |
| 14 | Output enable time | $t_{EN}$ | | | 3 | cycles | |
| 15 | Output disable time | $t_{DIS}$ | | | 3 | cycles | |
| 16 | Additive RMS jitter in 1MHz to 20MHz band | $T_{j\_1M\_20M}$ | | 68 | 96 | fs | Input clock: 100 MHz |
| | | | | 50 | 64 | fs | Input clock: 156.25MHz |
| | | | | 20 | 32 | fs | Input clock: 625 MHz |
| 17 | Additive RMS jitter in 12kHz to 20MHz band | $T_{j\_12k\_20M}$ | | 71 | 101 | fs | Input clock: 100 MHz |
| | | | | 55 | 70 | fs | Input clock: 156.25MHz |
| | | | | 25 | 39 | fs | Input clock: 625 MHz |
| 18 | Noise floor | $N_F$ | | -161 | -159 | dBc/Hz | Input clock: 100 MHz |
| | | | | -160 | -155 | dBc/Hz | Input clock: 156.25 MHz |
| | | | | -155 | -151 | dBc/Hz | Input clock: 625 MHz |

\* Values are over Recommended Operating Conditions

\*\*Output differential swing is calculated as $V_{SW} = V_{OH} - V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH} - V_{OL})$ used in some datasheets. . Please refer to Figure 45.



**Figure 45.       Differential Output Voltage Levels**

**Table 15 LVPECL Output Characteristics for VDDO = 2.5V***

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Output high voltage | $V_{LVPECL\_OH}$ | 1.1 | 1.28 | 1.7 | V | DC Measurement |
| 2 | Output low voltage | $V_{LVPECL\_OL}$ | 0.4 | 0.57 | 0.9 | V | DC Measurement |
| 3 | Output differential swing** | $V_{LVPECL\_SW}$ | 0.6 | 0.71 | 0.9 | V | DC Measurement |
| 4 | Variation of $V_{LVPECL\_SW}$ for complementary output states | $\Delta V_{LVPECL\_SW}$ | 0 | 0.02 | 0.05 | V | |
| 5 | Common mode output | $V_{CM}$ | 0.8 | 0.92 | 1.2 | V | |
| 7 | Output frequency when $V_{LVPECL\_SW} \geq 0.6V$ | $F_{MAX\_0.6VSW}$ | | | 800 | MHz | |
| 8 | Output frequency when $V_{LVPECL\_SW} \geq 0.4V$ | $F_{MAX\_0.4VSW}$ | | | 1600 | MHz | |
| 9 | Rise or fall time (20% to 80%) | $t_r$, $t_f$ | | 120 | 170 | ps | |
| 10 | Output frequency | $F_O$ | 0 | | 1600 | MHz | |
| 11 | Output to output skew | $t_{OOSK}$ | | | 40 | ps | |
| 12 | Device to device output skew | $t_{DOOSK}$ | | | 120 | ps | |
| 13 | Input to output delay | $t_{IOD}$ | 0.75 | 0.87 | 1.1 | ns | |
| 14 | Output enable time | $t_{EN}$ | | | 3 | cycles | |
| 15 | Output disable time | $t_{DIS}$ | | | 3 | cycles | |
| 16 | Additive RMS jitter in 1MHz to 20MHz band | $T_{j\_1M\_20M}$ | | 65 | 91 | fs | Input clock: 100 MHz |
| | | | | 50 | 64 | fs | Input clock: 156.25MHz |
| | | | | 20 | 30 | fs | Input clock: 625 MHz |
| 17 | Additive RMS jitter in 12kHz to 20MHz band | $T_{j\_12k\_20M}$ | | 69 | 99 | fs | Input clock: 100 MHz |
| | | | | 54 | 75 | fs | Input clock: 156.25MHz |
| | | | | 26 | 41 | fs | Input clock: 625 MHz |
| 18 | Noise floor | $N_F$ | | -161 | -159 | dBc/Hz | Input clock: 100 MHz |
| | | | | -160 | -156 | dBc/Hz | Input clock: 156.25 MHz |
| | | | | -155 | -151 | dBc/Hz | Input clock: 625 MHz |

* Values are over Recommended Operating Conditions

**Output differential swing is calculated as $V_{SW} = V_{OH} - V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH} - V_{OL})$ used in some datasheets. Please refer to Figure 45.

### Table 16 LVDS Outputs for VDDO = 3.3V*

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Output high voltage | $V_{LVDS\_OH}$ | 1.3 | 1.39 | 1.47 | V | DC Measurement |
| 2 | Output low voltage | $V_{LVDS\_OL}$ | 1.0 | 1.07 | 1.15 | V | DC Measurement |
| 3 | Output differential swing** | $V_{LVDS\_SW}$ | 0.25 | 0.32 | 0.39 | V | DC Measurement |
| 4 | Variation of $V_{LVDS\_SW}$ for complementary output states | $\Delta V_{LVDS\_SW}$ | 0 | 0.002 | 0.01 | V | |
| 5 | Common mode output | $V_{CM}$ | 1.15 | 1.23 | 1.3 | V | |
| 6 | Variation of $V_{CM}$ for complementary output states | $\Delta V_{CM}$ | 0 | 0.001 | 0.01 | V | |
| 7 | Output frequency when $V_{LVDS\_SW} \geq 250mV$ | $F_{MAX\_0.25VSW}$ | | | 800 | MHz | |
| 8 | Output frequency when $V_{LVDS\_SW} \geq 200mV$ | $F_{MAX\_0.2VSW}$ | | | 1600 | MHz | |
| 9 | Rise or fall time (20% to 80%) | $t_r$, $t_f$ | | 110 | 170 | ps | |
| 10 | Output frequency | $F_O$ | 0 | | 1600 | MHz | |
| 11 | Output to output skew | $t_{OOSK}$ | | | 20 | ps | |
| 12 | Device to device output skew | $t_{DOOSK}$ | | | 130 | ps | |
| 13 | Input to output delay | $t_{IOD}$ | 0.76 | 0.86 | 1.1 | ns | |
| 14 | Output Short Circuit Current Single Ended | $I_S$ | -24 | | 24 | mA | Single ended outputs shorted to GND |
| 15 | Output Short Circuit Current Differential | $I_{SD}$ | -24 | | 24 | mA | Complementary outputs shorted |
| 16 | Output enable time | $t_{EN}$ | | | 3 | cycles | |
| 17 | Output disable time | $t_{DIS}$ | | | 3 | cycles | |
| 18 | Additive RMS jitter in 1MHz to 20MHz band | $T_{j\_1M\_20M}$ | | 110 | 144 | fs | Input clock: 100 MHz |
| | | | | 63 | 81 | fs | Input clock: 156.25MHz |
| | | | | 21 | 33 | fs | Input clock: 625 MHz |
| 19 | Additive RMS jitter in 12kHz to 20MHz band | $T_{j\_12k\_20M}$ | | 115 | 150 | fs | Input clock: 100 MHz |
| | | | | 73 | 102 | fs | Input clock: 156.25MHz |
| | | | | 26 | 40 | fs | Input clock: 625 MHz |
| 20 | Noise floor | $N_F$ | | -158 | -156 | dBc/Hz | Input clock: 100 MHz |
| | | | | -158 | -155 | dBc/Hz | Input clock: 156.25 MHz |
| | | | | -154 | -151 | dBc/Hz | Input clock: 625 MHz |

* Values are over Recommended Operating Conditions

**Output differential swing is calculated as $V_{SW} = V_{OH} - V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH} - V_{OL})$ used in some datasheets. Please refer to Figure 45.
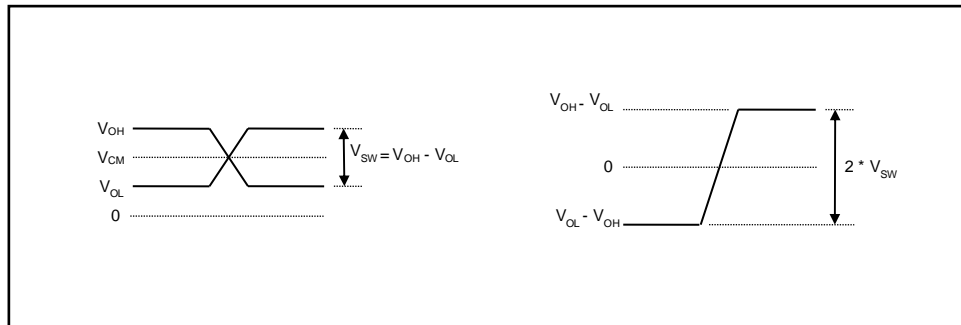
**Table 17 LVDS Outputs for VDDO = 2.5V***

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Output high voltage | $V_{LVDS\_OH}$ | 1.3 | 1.4 | 1.5 | V | DC Measurement |
| 2 | Output low voltage | $V_{LVDS\_OL}$ | 0.97 | 1.05 | 1.13 | V | DC Measurement |
| 3 | Output differential swing** | $V_{LVDS\_SW}$ | 0.25 | 0.35 | 0.44 | V | DC Measurement |
| 4 | Variation of $V_{LVDS\_SW}$ for complementary output states | $\Delta V_{LVDS\_SW}$ | 0 | 0.001 | 0.01 | V | |
| 5 | Common mode output | $V_{CM}$ | 1.15 | 1.23 | 1.3 | V | |
| 6 | Variation of $V_{CM}$ for complementary output states | $\Delta V_{CM}$ | 0 | 0.001 | 0.01 | V | |
| 7 | Output frequency when $V_{LVDS\_SW} \geq 250mV$ | $F_{MAX\_0.25VSW}$ | | | 800 | MHz | |
| 8 | Output frequency when $V_{LVDS\_SW} \geq 200mV$ | $F_{MAX\_0.2VSW}$ | | | 1600 | MHz | |
| 9 | Rise or fall time (20% to 80%) | $t_r, t_f$ | | 110 | 170 | ps | |
| 10 | Output frequency | $F_O$ | 0 | | 1600 | MHz | |
| 11 | Output to output skew | $t_{OOSK}$ | | | 20 | ps | |
| 12 | Device to device output skew | $t_{DOOSK}$ | | | 130 | ps | |
| 13 | Input to output delay | $t_{IOD}$ | 0.78 | 0.86 | 1.12 | ns | |
| 14 | Output Short Circuit Current Single Ended | $I_S$ | -24 | | 24 | mA | Single ended outputs shorted to GND |
| 15 | Output Short Circuit Current Differential | $I_{SD}$ | -24 | | 24 | mA | Complementary outputs shorted |
| 16 | Output enable time | $t_{EN}$ | | | 3 | cycles | |
| 17 | Output disable time | $t_{DIS}$ | | | 3 | cycles | |
| 18 | Additive RMS jitter in 1MHz to 20MHz band | $T_{j\_1M\_20M}$ | | 107 | 140 | fs | Input clock: 100 MHz |
| | | | | 62 | 77 | fs | Input clock: 156.25MHz |
| | | | | 20 | 31 | fs | Input clock: 625 MHz |
| 19 | Additive RMS jitter in 12kHz to 20MHz band | $T_{j\_12k\_20M}$ | | 111 | 146 | fs | Input clock: 100 MHz |
| | | | | 66 | 83 | fs | Input clock: 156.25MHz |
| | | | | 24 | 36 | fs | Input clock: 625 MHz |
| 20 | Noise floor | $N_F$ | | -158 | -156 | dBc/Hz | Input clock: 100 MHz |
| | | | | -159 | -155 | dBc/Hz | Input clock: 156.25 MHz |
| | | | | -155 | -151 | dBc/Hz | Input clock: 625 MHz |

* Values are over Recommended Operating Conditions
**Output differential swing is calculated as $V_{SW} = V_{OH}-V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH}-V_{OL})$ used in some datasheets. Please refer to Figure 45.

## Table 18 HCSL Outputs for VDDO = 3.3V*

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Output high voltage | $V_{HCSL\_OH}$ | 0.6 | 0.85 | 1.1 | V | DC Measurement |
| 2 | Output low voltage | $V_{HCSL\_OL}$ | -0.05 | 0 | 0.05 | V | DC Measurement |
| 3 | Output differential swing** | $V_{HCSL\_SW}$ | 0.6 | 0.85 | 1.1 | V | DC Measurement |
| 4 | Variation of $V_{HCSL\_SW}$ for complementary output states | $\Delta V_{HCSL\_SW}$ | 0 | 0.003 | 0.05 | V | |
| 5 | Common mode output | $V_{CM}$ | 0.28 | 0.43 | 0.55 | V | |
| 6 | Variation of $V_{CM}$ for complementary output states | $\Delta V_{CM}$ | 0 | 0.002 | 0.05 | V | |
| 7 | Absolute Crossing Voltage | $V_{CROSS}$ | 0.320 | 0.384 | 0.447 | V | |
| 8 | Total Variation of $V_{CROSS}$ | $\Delta V_{CROSS}$ | | | 0.127 | V | |
| 9 | Output frequency | $F_{MAX}$ | 0 | | 400 | MHz | |
| 10 | Rise or fall time (20% to 80%) | $t_r$, $t_f$ | | 143 | 309 | ps | |
| 11 | Output to output skew | $t_{OOSK}$ | | | 21 | ps | |
| 12 | Device to device output skew | $t_{DOOSK}$ | | | 129 | ps | |
| 13 | Input to output delay | $t_{IOD}$ | 0.73 | 0.90 | 1.08 | ns | |
| 14 | Output enable time | $t_{EN}$ | | | 3 | cycles | |
| 15 | Output disable time | $t_{DIS}$ | | | 3 | cycles | |
| 16 | Additive Jitter as per PCIe 3.0 (PLL_BW = 2 to 5MHz, CDR = 10MHz) | $T_{jPCIe\_3.0}$ | | 20 | 40 | fs | Input clock: 100MHz |
| 17 | Additive RMS jitter in 1MHz to 20MHz band | $T_{j\_1M\_20M}$ | | 73 | 104 | fs | Input clock: 100 MHz |
| | | | | 53 | 69 | fs | Input clock: 156.25MHz |
| 18 | Additive RMS jitter in 12kHz to 20MHz band | $T_{j\_12k\_20M}$ | | 77 | 112 | fs | Input clock: 100 MHz |
| | | | | 64 | 100 | fs | Input clock: 156.25MHz |
| 19 | Noise floor | $N_F$ | | -161 | -159 | dBc/Hz | Input clock: 100 MHz |
| | | | | -159 | -155 | dBc/Hz | Input clock: 156.25 MHz |

* Values are over Recommended Operating Conditions

**Output differential swing is calculated as $V_{SW} = V_{OH}-V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH}-V_{OL})$ used in some datasheets. Please refer to Figure 45.

## Table 19 HCSL Outputs for VDDO = 2.5V*

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Output high voltage | $V_{HCSL\_OH}$ | 0.6 | 0.83 | 1.1 | V | DC Measurement |
| 2 | Output low voltage | $V_{HCSL\_OL}$ | -0.05 | 0 | 0.05 | V | DC Measurement |
| 3 | Output differential swing** | $V_{HCSL\_SW}$ | 0.5 | 0.83 | 1.1 | V | DC Measurement |
| 4 | Variation of $V_{HCSL\_SW}$ for complementary output states | $\Delta V_{HCSL\_SW}$ | 0 | 0.003 | 0.05 | V | |
| 5 | Common mode output | $V_{CM}$ | 0.28 | 0.42 | 0.55 | V | |
| 6 | Variation of $V_{CM}$ for complementary output states | $\Delta V_{CM}$ | 0 | 0.002 | 0.05 | V | |
| 7 | Absolute Crossing Voltage | $V_{CROSS}$ | 0.260 | 0.316 | 0.372 | V | |
| 8 | Total Variation of $V_{CROSS}$ | $\Delta V_{CROSS}$ | | | 0.108 | V | |
| 9 | Output frequency | $F_{MAX}$ | 0 | | 400 | MHz | |
| 10 | Rise or fall time (20% to 80%) | $t_r, t_f$ | | 125 | 162 | ps | |
| 11 | Output to output skew | $t_{OOSK}$ | | | 21 | ps | |
| 12 | Device to device output skew | $t_{DOOSK}$ | | | 129 | ps | |
| 13 | Input to output delay | $t_{IOD}$ | 0.76 | 0.92 | 1.10 | ns | |
| 14 | Output enable time | $t_{EN}$ | | | 3 | cycles | |
| 15 | Output disable time | $t_{DIS}$ | | | 3 | cycles | |
| 16 | Additive Jitter as per PCIe 3.0 (PLL_BW = 2 to 5MHz, CDR = 10MHz) | $T_{jPCIe\_3.0}$ | | 20 | 40 | fs | Input clock: 100MHz |
| 17 | Additive RMS jitter in 1MHz to 20MHz band | $T_{j\_1M\_20M}$ | | 68 | 95 | fs | Input clock: 100 MHz |
| | | | | 52 | 66 | fs | Input clock: 156.25MHz |
| 18 | Additive RMS jitter in 12kHz to 20MHz band | $T_{j\_12k\_20M}$ | | 72 | 102 | fs | Input clock: 100 MHz |
| | | | | 56 | 71 | fs | Input clock: 156.25MHz |
| 19 | Noise floor | $N_F$ | | -161 | -158 | dBc/Hz | Input clock: 100 MHz |
| | | | | -160 | -153 | dBc/Hz | Input clock: 156.25 MHz |

\* Values are over Recommended Operating Conditions
\*\*Output differential swing is calculated as $V_{SW} = V_{OH} - V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH} - V_{OL})$ used in some datasheets. Please refer to Figure 45.

**Table 20 LVCMOS Output Phase Noise with 25 MHz XTAL***

| | Characteristics | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | Jitter RMS in 12kHz to 5MHz band | | 103 | | fs | VDD = 3.3V, VDDO = 3.3V |
| | | | 117 | | fs | VDD = 2.5V; VDDO = 2.5V |
| 2 | Noise floor | | -75 | | dBc/Hz | @10Hz , VDD = 3.3V, VDDO = 3.3V |
| | | | -107 | | dBc/Hz | @100Hz, VDD = 3.3V, VDDO = 3.3V |
| | | | -132 | | dBc/Hz | @1kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -150 | | dBc/Hz | @10kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -162 | | dBc/Hz | @100kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -166 | | dBc/Hz | @1MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -166 | | dBc/Hz | @5MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -70 | | dBc/Hz | @10Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -102 | | dBc/Hz | @100Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -130 | | dBc/Hz | @1kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -149 | | dBc/Hz | @10kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -161 | | dBc/Hz | @100kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -165 | | dBc/Hz | @1MHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -165 | | dBc/Hz | @5MHz, VDD = 2.5V; VDDO = 2.5V |

* Values are over Recommended Operating Conditions

**Table 21 LVPECL Output Phase Noise with 25 MHz XTAL***

| | Characteristics | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | Jitter RMS in 12kHz to 5MHz band | | 265 | | fs | VDD = 3.3V, VDDO = 3.3V |
| | | | 213 | | fs | VDD = 2.5V; VDDO = 2.5V |
| 2 | Noise floor | | -75 | | dBc/Hz | @10Hz , VDD = 3.3V, VDDO = 3.3V |
| | | | -107 | | dBc/Hz | @100Hz, VDD = 3.3V, VDDO = 3.3V |
| | | | -133 | | dBc/Hz | @1kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -152 | | dBc/Hz | @10kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -157 | | dBc/Hz | @100kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -158 | | dBc/Hz | @1MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -157 | | dBc/Hz | @5MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -71 | | dBc/Hz | @10Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -103 | | dBc/Hz | @100Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -130 | | dBc/Hz | @1kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -151 | | dBc/Hz | @10kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -158 | | dBc/Hz | @100kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -160 | | dBc/Hz | @1MHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -159 | | dBc/Hz | @5MHz, VDD = 2.5V; VDDO = 2.5V |

* Values are over Recommended Operating Conditions

**Table 22 LVDS Output Phase Noise with 25 MHz XTAL**

| | Characteristics | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | Jitter RMS in 12kHz to 5MHza band | | 178 | | fs | VDD = 3.3V, VDDO = 3.3V |
| | | | 190 | | fs | VDD = 2.5V; VDDO = 2.5V |
| 2 | Noise floor | | -75 | | dBc/Hz | @10Hz , VDD = 3.3V, VDDO = 3.3V |
| | | | -107 | | dBc/Hz | @100Hz, VDD = 3.3V, VDDO = 3.3V |
| | | | -133 | | dBc/Hz | @1kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -154 | | dBc/Hz | @10kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -161 | | dBc/Hz | @100kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -161 | | dBc/Hz | @1MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -160 | | dBc/Hz | @5MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -68 | | dBc/Hz | @10Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -103 | | dBc/Hz | @100Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -130 | | dBc/Hz | @1kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -152 | | dBc/Hz | @10kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -161 | | dBc/Hz | @100kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -160 | | dBc/Hz | @1MHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -159 | | dBc/Hz | @5MHz, VDD = 2.5V; VDDO = 2.5V |

\* Values are over Recommended Operating Conditions

**Table 23 HCSL Output Phase Noise with 25 MHz XTAL**

| | Characteristics | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | Jitter RMS in 12kHz to 20MHz band | | 269 | | fs | VDD = 3.3V, VDDO = 3.3V |
| | | | 228 | | fs | VDD = 2.5V; VDDO = 2.5V |
| 2 | Noise floor | | -76 | | dBc/Hz | @10Hz , VDD = 3.3V, VDDO = 3.3V |
| | | | -107 | | dBc/Hz | @100Hz, VDD = 3.3V, VDDO = 3.3V |
| | | | -133 | | dBc/Hz | @1kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -152 | | dBc/Hz | @10kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -157 | | dBc/Hz | @100kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -157 | | dBc/Hz | @1MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -157 | | dBc/Hz | @5MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -73 | | dBc/Hz | @10Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -105 | | dBc/Hz | @100Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -131 | | dBc/Hz | @1kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -151 | | dBc/Hz | @10kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -158 | | dBc/Hz | @100kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -159 | | dBc/Hz | @1MHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -159 | | dBc/Hz | @5MHz, VDD = 2.5V; VDDO = 2.5V |

\* Values are over Recommended Operating Conditions

## Table 24 LVCMOS Output Phase Noise with 125 MHz XTAL*

| | Characteristics | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | Jitter RMS in 12kHz to 20MHz band | | 92 | | fs | VDD = 3.3V, VDDO = 3.3V |
| | | | 105 | | fs | VDD = 2.5V; VDDO = 2.5V |
| 2 | Noise floor | | -58 | | dBc/Hz | @10Hz , VDD = 3.3V, VDDO = 3.3V |
| | | | -90 | | dBc/Hz | @100Hz, VDD = 3.3V, VDDO = 3.3V |
| | | | -118 | | dBc/Hz | @1kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -136 | | dBc/Hz | @10kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -150 | | dBc/Hz | @100kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -158 | | dBc/Hz | @1MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -159 | | dBc/Hz | @10MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -53 | | dBc/Hz | @10Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -86 | | dBc/Hz | @100Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -113 | | dBc/Hz | @1kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -134 | | dBc/Hz | @10kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -148 | | dBc/Hz | @100kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -157 | | dBc/Hz | @1MHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -158 | | dBc/Hz | @10MHz, VDD = 2.5V; VDDO = 2.5V |

* Values are over Recommended Operating Conditions

## Table 25 LVPECL Output Phase Noise with 125 MHz XTAL*

| | Characteristics | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | Jitter RMS in 12kHz to 20MHz band | | 76 | | fs | VDD = 3.3V, VDDO = 3.3V |
| | | | 86 | | fs | VDD = 2.5V; VDDO = 2.5V |
| 2 | Noise floor | | -58 | | dBc/Hz | @10Hz , VDD = 3.3V, VDDO = 3.3V |
| | | | -90 | | dBc/Hz | @100Hz, VDD = 3.3V, VDDO = 3.3V |
| | | | -118 | | dBc/Hz | @1kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -140 | | dBc/Hz | @10kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -154 | | dBc/Hz | @100kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -159 | | dBc/Hz | @1MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -161 | | dBc/Hz | @10MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -54 | | dBc/Hz | @10Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -86 | | dBc/Hz | @100Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -114 | | dBc/Hz | @1kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -137 | | dBc/Hz | @10kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -152 | | dBc/Hz | @100kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -158 | | dBc/Hz | @1MHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -160 | | dBc/Hz | @10MHz, VDD = 2.5V; VDDO = 2.5V |

* Values are over Recommended Operating Conditions

### Table 26 LVDS Output Phase Noise with 125 MHz XTAL

| | Characteristics | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | Jitter RMS in 12kHz to 20MHz band | | 98 | | fs | VDD = 3.3V, VDDO = 3.3V |
| | | | 100 | | fs | VDD = 2.5V; VDDO = 2.5V |
| 2 | Noise floor | | -57 | | dBc/Hz | @10Hz , VDD = 3.3V, VDDO = 3.3V |
| | | | -90 | | dBc/Hz | @100Hz, VDD = 3.3V, VDDO = 3.3V |
| | | | -118 | | dBc/Hz | @1kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -140 | | dBc/Hz | @10kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -152 | | dBc/Hz | @100kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -157 | | dBc/Hz | @1MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -158 | | dBc/Hz | @10MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -54 | | dBc/Hz | @10Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -86 | | dBc/Hz | @100Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -114 | | dBc/Hz | @1kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -137 | | dBc/Hz | @10kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -153 | | dBc/Hz | @100kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -157 | | dBc/Hz | @1MHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -158 | | dBc/Hz | @10MHz, VDD = 2.5V; VDDO = 2.5V |

* Values are over Recommended Operating Conditions

### Table 27 HCSL Output Phase Noise with 125 MHz XTAL

| | Characteristics | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | Jitter RMS in 12kHz to 20MHz band | | 83 | | fs | VDD = 3.3V, VDDO = 3.3V |
| | | | 85 | | fs | VDD = 2.5V; VDDO = 2.5V |
| 2 | Noise floor | | -58 | | dBc/Hz | @10Hz , VDD = 3.3V, VDDO = 3.3V |
| | | | -90 | | dBc/Hz | @100Hz, VDD = 3.3V, VDDO = 3.3V |
| | | | -118 | | dBc/Hz | @1kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -140 | | dBc/Hz | @10kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -152 | | dBc/Hz | @100kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -158 | | dBc/Hz | @1MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -160 | | dBc/Hz | @10MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -54 | | dBc/Hz | @10Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -86 | | dBc/Hz | @100Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -114 | | dBc/Hz | @1kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -137 | | dBc/Hz | @10kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -153 | | dBc/Hz | @100kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -158 | | dBc/Hz | @1MHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -159 | | dBc/Hz | @10MHz, VDD = 2.5V; VDDO = 2.5V |

* Values are over Recommended Operating Conditions

### Table 28 LVCMOS Output Phase Noise with 156.25 MHz XTAL*

| | Characteristics | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | Jitter RMS in 12kHz to 20MHz band | | 79 | | fs | VDD = 3.3V, VDDO = 3.3V |
| | | | 88 | | fs | VDD = 2.5V; VDDO = 2.5V |
| 2 | Noise floor | | -53 | | dBc/Hz | @10Hz , VDD = 3.3V, VDDO = 3.3V |
| | | | -81 | | dBc/Hz | @100Hz, VDD = 3.3V, VDDO = 3.3V |
| | | | -111 | | dBc/Hz | @1kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -135 | | dBc/Hz | @10kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -149 | | dBc/Hz | @100kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -157 | | dBc/Hz | @1MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -159 | | dBc/Hz | @10MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -53 | | dBc/Hz | @10Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -82 | | dBc/Hz | @100Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -113 | | dBc/Hz | @1kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -135 | | dBc/Hz | @10kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -148 | | dBc/Hz | @100kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -156 | | dBc/Hz | @1MHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -158 | | dBc/Hz | @10MHz, VDD = 2.5V; VDDO = 2.5V |

* Values are over Recommended Operating Conditions

### Table 29 LVPECL Output Phase Noise with 156.25 MHz XTAL*

| | Characteristics | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | Jitter RMS in 12kHz to 20MHz band | | 61 | | fs | VDD = 3.3V, VDDO = 3.3V |
| | | | 68 | | fs | VDD = 2.5V; VDDO = 2.5V |
| 2 | Noise floor | | -52 | | dBc/Hz | @10Hz , VDD = 3.3V, VDDO = 3.3V |
| | | | -80 | | dBc/Hz | @100Hz, VDD = 3.3V, VDDO = 3.3V |
| | | | -111 | | dBc/Hz | @1kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -140 | | dBc/Hz | @10kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -153 | | dBc/Hz | @100kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -159 | | dBc/Hz | @1MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -161 | | dBc/Hz | @10MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -53 | | dBc/Hz | @10Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -81 | | dBc/Hz | @100Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -114 | | dBc/Hz | @1kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -140 | | dBc/Hz | @10kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -151 | | dBc/Hz | @100kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -158 | | dBc/Hz | @1MHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -160 | | dBc/Hz | @10MHz, VDD = 2.5V; VDDO = 2.5V |

* Values are over Recommended Operating Conditions

**Table 30 LVDS Output Phase Noise with 156.25 MHz XTAL**

| | Characteristics | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | Jitter RMS in 12kHz to 20MHz band | | 79 | | fs | VDD = 3.3V, VDDO = 3.3V |
| | | | 76 | | fs | VDD = 2.5V; VDDO = 2.5V |
| 2 | Noise floor | | -52 | | dBc/Hz | @10Hz , VDD = 3.3V, VDDO = 3.3V |
| | | | -81 | | dBc/Hz | @100Hz, VDD = 3.3V, VDDO = 3.3V |
| | | | -111 | | dBc/Hz | @1kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -138 | | dBc/Hz | @10kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -148 | | dBc/Hz | @100kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -157 | | dBc/Hz | @1MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -159 | | dBc/Hz | @10MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -52 | | dBc/Hz | @10Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -82 | | dBc/Hz | @100Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -113 | | dBc/Hz | @1kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -140 | | dBc/Hz | @10kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -151 | | dBc/Hz | @100kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -157 | | dBc/Hz | @1MHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -159 | | dBc/Hz | @10MHz, VDD = 2.5V; VDDO = 2.5V |

* Values are over Recommended Operating Conditions

**Table 31 HCSL Output Phase Noise with 156.25 MHz XTAL**

| | Characteristics | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | Jitter RMS in 12kHz to 20MHz band | | 72 | | fs | VDD = 3.3V, VDDO = 3.3V |
| | | | 72 | | fs | VDD = 2.5V; VDDO = 2.5V |
| 2 | Noise floor | | -53 | | dBc/Hz | @10Hz , VDD = 3.3V, VDDO = 3.3V |
| | | | -86 | | dBc/Hz | @100Hz, VDD = 3.3V, VDDO = 3.3V |
| | | | -114 | | dBc/Hz | @1kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -139 | | dBc/Hz | @10kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -148 | | dBc/Hz | @100kHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -157 | | dBc/Hz | @1MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -160 | | dBc/Hz | @10MHz, VDD = 3.3V, VDDO = 3.3V |
| | | | -53 | | dBc/Hz | @10Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -86 | | dBc/Hz | @100Hz, VDD = 2.5V; VDDO = 2.5V |
| | | | -115 | | dBc/Hz | @1kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -140 | | dBc/Hz | @10kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -151 | | dBc/Hz | @100kHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -157 | | dBc/Hz | @1MHz, VDD = 2.5V; VDDO = 2.5V |
| | | | -160 | | dBc/Hz | @10MHz, VDD = 2.5V; VDDO = 2.5V |

* Values are over Recommended Operating Conditions

## Table 32 AC Electrical Characteristics* - SPI (Serial Peripheral Interface) Timing

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | sck period | tcyc | 124 | | | ns | See Figure 46& Figure 47 |
| 2 | sck pulse width low | tclkl | 62 | | | ns | |
| 3 | sck pulse width high | tclkh | 62 | | | ns | |
| 4 | si setup (write) from sck rising edge | trxs | 10 | | | ns | |
| 5 | si hold (write) from sck falling edge | trxh | 10 | | | ns | |
| 6 | so delay (read) from sck falling edge | txd | | | 25 | ns | |
| 7 | cs_b to output high impedance | tohz | | | 60 | ns | |
| 8 | cs_b setup from sck falling edge (LSB first) | tcssi | 20 | | | ns | See Figure 46 |
| 9 | cs_b hold from sck falling edge (LSB first) | tcshi | 10 | | | ns | |
| 10 | cs_b setup from sck falling edge (MSB first) | tcssm | 20 | | | ns | See Figure 47 |
| 11 | cs_b hold from sck falling edge (MSB first) | tcshm | 10 | | | ns | |

* Values are over Recommended Operating Conditions
* For LSB first mode timing diagram, refer to Figure 46
* For MSB first mode timing diagram, refer to Figure 47
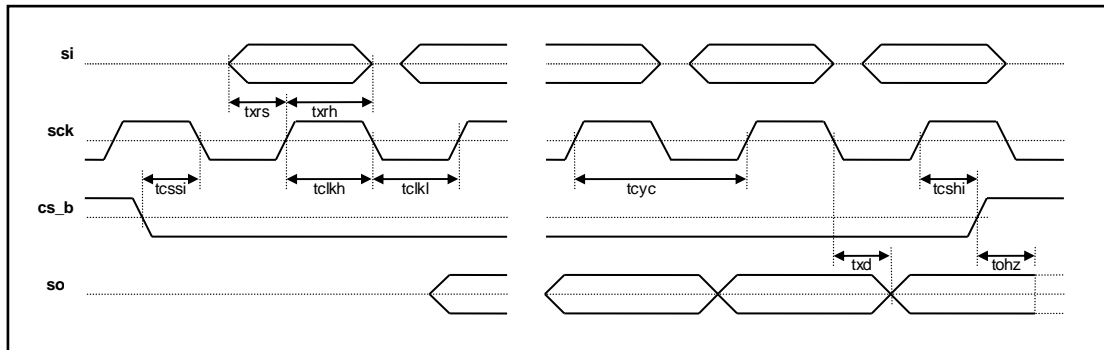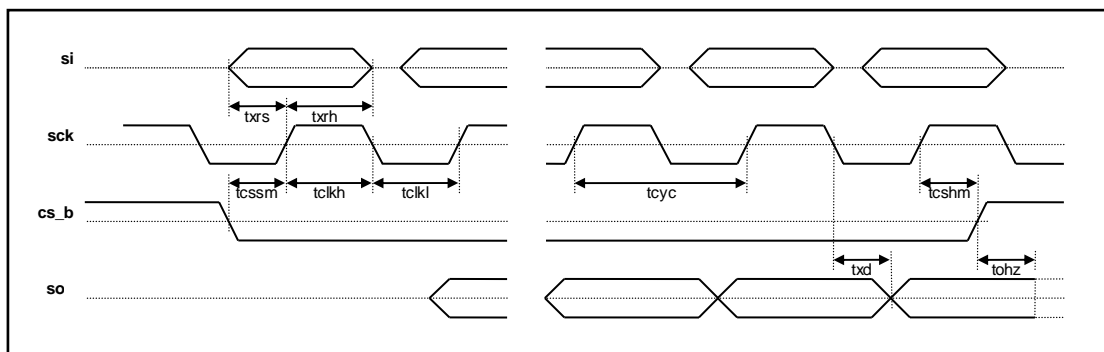* Values shown are proposed for the data sheet, these values are to be confirmed



**Figure 46.  SPI (Serial Peripheral Interface) Timing - LSB First Mode**



**Figure 47.  SPI (Serial Peripheral Interface) Timing - MSB First Mode**

**Table 33 6x6mm QFN Package Thermal Properties**

| Parameter | Symbol | Condition | Value | Units |
|---|---|---|---|---|
| Maximum Ambient Temperature | $T_A$ | | 85 | °C |
| Maximum Junction Temperature | $T_{JMAX}$ | | 125 | °C |
| Junction to Ambient Thermal Resistance[1] (Note 1) | $\theta_{JA}$ | still air | 22.2 | °C/W |
| | | 1m/s airflow | 17.6 | |
| | | 2.5m/s airflow | 15.8 | |
| Junction to Board Thermal Resistance | $\theta_{JB}$ | | 7.2 | °C/W |
| Junction to Case Thermal Resistance | $\theta_{JC}$ | | 14.3 | °C/W |
| Junction to Pad Thermal Resistance[2] | $\theta_{JP}$ | Still air | 3.9 | °C/W |
| Junction to Top-Center Thermal Characterization Parameter | $\psi_{JT}$ | Still air | 0.2 | °C/W |

(1)    Theta-JA ($\theta_{JA}$) is the thermal resistance from junction to ambient when the package is mounted on an 4-layer JEDEC standard test board and dissipating maximum power

(2)    Theta-JP ($\theta_{JP}$) is the thermal resistance from junction to the center exposed pad on the bottom of the package)

## Change History

June 2017 was the first release of the document.

July 2017 release changes:

- Modified power calculation in the Power Consumption section.

August 2017 release changes:

- Modified "Input driven by HCSL output" figure.

- Modified additive jitter for 156.25MHz input clock.

- Added Figure 44 and Figure 45.

## Package Outline

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

**Microsemi Corporate Headquarters**
One Enterprise, Aliso Viejo,
CA 92656 USA

**Within the USA**: +1 (800) 713-4113
**Outside the USA**: +1 (949) 380-6100
**Sales**: +1 (949) 380-6136
**Fax**: +1 (949) 215-4996

**E-mail**: sales.support@microsemi.com

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