5 Marking

Table 2. Marking codes

Type number	Marking code
TEA1708T/1	TEA1708

6 Block diagram

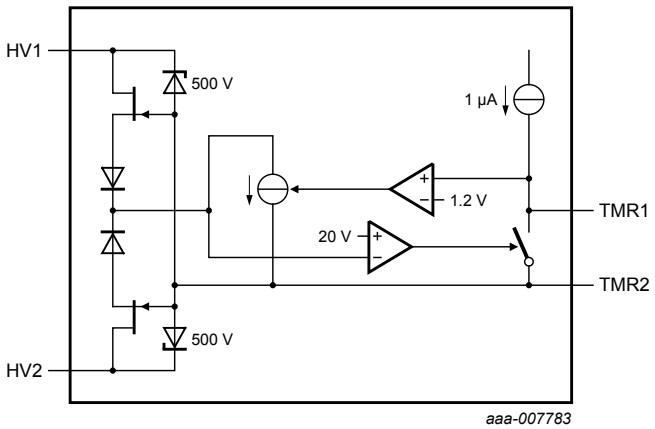


Figure 1. TEA1708 block diagram

7 Pinning information

7.1 Pinning

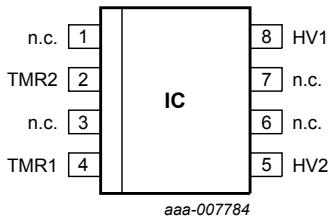


Figure 2. TEA1708 pinning diagram

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
n.c.	1	not connected
TMR2	2	timer pin 2
n.c.	3	not connected
TMR1	4	timer pin 1
HV2	5	high-voltage mains connection 2
n.c.	6	not connected
n.c.	7	not connected
HV1	8	high-voltage mains connection 1

8 Functional description

The TEA1708 incorporates a timer and a zero-crossing mains voltage detector. If a positive or negative voltage exceeding the threshold zero-crossing mains voltage (20 V) is applied between the high-voltage pins, the timer charges the external capacitor on the TMR1 and TMR2 pins. If the voltage between the TMR1 and TMR2 pins reaches 1.2 V, a discharge current is activated. If the voltage applied between the high-voltage pins, is below the threshold zero-crossing mains voltage, the external capacitor is discharged and the discharging stops. The discharge current is internally limited.

When an AC mains voltage is applied, the timer capacitor is charged between the mains zero crossings and discharged during the mains zero crossings. When the AC mains is disconnected and a high voltage remains on the X-capacitor, the timer charges the external capacitor above its discharge activation threshold voltage point (1.2 V), switching on the internally limited discharge current of the external X-capacitor.

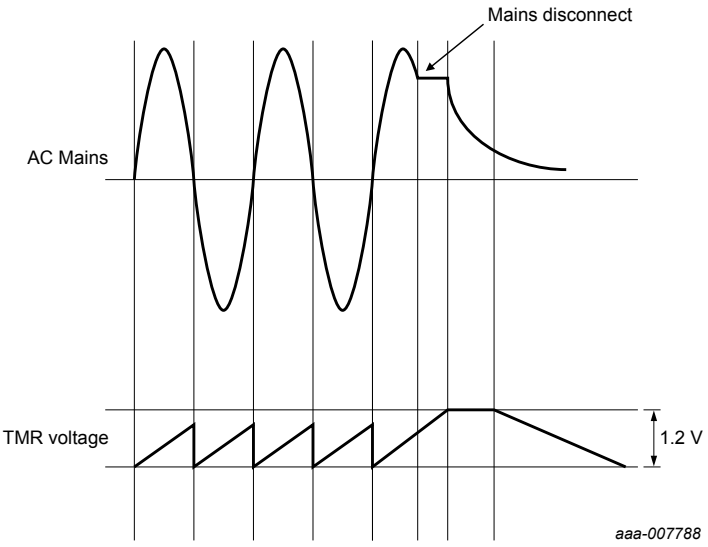


Figure 3. Functional behavior

To protect the IC during mains surges, a high-voltage clamping circuit is integrated. The clamping circuit is activated for positive and negative voltages > 500 V. The high-voltage pins HV1 and HV2 are fully symmetrical.

9 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Voltages						
$V_{TMR1-TMR2}$	voltage between pin TMR1 and pin TMR2	0 µA > $I_{dch(tmr)}$ < 10 µA		−0.4	+3.5	V
$V_{HV1-HV2}$	voltage between pin HV1 and pin HV2	normal operation, so no mains surge		−410	+410	V
Currents						
I_{HV}	current on pin HV	both HV pins; t < 2 ms, during mains surge		−15	+15	mA
General						
P_{tot}	total power dissipation	T_{amb} < 75 °C		-	0.5	W
T_{stg}	storage temperature			−55	+150	°C
T_j	junction temperature			−40	+150	°C
ESD						
V_{ESD}	electrostatic discharge voltage	class 1				
		human body model (HBM); pins HV1 and HV2	[1]	-	1000	V
		human body model(HBM); all other pins		-	4000	V
		charged device model (CDM); all pins	[2]	-	750	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
[2] Equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω resistor.

10 Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; JEDEC test board	160	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air; JEDEC test board	72	K/W

11 Characteristics

Table 6. Characteristics

T_{amb} = 25 °C; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High voltage (pins HV1 and HV2)						
I_{HV}	current on pin HV	both HV pins; V_{HV1} > 50 V; V_{HV2} > 50 V				
		V_{TMR} < 1.2 V	2.5	3.5	4.5	µA
		current limited; V_{TMR} > 1.2 V	1.8	2.3	2.8	mA
V_{clamp}	clamp voltage		475	500	525	V
$V_{th(ch)}$	charge threshold voltage	threshold zero-crossing mains voltage	19	21	23	V
Timer (pins TMR1 and TMR2)						
$V_{th(act)dch}$	discharge activation threshold voltage	to discharge the X-capacitor	1.1	1.2	1.3	V
$I_{dch(tmr)}$	timer discharge current		−1.20	−0.95	−0.70	µA

12 Application information

The TEA1708 is typically connected across the X-capacitor. A metal-oxide varistor is not required to protect the IC because the device incorporates a high-voltage clamping circuit. The IC is sufficiently protected for differential mode surge voltages up to 4 kV with only two 200 kΩ resistors (see Figure 4).

The discharge delay time is set externally using a low-voltage capacitor connected between the TMR1 and TMR2 pins. Select a value between 10 nF and 22 nF for a mains frequency of 50 Hz or 60 Hz. The minimum value is 10 nF which gives the smallest delay time. Do not use values < 10 nF. They can lead to unwanted discharge of the X-capacitor.

The delay time (t_d) for discharge can be calculated with Equation 1:

$$t_d = C_{tmr} \times \frac{V_{th(act)dch}}{I_{dch(tmr)}} \quad (1)$$

If the low-voltage capacitor value is 22 nF the delay time is:

$$22nF \times \frac{1.2V}{1\mu A} = 26ms$$

When the voltage across the device exceeds the threshold zero-crossing mains voltage, the discharge current is activated. The current is limited to ≅ 2.3 mA. When the current < the current limit, I_{HV} is calculated with Equation 2:

$$I_{HV1} = I_{HV2} \approx \frac{V_{xcap(t)} - (V_{th(ch)} + 4V)}{(R1+R2)} \quad (2)$$

When the X-capacitor value is 330 nF and R1 = R2 = 200 kΩ, the capacitor is discharged to a voltage < 60 V at a mains of 230 V (AC) in 300 ms.

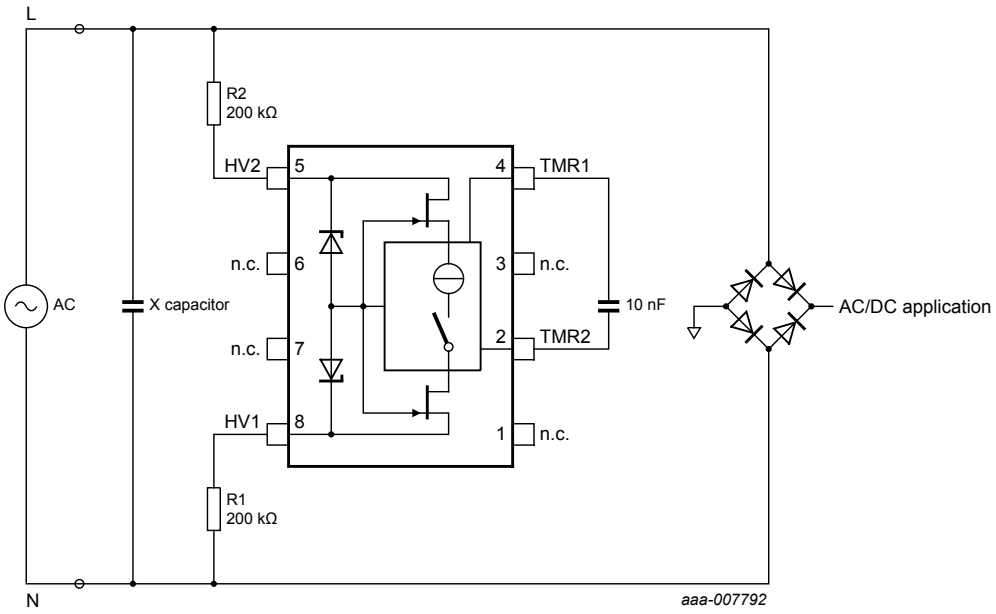
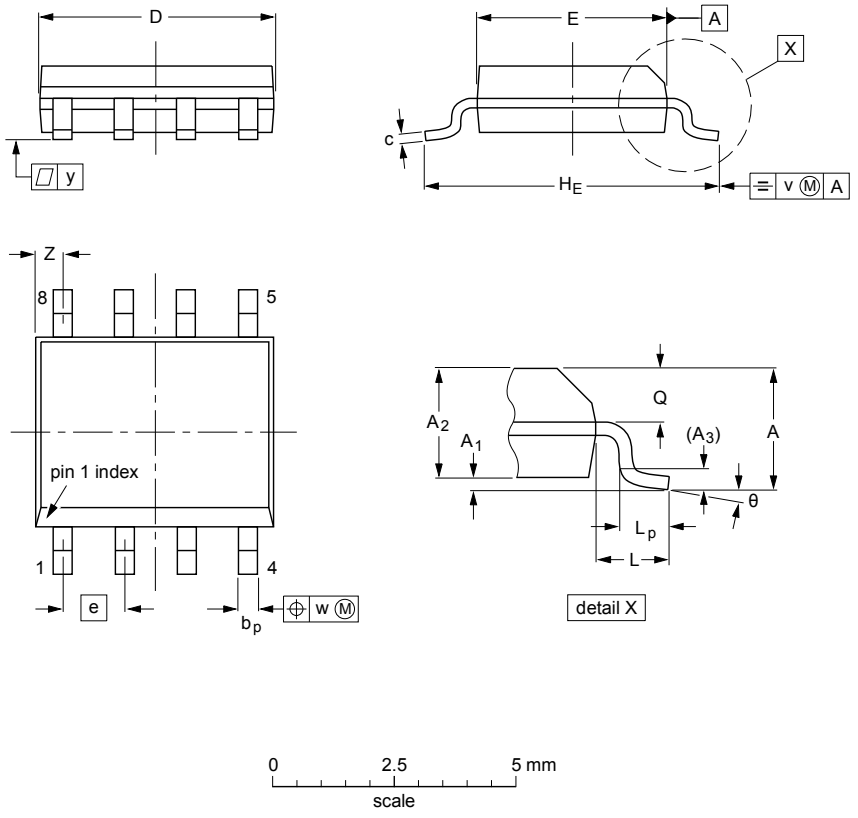


Figure 4. TEA1708 application diagram

To ensure that the capacitor is discharged to a voltage < 60 V within 2 seconds, use R1 = R2 = 200 kΩ for X-capacitor values < 1.8 µF. Lowering R1 + R2, for faster discharge or when a higher value for the X-capacitor is required, is possible but it decreases the surge protection level.

13 Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Figure 5. Package outline SOT96-1 (SO8)

14 Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1708T_1 v.1.1	20200406	Product data sheet	-	TEA1708T_1 v.1
TEA1708T_1 v.1	20130925	Product data sheet	-	-

15 Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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