

STSR3

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V _{CC}	DC Input Voltage		-0.3 to 6	V
V _{OUTGATE}	Max Gate Drive Output Voltage		-0.3 to V _{CC}	V
V _{INHIBIT}	Max INHIBIT Voltage (*)		-0.6 to V _{CC}	V
V _{CK}	Clock Input Voltage Range (*)		-0.3 to V _{CC}	V
P _{TOT}	Continuous Power Dissipation at T _A =105°C without heatsink		270	mW
ESD	Human Body Model	Pins 1,2, 4, 5, 6, 7, 8	±1	KV
		Pin 3	±0.9	KV
T _{stg}	Storage Temperature Range		-55 to +150	°C
T _{op}	Operating Junction Temperature Range		-40 to +125	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) A higher positive voltage level can be applied to the pin with a resistor which limits the current flowing into the pin to 10mA maximum

THERMAL DATA

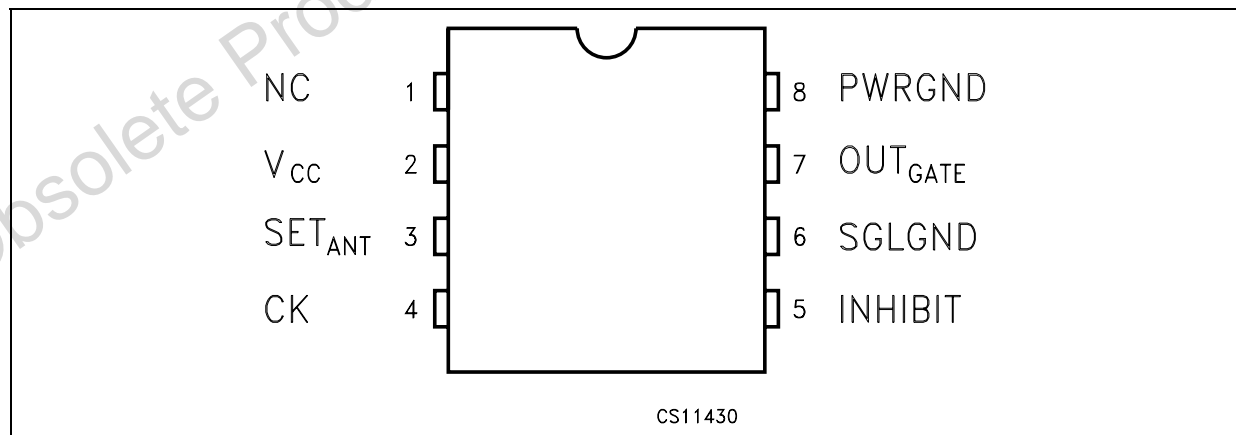
Symbol	Parameter	SO-8	Unit
R _{thj-amb}	Thermal Resistance Junction-case	40	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient (*)	160	°C/W

(*) This value is referred to one layer pcb board with minimum copper connections for the leads. a minimum value of 120 °C/W can be obtained improving thermal conductivity of the board

ORDERING CODES

TYPE	SO-8	SO-8 (T&R)
STSR3	STSR3CD	STSR3CD-TR

CONNECTION DIAGRAM (top view)



PIN DESCRIPTION

Pin N°	Symbol	Name and Function
1	NC	No internally connected
2	V_{CC}	The supply voltage range from 4.0V to 5.5V allows applications with logic gate threshold mosfets. UVLO feature guarantees proper start-up while it avoids undesirable driving during eventual dropping of the supply voltage.
3	SET_{ANT}	The voltage on this pin sets the anticipation (t_{ANT}) in turning off the OUT_{GATE} . It is possible to choose among three different anticipation times by discrete partitioning of the supply voltage.
4	CK	This input provides synchronization for IC's operations, being the transitions between the two output conditions based on a positive threshold, equal for the two slopes. A smart internal control logic mechanism using a 15MHz internal oscillator generates proper anticipation timing at the turn-off of each output. This feature allows safe turn-off of Synchronous Rectifier avoiding any eventual shoot-through situation on secondary side at both transitions. Smart clock revelation mechanism makes these operations independent by false triggering pulses generated in light load conditions. Absolute maximum voltage rating of the pin can be exceeded limiting the current flowing into the pin to 10mA max.
5	INHIBIT	This input enables OUT_{GATE} to work when its voltage is lower than the negative threshold voltage ($V_{INHIBIT} < V_H$). If $V_{INHIBIT} > V_H$ the OUT_{GATE} will be high for a minimum conduction time ($t_{ON(GATE)}$). In typical flyback converter application, it is possible to turn off the synchronous MOSFET when the current through it tends to reverse, allowing discontinuous conduction mode and providing protection to the converter from eventual sinking current from the load. Absolute maximum voltage rating of the pin can be exceeded limiting the current flowing into the pin to 10mA max.
6	SGLGND	Reference for all the control logic signals. This pin is completely separated from the PWRGND to prevent eventual disturbances to affect the control logic.
7	OUT_{GATE}	Gate Drive signal for synchronous MOSFET. Anticipation [t_{ANT}] in turning off OUT_{GATE} is provided during the transition in which the clock input goes to high level.
8	PWRGND	Reference for power signals, this pin carries the full peak currents for the two outputs.

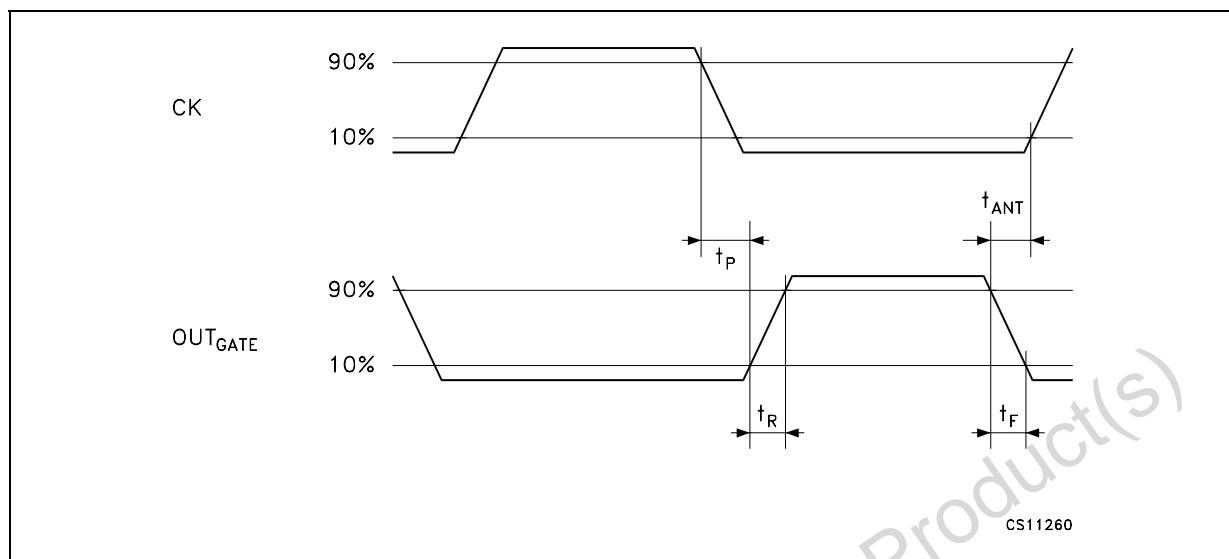
ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $CK=250kHz$, duty-cycle=50%, $V_{INHIBIT}=-200mV$, $T_J=-40$ to $125^{\circ}C$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY INPUT AND UNDER VOLTAGE LOCK OUT						
V _{CCON}	Start Threshold			3.8	4	V
V _{CCOFF}	Turn OFF Threshold After Start		3.5	3.6		V
V _Z	Zener Voltage	CK=0V I _Z = 2mA	5.5	5.8	6	V
I _{CC}	Unloaded Supply Current	OUT _{GATE} = no load		15	20	mA
		CK=0V OUT _{GATE} = no load		3	5	
GATE DRIVER OUTPUTS						
V _{OL}	Output Low Voltage	I _{OUTGATE} = -200mA		0.10	0.16	V
V _{OH}	Output High Voltage	I _{OUTGATE} =200mA	4.70	4.85		V
I _{OUT}	Output Source Peak Current			2		A
	Output Sink Peak Current			3.5		
R _{OUT}	Output Series Source Resistance	I _{OUTGATE} = -200mA		0.75	1.5	Ω
	Output Series Sink Resistance	I _{OUTGATE} =200mA		0.5	0.8	
t _R	OUT _{GATE} Rise Time	C _{LOAD} =5nF (Note 1)		40		ns
t _F	OUT _{GATE} Fall Time	C _{LOAD} =5nF (Note 1)		30		ns
t _p	Clock Propagation Delay to Turn ON of OUT _{GATE}	No Load		50		ns
TURN-OFF ANTICIPATION TIME						
t _{ANT}	OUT _{GATE} Turn-off Anticipation Time	V _{ANT} = 0 to 1/3V _{CC} ; no load		75		ns
		V _{ANT} = 1/3V _{CC} to 2/3V _{CC} ; no load		150		
		V _{ANT} = 2/3V _{CC} to V _{CC} ; no load		225		
I _{SETANT}	Leakage Current (Note 2)		-0.1		0.1	μA
INHIBIT OUT _{GATE} ENABLE						
V _H	Threshold Voltage	T _J = 25°C	-30	-25		mV
I _H	Leakage Current (Note 2)	V _{INHIBIT} = 200mV		-400		nA
		V _{INHIBIT} = -200mV			1	μA
t _{ON(GATE)}	Minimum OUT _{GATE} On time	V _{INHIBIT} = +200mV		250		ns
SYNCHRONIZATION INPUT						
V _{CK}	Reference Voltage	T _J = 25°C		2.6	2.8	V
D _{OFF}	Duty Cycle Shut Down	T _J = 25°C	13	14		%
	Duty Cycle Turn ON after Shut Down	T _J = 25°C		18	20	

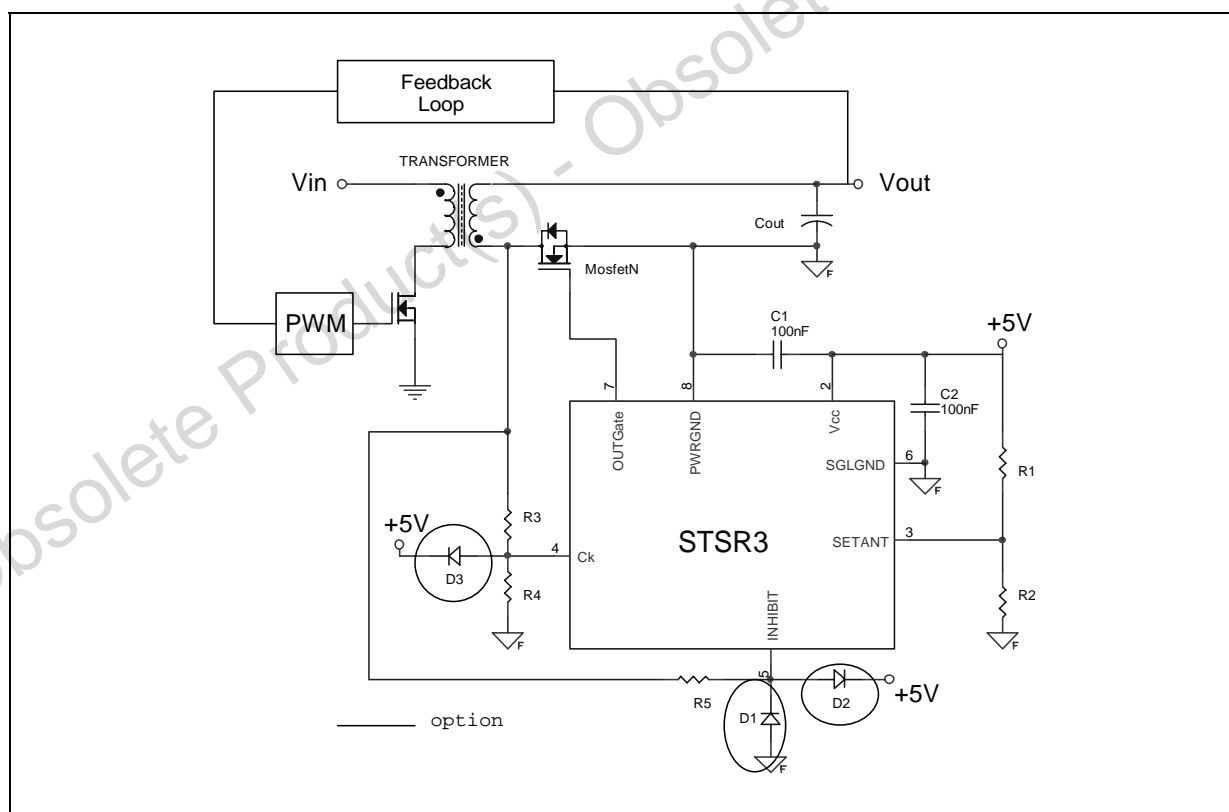
Note1: t_R is measured between 10% and 90% of the final voltage; t_F is measured between 90% and 10% on the initial voltage

Note2: Parameter guaranteed by design

TIMING DIAGRAM



APPLICATION INFORMATION: STSR3 IN FLYBACK CONVERTER SECONDARY SIDE



NOTES

- 1) Ceramic Capacitors C₁ and C₂ must be placed very close to the IC;
- 2) R₁ and R₂ set the anticipation time by partitioning the V_{CC} voltage;
- 3) R₃ and R₄ is a resistor divider meant to provide the correct CK voltage range;
- 4) R₅ limits the current flowing through diode D₂ when Freewheeling drain voltage is high;
- 5) D₁ could be necessary to protect INHIBIT pin from negative voltages.
- 6) D₂ could be necessary to protect INHIBIT pin from voltages higher than V_{CC}.
- 7) D₃ could be necessary to protect CK pin from voltages higher than V_{CC}.
- 8) SGLGND layout trace must not include OUT_{GATE} current paths.
- 9) A capacitor in parallel with R₄ could be necessary to eliminate turn off voltage spike.



EXAMPLE OF COMPONENTS SELECTION FOR A FLYBACK CONVERTER

Flyback Specification:

$$V_{IN}=36-72V$$

$$V_{OUT}=3.3V$$

$$n=N_p/N_s=4.5$$

R_3 and R_4 are calculated assuring a minimum voltage of 2.8V at Ck pin. At 36V input, the voltage on the secondary winding is $36/4.5=8V$. Choosing $R_3=1.5k\Omega$, R_4 results to be:

$$R_4 \geq \frac{V_{CK} \times R_3}{V_{IN} - I_{CK(2.8)} \times R_3 - V_{CK}} = 1k\Omega \times \frac{2.8V \times 1.5k\Omega}{8V - 220\mu A \times 1.5k\Omega - 2.8V} = 862\Omega$$

$R_4=1k\Omega$ is chosen. At 72V input the current at Ck pin is calculated as:

$$I_{CK} = \frac{V_{IN(max)} - V_{CC} - 0.3}{R_3} = \frac{16 - 5 - 0.3}{1.5k\Omega} = 7.13mA$$

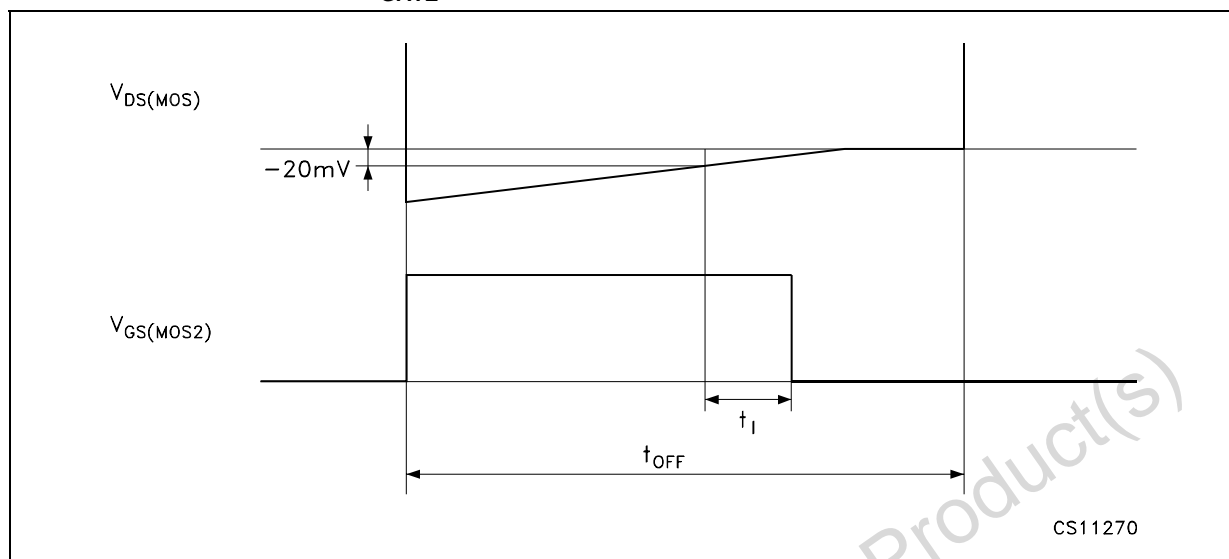
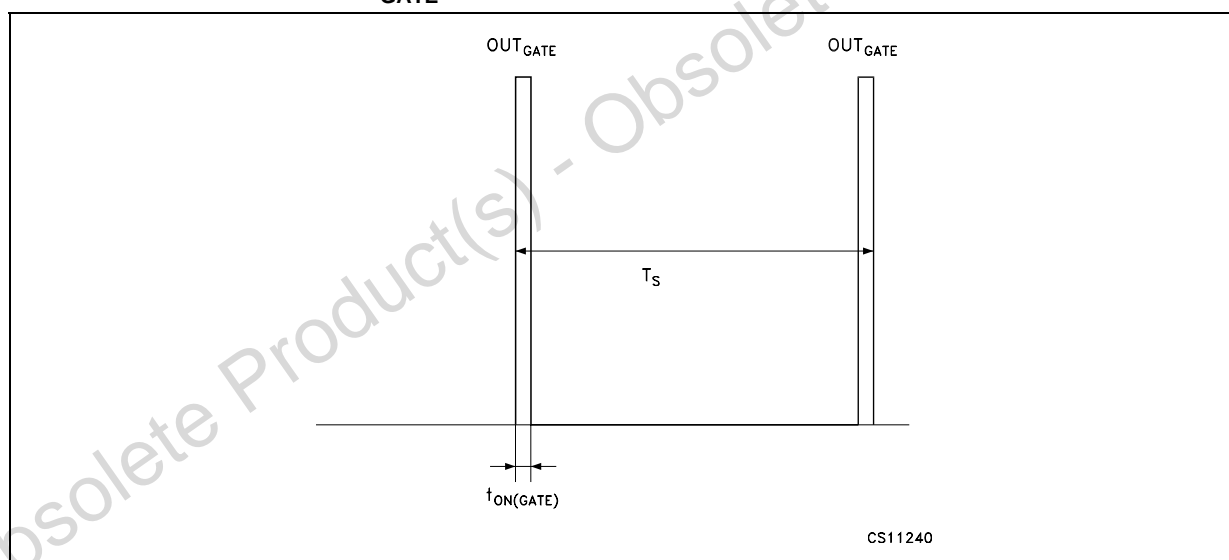
This value is below the maximum allowable current flowing into the Ck pin (10mA). If the 10mA value is exceeded an external diode connected to V_{CC} must be added (D3).

R_1 and R_2 values set the anticipation time for OUT_{GATE} . For $R_1=\infty$ and $R_2=0$, $t_{ANT}=75ns$; for $R_1=R_2=10k\Omega$, $t_{ANT}=150ns$; for $R_1=0$ and $R_2=\infty$, $t_{ANT}=225ns$.

The RC group composed by R_5 and the parasitic capacitance of Inhibit pin (typically 5pF) delays the signal on Inhibit comparator. This delay must be lower than 200ns. This condition imposes a maximum value for R_5 of about 20k Ω .

In general a suggested value for R_5 is 10k Ω . At 72V input, the secondary voltage is 16V, so the maximum current flowing into Inhibit pin is $16V/10k\Omega=1.6mA$ which is below the maximum allowable current for the pin (10mA). If the 10mA value is exceeded an external diode (D2) connected to V_{CC} must be added.

The maximum negative voltage of -0.6V must be guaranteed for the Inhibit pin. If this negative voltage is exceeded the current must be limited to 50mA. If necessary, a diode (D1) connected to SGLGND can be added to satisfy this specification.

INHIBIT OPERATION OF OUT_{GATE} IN DISCONTINUOUS CONDUCTION MODEINHIBIT OPERATION OF OUT_{GATE} 

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified $T_J = 25^\circ\text{C}$)

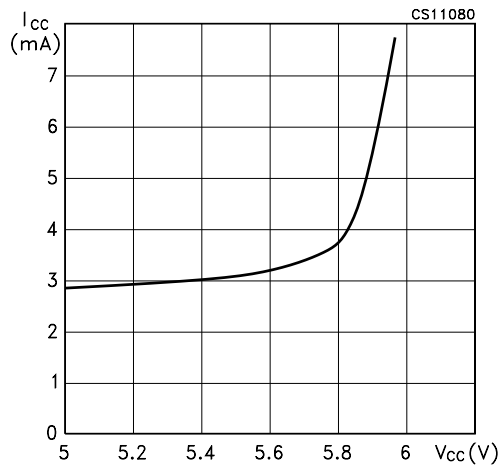
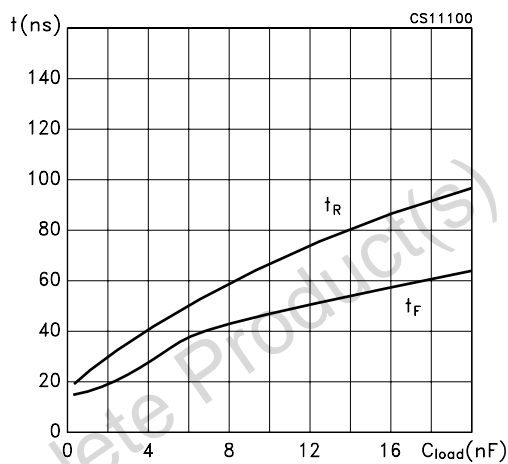
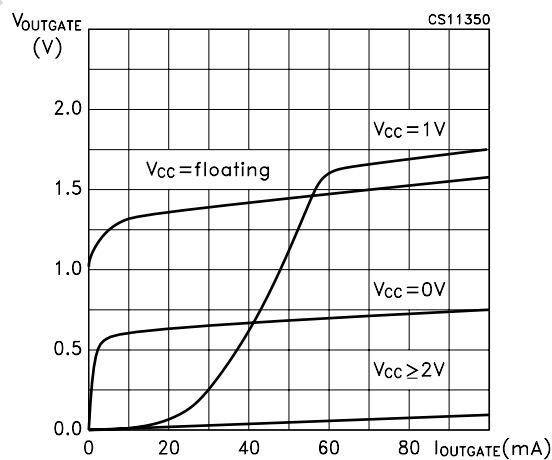
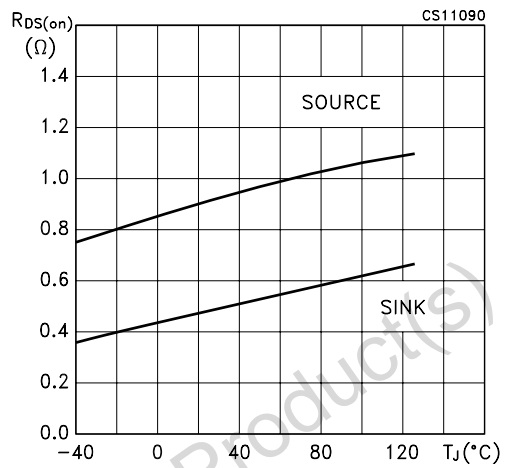
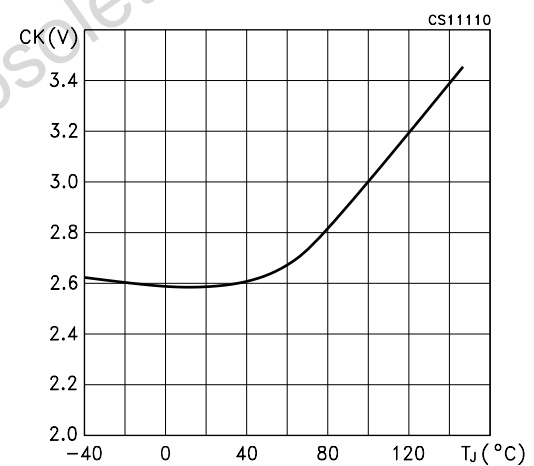
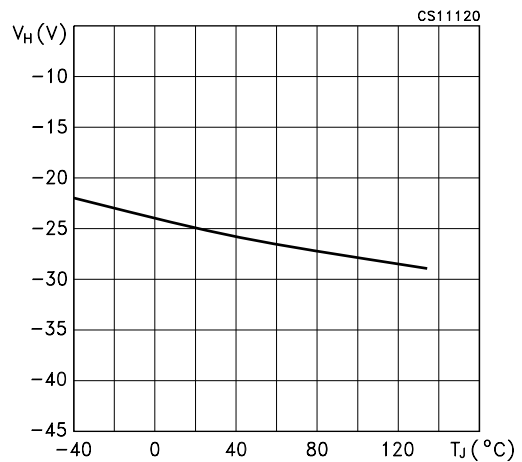
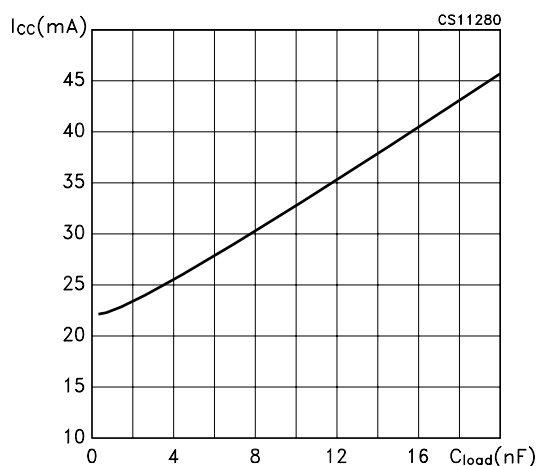
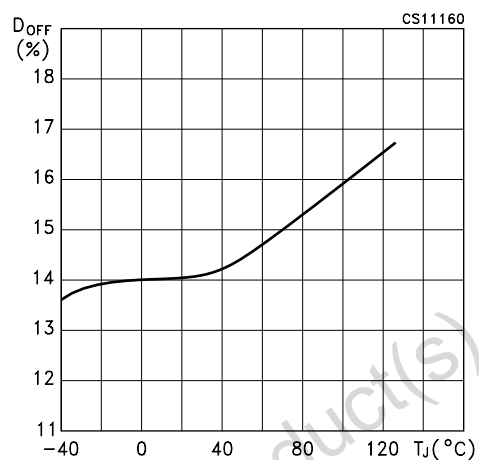
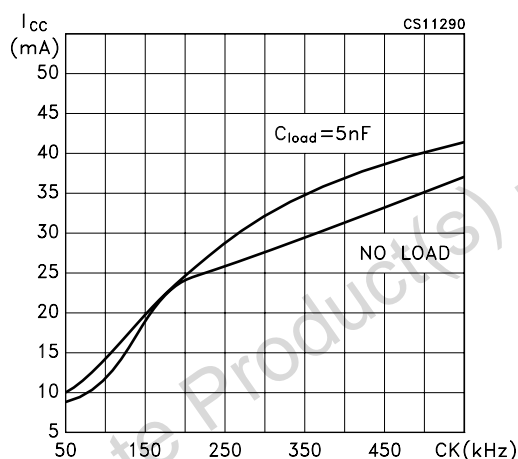
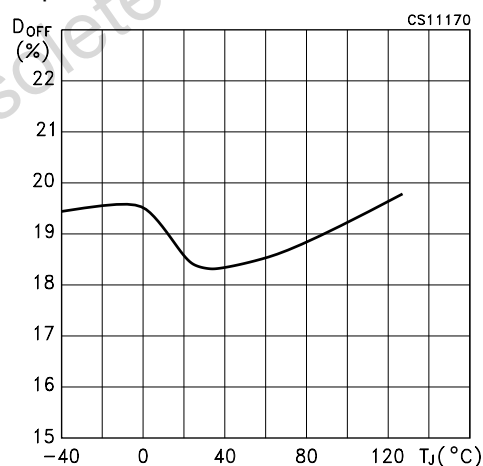
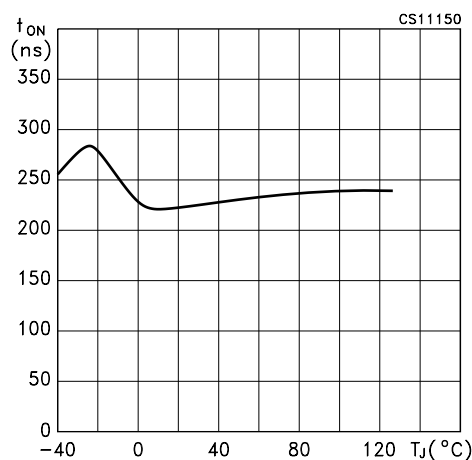
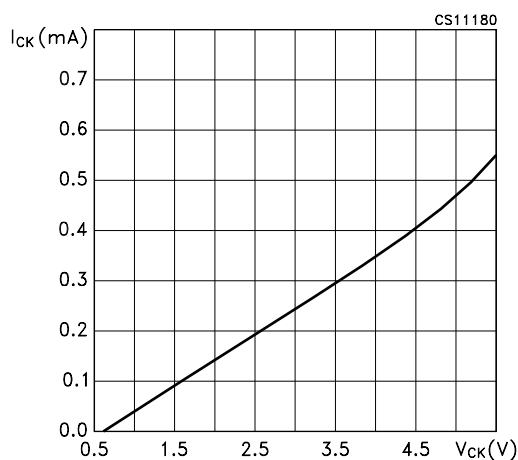
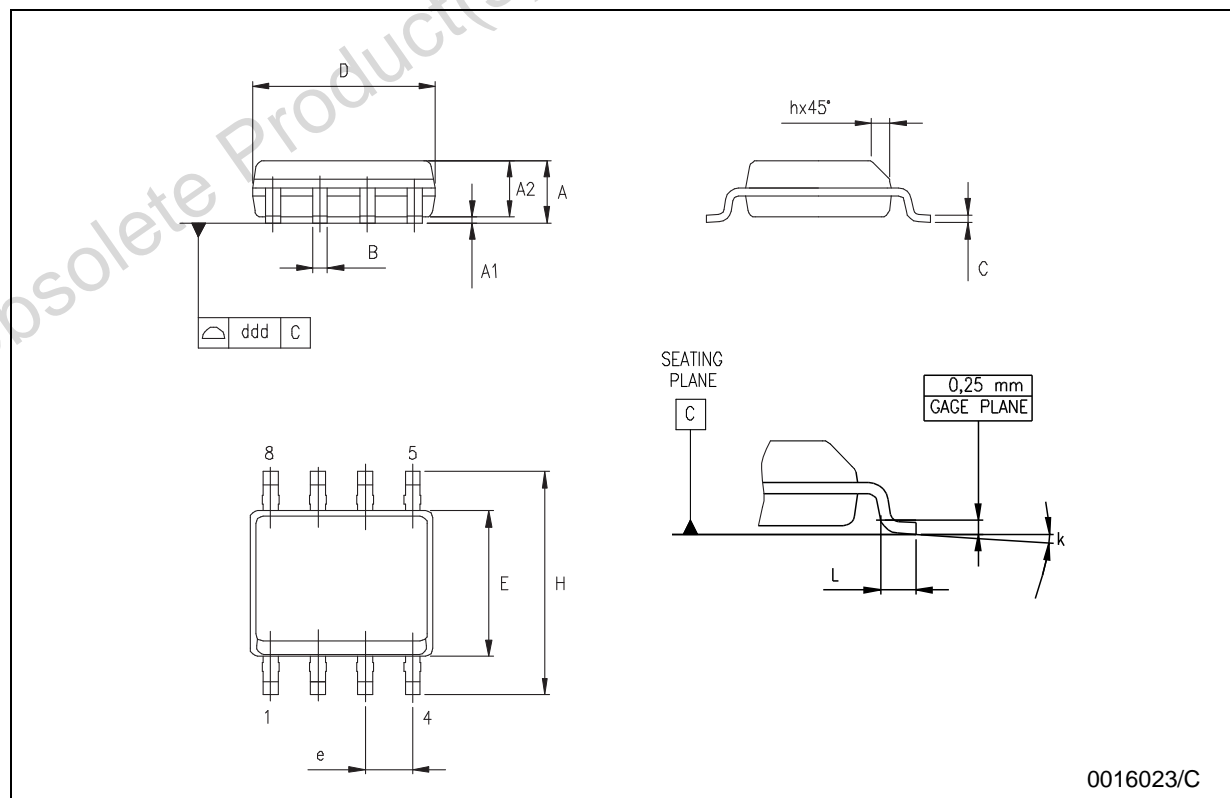
Figure 1 : Zener Characteristics

Figure 2 : Rise and Fall Time vs Load Capacitor

Figure 3 : OUT_{GATE} vs Characteristics

Figure 4 : Sink-Source ON Resistance vs Temperature

Figure 5 : Clock Threshold Voltage vs Temperature

Figure 6 : INHIBIT Threshold Voltage vs Temperature


Figure 7 : Supply Current vs Load Capacitor**Figure 10 : Duty Cycle Shut Down vs Temperature****Figure 8 : Supply Current vs Clock Frequency****Figure 11 : Duty Cycle Turn ON After Shut Down vs Temperature****Figure 9 : GATE ON Time vs Temperature****Figure 12 : Clock Leakage Current vs Clock Voltage**

SO-8 MECHANICAL DATA

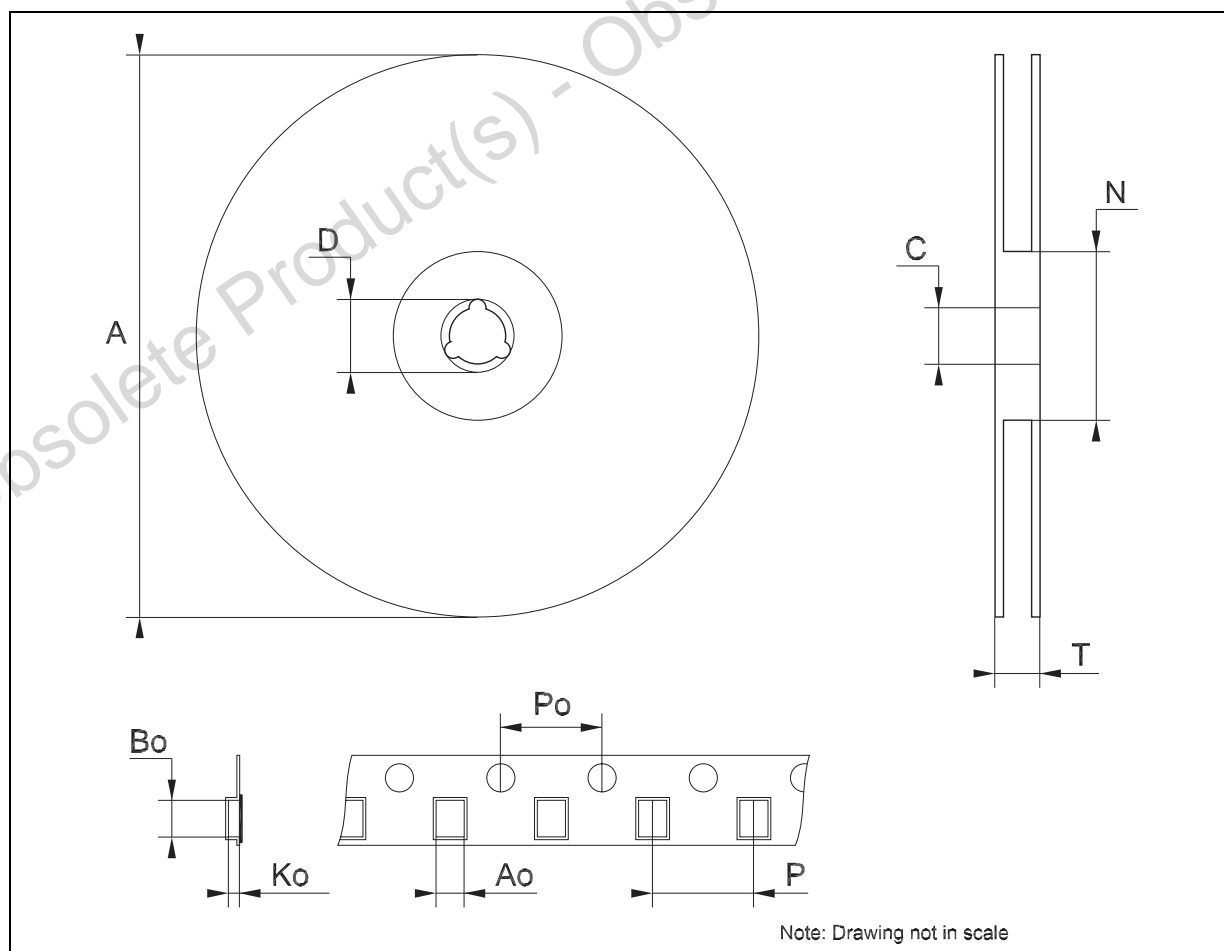
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



0016023/C

Tape & Reel SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



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