Table 1. Electrical Characteristics (continuous)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time[3]	T_r, T_f	–	4	8	ns	Vdd = 1.8 V, 20% - 80%. Contact SiTime for other programmable rise/fall options
		–	–	8	ns	Vdd = 2.25 V to 3.63 V, 20% - 80%. Contact SiTime for other programmable rise/fall options
Output High Voltage	VOH	90%	–	–	VDD	IOH = -0.5 mA (Vdd = 1.8 V) IOH = -1.2 mA (Vdd = 2.25 V to 3.63 V)
Output Low Voltage	VOL	–	–	10%	VDD	IOL = 0.5 mA (Vdd = 1.8 V) IOL = 1.2 mA (Vdd = 2.25 V to 3.63 V)
Input Characteristics						
Input High Voltage	VIH	80%	–	–	VDD	
Input Low Voltage	VIL	–	–	20%	VDD	
Input Slew Rate	In-slew	10	–	–	V/µs	
Input Pull-down Impedance	Z_in	300	–	–	kΩ	Active mode (ST pin = LOW), Vdd = 1.8 V
		270	–	–	kΩ	Active mode (ST pin = LOW), Vdd = 2.25 V to 3.63 V
		2.5	–	–	MΩ	Standby mode (ST pin = HIGH), Vdd = 1.8 V
		1.3	–	–	MΩ	Standby mode (ST pin = HIGH), Vdd = 2.25 V to 3.63 V
Startup, Standby and Resume Timing						
Startup Time	T_start	–	75	150	ms	Measured from the time VDD reaches 90% of its final value
Standby Time	T_stdby	–	–	20	µs	Measured from the time ST pin crosses 50% threshold
Resume Time	T_resume	–	2	3	ms	Measured from the time ST pin crosses 50% threshold
Jitter						
RMS Period Jitter[3]	T_jitt	–	75	110	ps	f = 6.144 MHz, Vdd = 1.8 V
		–	–	110	ps	f = 6.144 MHz, Vdd = 2.25 V to 3.63 V
RMS Phase Jitter[3]	T_phj	–	0.8	2.5	ns	f = 6.144 MHz, Vdd = 1.8 V, Integration bandwidth = 100 Hz to 40 kHz[2]
		–	–	2.5	ns	f = 6.144 MHz, Vdd = 2.25 V to 3.63 V, Integration bandwidth = 100 Hz to 40 kHz[2]

Notes:

1. Current consumption with load is a function of the output frequency and output load. For any given output frequency, the capacitive loading will increase current consumption equal to C_load*VDD*f(MHz).
2. Max spec inclusive of 25 mV peak-to-peak sinusoidal noise on VDD. Noise frequency 100 Hz to 20 MHz.
3. Refer to the performance plot section for typical values at 2.5, 2.8, 3.0 and 3.3 V condition

Table 2. Pin Description

Pin	Symbol	Functionality	
1	ST	Input	L: Specified frequency output H: Output is low (weak pull down). Device goes to the standby mode. Supply current reduces to I_std.
2	OUT	Output	LVCMOS clock output
3	VDD	Power	Supply voltage. Bypass with a 0.01 µF X7R capacitor.
4	GND	Power	Connect to ground

Top View

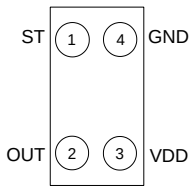


Figure 1. Pin Assignments

Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Condition	Value	Unit
Continuous Power Supply Voltage Range (VDD)		-0.5 to 3.63	V
Short Duration Maximum Power Supply Voltage (VDD)	<30 seconds	4.0	V
Continuous Maximum Operating Temperature		105	°C
Short Duration Maximum Operating Temperature	≤30 seconds	125	°C
Human Body Model (HBM) ESD Protection	JESD22-A115	2000	V
Charge-Device Model (CDM) ESD Protection	JESD22-C101	750	V
Machine Model (MM) ESD Protection	T_A = 25°C	200	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	MII 883, Method 2002	10,000	*g*
Mechanical Vibration Resistance	MII 883, Method 2007	70	*g*
1508 CSP Junction Temperature		150	°C
Storage Temperature		-65 to 150	°C
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C

Block Diagram

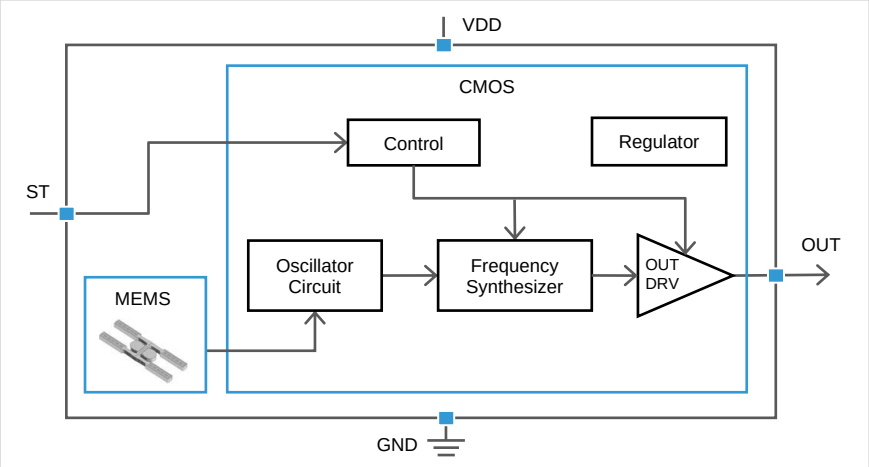


Figure 2. SiT8021 Block Diagram

Device Operating Modes and Outputs

The SiT8021 supports a ≤0.7 µA standby mode for battery-powered and other power sensitive applications. The switching between the active and standby modes is controlled by the logic level on the ST pin as shown in the table below.

Table 4. Operating Modes and Output States

ST Pin	MODE	OUTPUT	IDD Example
LOW	Active	Specified frequency	60 µA @ 3.072 MHz
FLOAT	Active with 200 kΩ internal pull-down	Specified frequency	60 µA @ 3.072 MHz
HIGH	Standby	Hi-Z, pulled-down with 1 MΩ impedence	1.3 µA

Active Mode

The SiT8021 operates in the active mode when the ST pin is at logic LOW or FLOAT. In the active mode, the device uses the on-chip frequency synthesizer to generate an output from the internal MEMS resonator reference. The frequency of the output is factory programmed based on the device ordering code.

Standby Mode

The SiT8021 operates in the standby mode when the ST pin is at logic HIGH. In the standby mode, all internal circuits with the exception of the MEMS oscillator circuit and the ST pin detection logic are turned off to reduce power consumption. While in standby mode, the input impedance of the ST pin is increased to further reduce system-level power consumption.

The output driver of the device in the standby mode is pulled-down with 1 MΩ impedance.

Output During Startup and Resume

The SiT8021 starts up with the output disabled. The output is enabled once all internal circuit blocks are active, and logic LOW or FLOAT is detected on the ST pin.

As shown in Table 4, logic HIGH at the ST pin forces the SiT8021 into the “standby” state, causing the output to disable. Upon pulling the ST pin LOW, the device enters the “resume” state, keeping the output disabled. Once the “resume” state ends, the device output enables.

The first clock pulse after startup or resume is accurate to the rated stability.

Low Power Design Guidelines

For high EM noise environments, we recommend the following design guidelines:

- Place oscillator as far away from EM noise sources as possible (e.g., high-voltage switching regulators, motor drive control).
- Route noisy PCB traces, such as digital data lines or high di/dt power supply lines, away from the SiTime oscillator.
- Place a solid GND plane underneath the SiTime oscillator to shield the oscillator from noisy traces on the other board layers.

Manufacturing Guidelines

- No Ultrasonic or Megasonic Cleaning: Do not subject the SiT8021 to an ultrasonic or megasonic cleaning environment. Permanent damage or long-term reliability issues to the device may occur in such an event.
- Applying board-level underfill (BLUF) to the device is acceptable, but will cause a slight shift of few ppm in the initial frequency tolerance. Tested with UF3810, UF3808, and FP4530 underfill.
- Reflow profile, per JESD22-A113D.

  For additional manufacturing guidelines and marking/tape-reel instructions, refer to SiTime Manufacturing Notes.

Test Circuit and Waveform

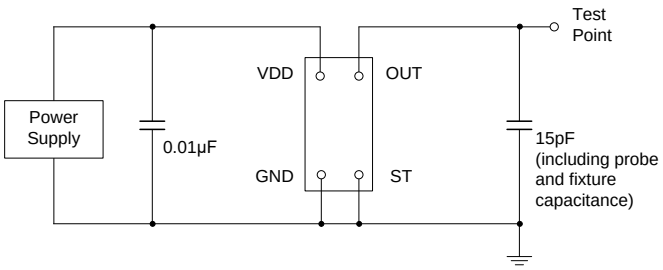


Figure 3. Test Circuit

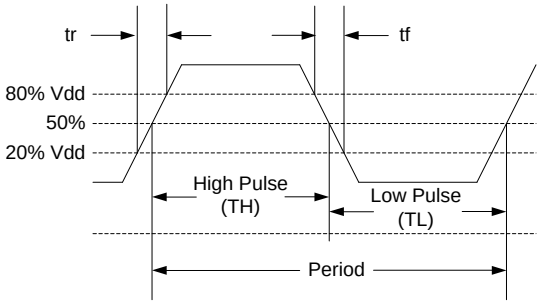
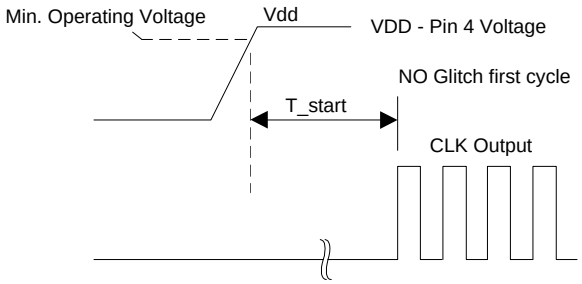


Figure 4. Waveform[4]

Note:

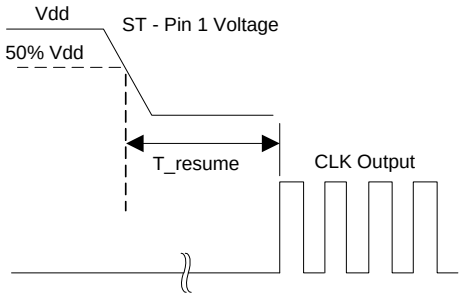
4. Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagram



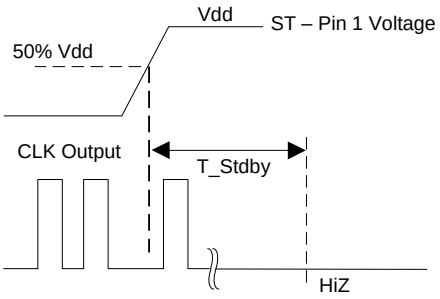
T_start: Time to valid clock output from power on

Figure 5. Startup Timing[5,6]



T_resume: Time to valid clock output from the time ST pin crosses 50% threshold

Figure 6. Resume Timing[5,6]



T_Stdby: Time for output to go high-Z from the time ST pin crosses 50% threshold

Figure 7. Standby Timing[5]

Notes:

5. SiT8021 supports “no runt” pulses and “no glitch” output during startup or resume.
6. SiT8021 supports gated output which is accurate within rated frequency stability from the first cycle.

Performance Plots[7]

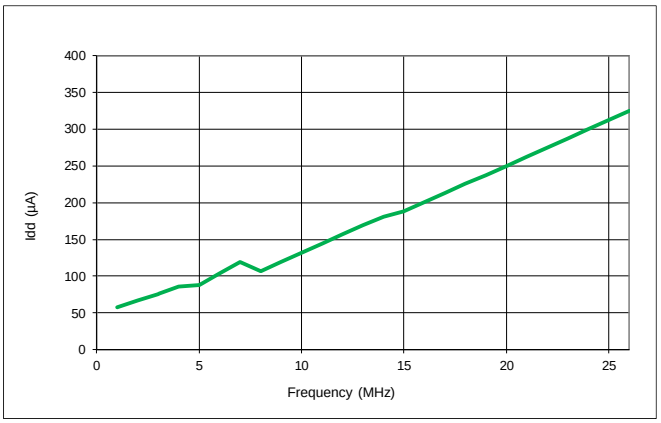


Figure 8. Idd vs Frequency without load

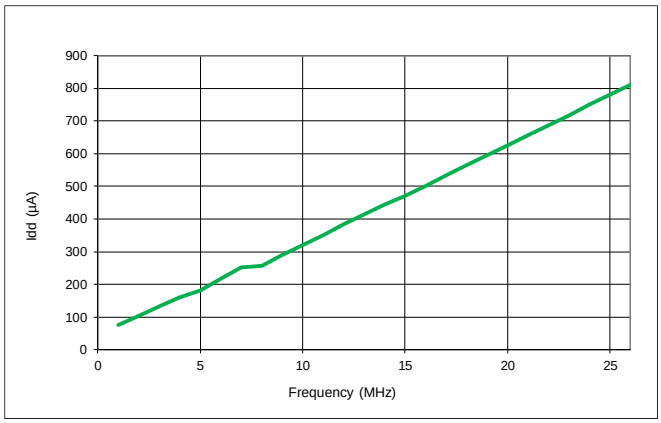


Figure 9. Idd vs Frequency with 10 pF load

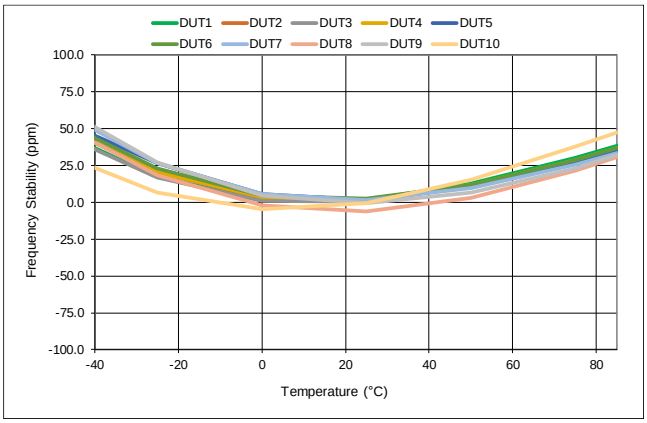


Figure 10. Frequency vs Temperature

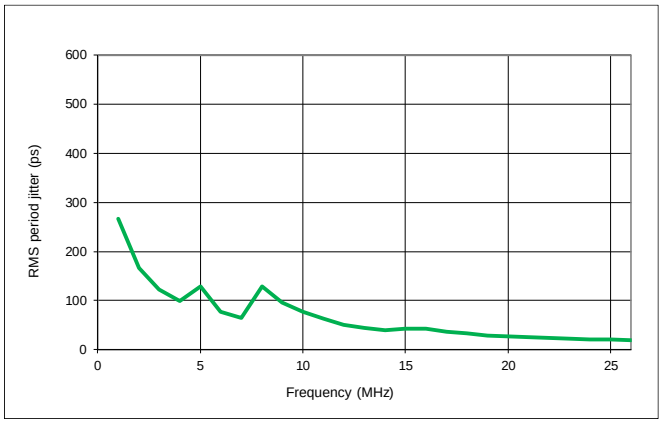


Figure 11. RMS Period Jitter vs Frequency

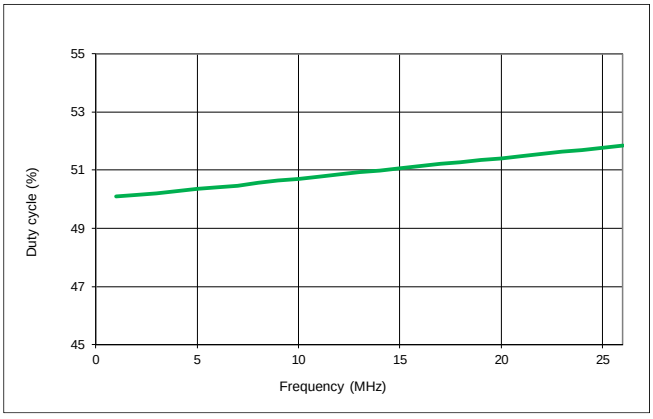


Figure 12. Duty Cycle vs Frequency

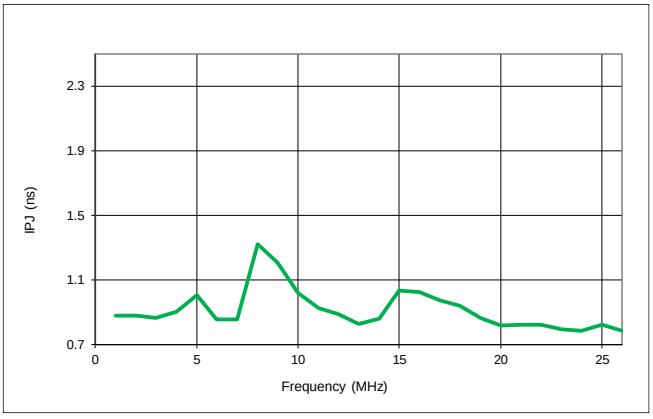


Figure 13. RMS Phase Jitter Random vs Frequency[8]

Performance Plots[7] (continuous)

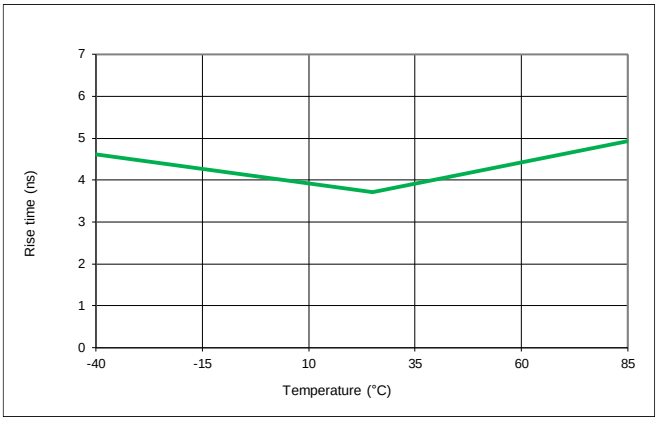


Figure 14. Rise Time vs Temperature[9]

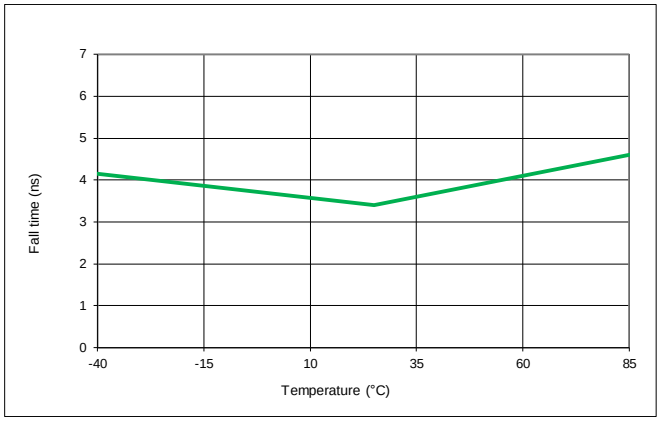


Figure 15. Fall Time vs Temperature[9]

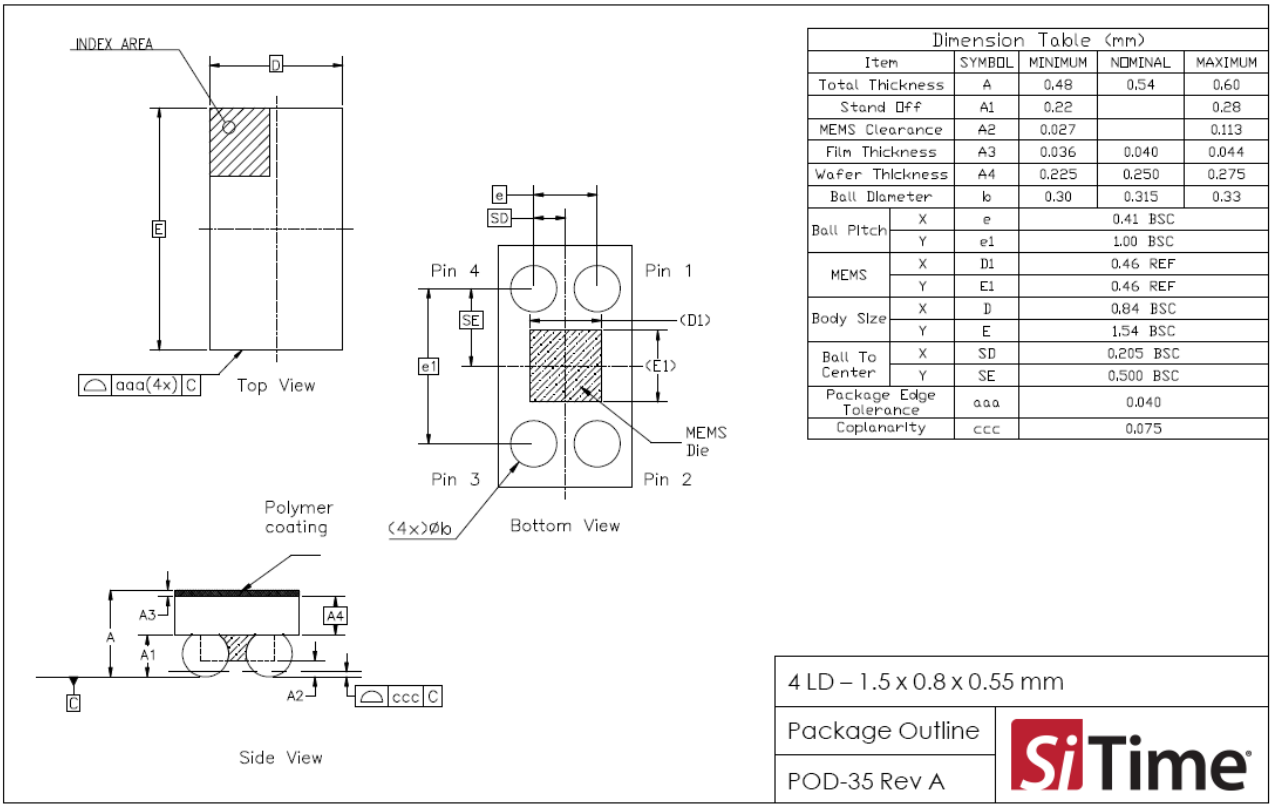
Notes:

7. All data is measured at room temperature, unless otherwise stated.
8. Integration range is from 100 Hz to 40 kHz.
9. Data is measured with 15 pF load.

Dimensions and Patterns

1.5 x 0.8 x 0.54 mm

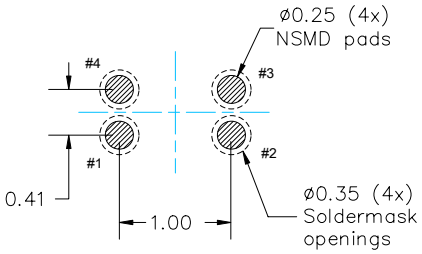
Package Size – Dimensions (Unit: mm)



Dimension Table (mm)

Item		SYMBOL	MINIMUM	NOMINAL	MAXIMUM
Total Thickness		A	0.48	0.54	0.60
Stand Off		A1	0.22		0.28
MEMS Clearance		A2	0.027		0.113
Film Thickness		A3	0.036	0.040	0.044
Wafer Thickness		A4	0.225	0.250	0.275
Ball Diameter		b	0.30	0.315	0.33
Ball Pitch	X	e	0.41 BSC		
	Y	e1	1.00 BSC		
MEMS	X	D1	0.46 REF		
	Y	E1	0.46 REF		
Body Size	X	D	0.84 BSC		
	Y	E	1.54 BSC		
Ball To Center	X	SD	0.205 BSC		
	Y	SE	0.500 BSC		
Package Edge Tolerance		aaa	0.040		
Coplanarity		ccc	0.075		

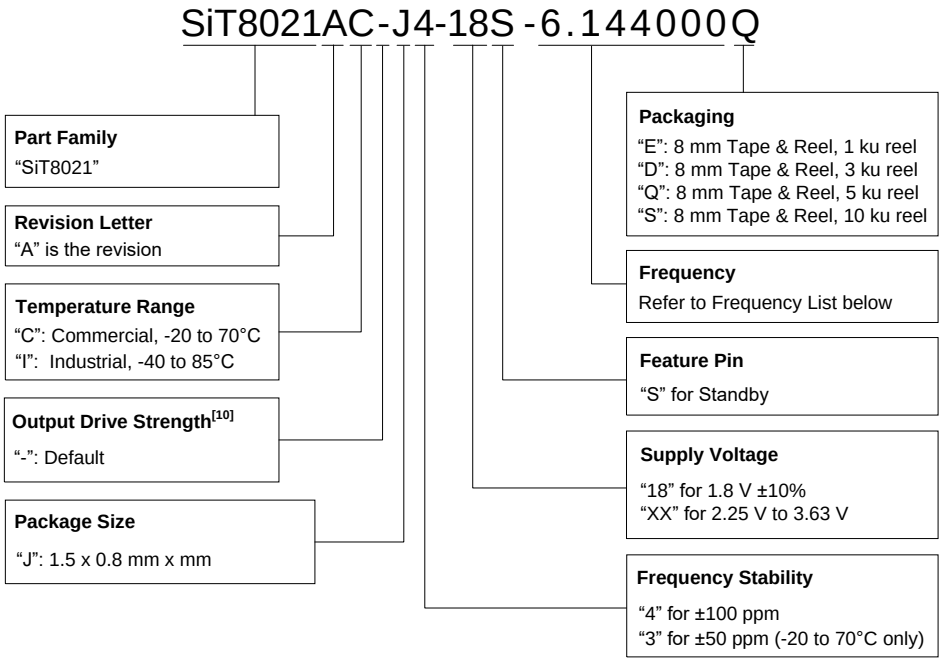
Recommended Land Pattern (Unit: mm)



(soldermask openings shown with dashed line around NSMD pad)

Recommended 4-mil (0.1mm) stencil thickness

Ordering Information



Notes:

10. Contact SiTime for other drive strength options that result in different rise/fall time for any given output load.

Table 5. List of Standard Frequencies[11]

2.048 MHz	4 MHz	6.144 MHz	8 MHz	12 MHz	12.288 MHz	16 MHz
19.2 MHz	24 MHz	26 MHz				

Notes:

11. All frequencies from 1 to 26 MHz are in production. Contact SiTime for minimum order quantity requirement.

Table 6. Revision History

Version	Release Date	Change Summary
0.1	15-Dec-2014	Advance Information
0.2	27-Jan-2015	Updated CSP dimension tolerance Removed 2.0 mm x 1.6 mm package Changed to 6.144 MHz as the reference frequency for jitter, IDD and other relevant parameters Changed resume time (max) to 5 ms Changed the parameter PSNR to Power Supply Noise Sensitivity and specified in RMS
0.3	31-Mar-2015	Changed VIL and VIH values in the EC table Reduced standby time in the EC table Revised phase jitter condition to include power supply noise sensitivity Removed power supply noise spec
0.9	22-May-2015	Added typical values for active and standby current Added current consumption for additional frequencies Changed ±50 ppm option to Contact SiTime Added manufacturing guideline Other miscellaneous format and footnote changes
1.0	18-Nov-2015	Revised initial tolerance, current consumption, standby current, input high/low voltage, input pull-down impedance, startup/resume time and RMS period/phase jitter in Table 1 Added performance plots
1.1	19-Feb-2016	Added 10 Standard frequencies to the ordering information
1.11	16-Sep-2016	Updated the table.5 list of standard frequencies Added a graph of Idd vs Frequency without load to the performance plots section
1.2	28-Sep-2017	Added 2.25 to 3.63 V supply voltage option Updated logo and company address, other page layout changes Added package dimension table to the dimensions and patterns section
1.3	18-Nov-2020	Added ±50 ppm frequency stability option Formatting, rev table date format and TempFlat MEMS logo update
1.31	29-Mar-2021	Added Q-suffix to the Ordering table options Updated hyperlinks, changed date format

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