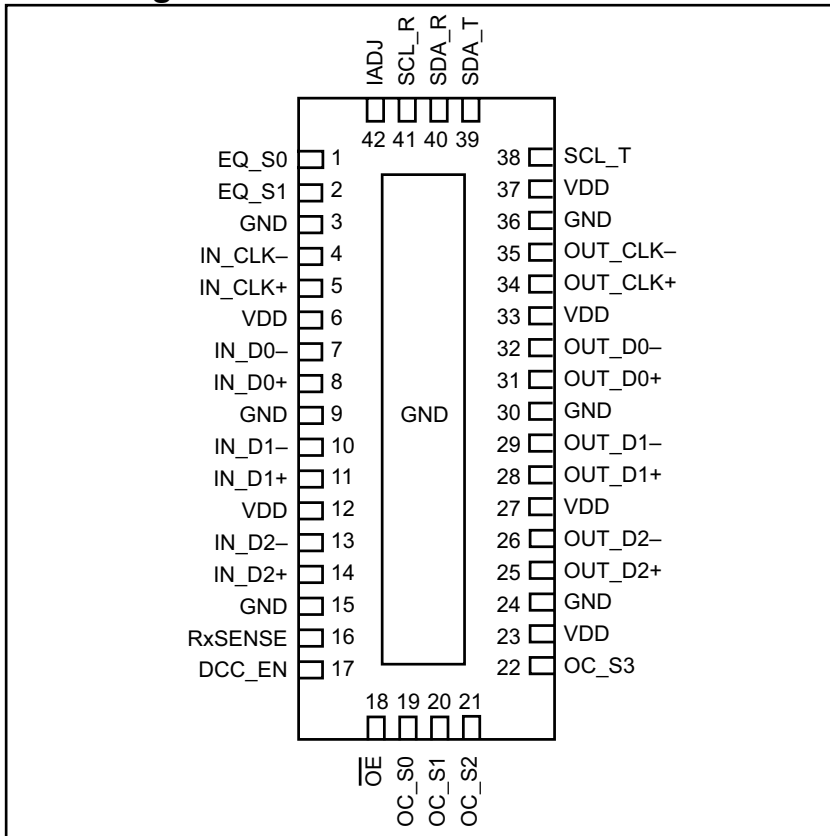
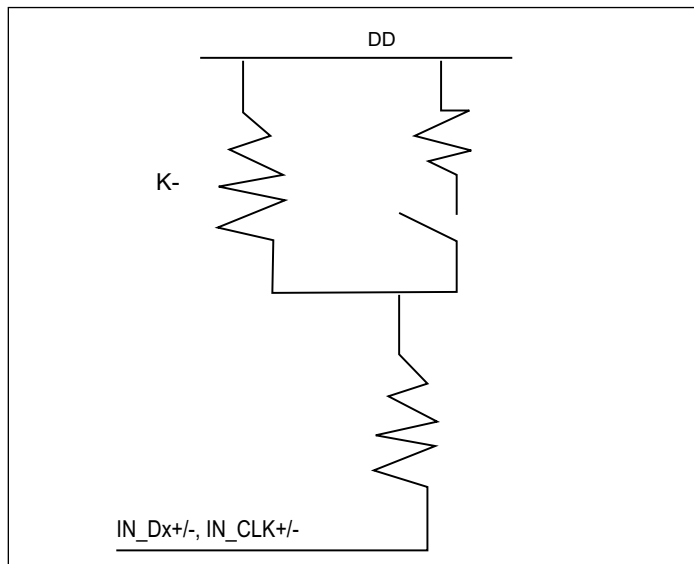


Pin Configuration

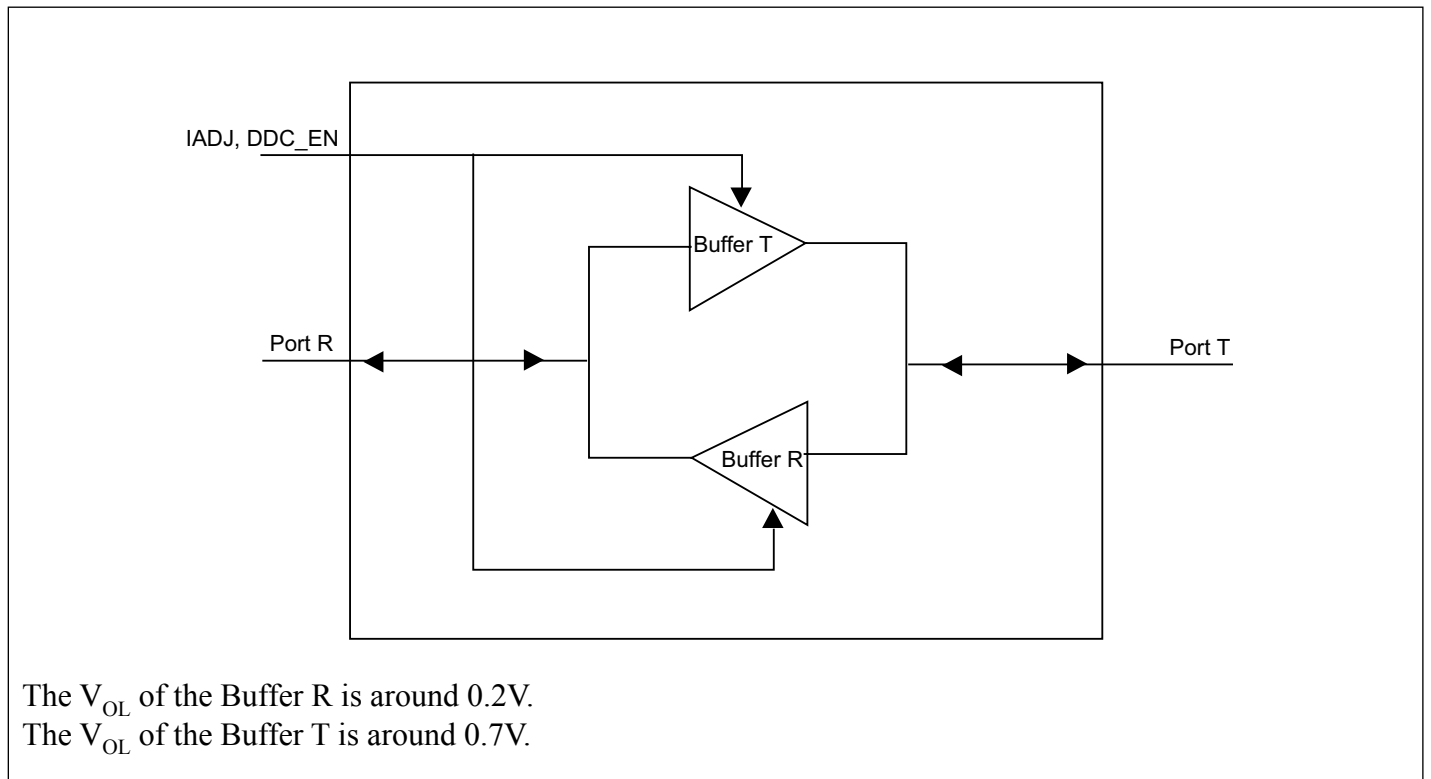


TMDS Receiver Block

Each high speed data and clock input has integrated equalization that can eliminate deterministic jitter caused by input cables. All activity can be configured using pin strapping. The Rx block is designed to receive all relevant signals directly from the HDMI™ connector without any additional circuitry, 3 High speed TMDS data, 1 pixel clock, and DDC signals. TMDS channels have the following termination scheme for Rx Sense support. The switching between 50-Ohm termination vs. 250K-Ohm termination is done automatically. The PI3HDMI101-B monitors the 50-Ohm termination in the Rx chipset behind our part, and when this 50-Ohm termination is not present, we disable our 50-Ohm termination at our input.



I²C Buffer



Functional Truth Tables

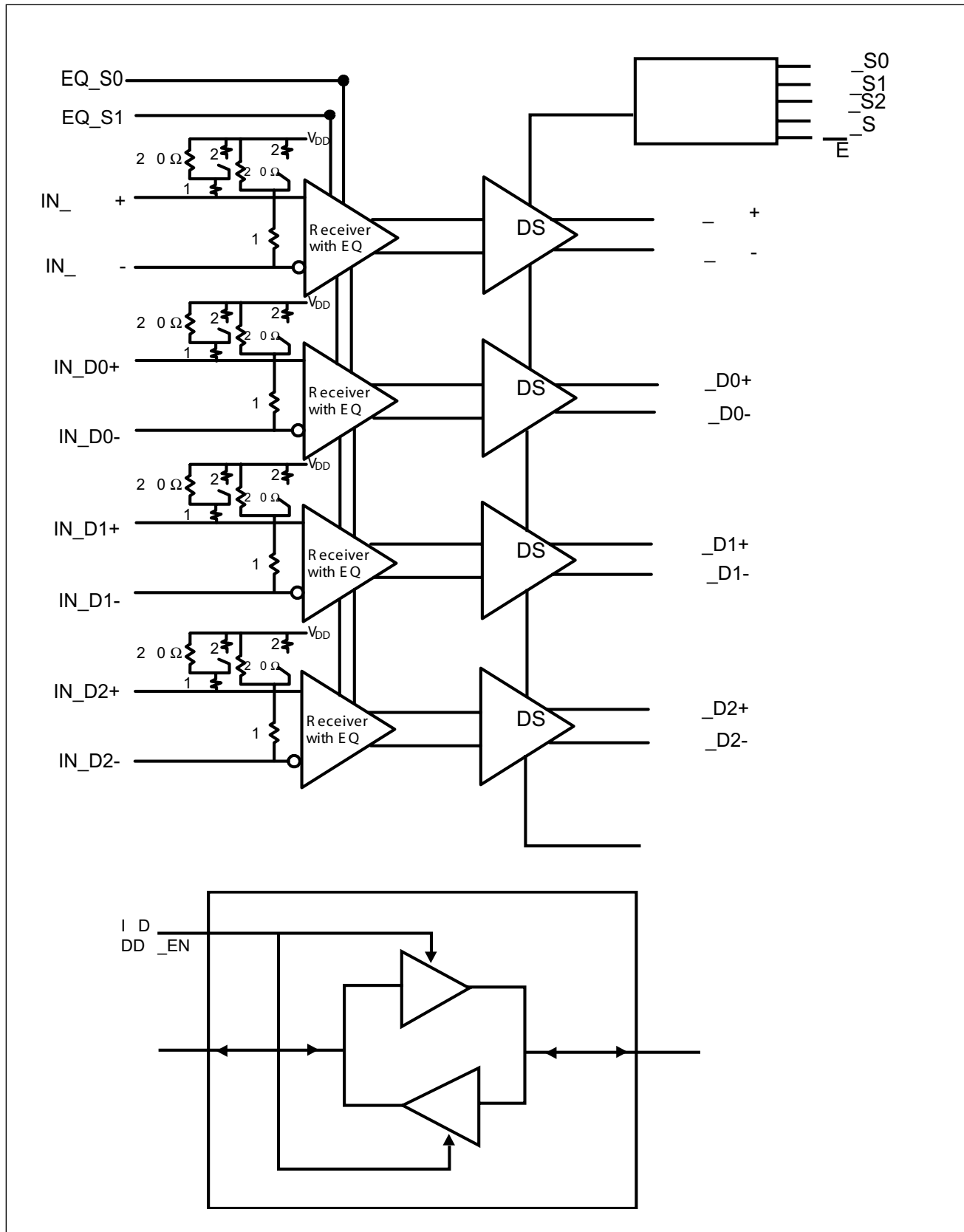
IADJ	External Pull-Up Range
H	1K-Ohm to 2K-Ohm (HDMI spec)
L	> 3K-Ohm (4.7K-Ohm typically)

DDC_EN	Port T / Port R (if no external pull-up resistor)
L	Hi-Z (I ² C buffer disable)
H	(I ² C buffer enable)

Pin Description

Pin #	Pin Name	I/O	Description
5 8 11 14	IN_CLK+ IN_D0+ IN_D1+ IN_D2+	I	TMDS Positive inputs
4 7 10 13	IN_CLK- IN_D0- IN_D1- IN_D2-	I	TMDS Negative inputs
3, 9, 15, 24, 30, 36	GND	P	Ground
18	$\overline{\text{OE}}$	I	Output Enable, Active LOW
41	SCL_R	I/O	DDC Clock , Source Side
40	SDA_R	I/O	DDC Data, Source Side
6, 12, 16, 23, 27, 33, 37	V _{DD}	P	3.3V Power Supply
34 31 28 25	OUT_CLK+ OUT_D0+ OUT_D1+ OUT_D2+	O	TMDS positive outputs
35 32 29 26	OUT_CLK- OUT_D0- OUT_D1- OUT_D2-	O	TMDS negative outputs
1 2	EQ_S0 EQ_S1	I	Equalizer controls, both pins with internal pull-ups
19 20 21 22	OC_S0 OC_S1 OC_S2 OC_S3	I	Output buffer controls Note: All 4 pins have internal pull-ups
17	DDC_EN	I	I ² C path enable
38	SCL_T	I/O	DDC Clock, Sink side
39	SDA_T	I/O	DDC Data, Sink side
42	IADJ	I	High/Low Voltage Selection, depends on I ² C external pull-up range

Complete high speed input Rx block is as follows:⁽¹⁾



Truth Table

$\overline{\text{OE}}$	Function
0	Active
1	All TMDS outputs are Hi-Z

Truth Table 1

OC_S3 ⁽²⁾	OC_S2 ⁽²⁾	OC_S1 ⁽²⁾	OC_S0 ⁽²⁾	Vswing(mv)	Pre/de-emphasis
1	1	1	1	500	0dB
1	1	1	0	600	0dB
1	1	0	1	750	0dB
1	1	0	0	1000	0dB
1	0	1	1	500	0dB
1	0	1	0	500	1.5dB
1	0	0	1	500	3.5dB
1	0	0	0	500	6dB
0	1	1	1	400	0dB
0	1	1	0	400	3.5dB
0	1	0	1	400	6dB
0	1	0	0	400	9dB
0	0	1	1	1000	0dB
0	0	1	0	666	-3.5dB
0	0	0	1	500	-6dB
0	0	0	0	333	-9dB

EQ Setting Value Logic Table

EQ_S1 ⁽²⁾	EQ_S0 ⁽²⁾	Gain (dB)
1	1	Optimized Equalization (Default Setting)
1	0	8
0	1	3
0	0	15

Notes:

1. External pull-ups are required along SCL/SDA path
2. Internal 100K-Ohm pull-ups

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential.....	–0.5V to +4.0V
DC Input Voltage	–0.5V to V _{DD}
DC Output Current.....	120mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V _{DD}	Supply Voltage	3.135	3.3	3.465	V
T _A	Operating free-air temperature	0		70	°C
TMDS Differential Pins					
V _{ID}	Receiver peak-to-peak differential input voltage	150		1560	mVp-p
V _{IC}	Input common mode voltage	2		V _{DD} + 0.01	V
V _{DD}	TMDS output termination voltage	3.135	3.3	3.465	V
R _T	Termination resistance	45	50	55	Ohm
	Signaling rate	0		2.5	Gbps
Control Pins (OC_Sx, EQ_Sx, $\overline{\text{OE}}$, DDC_EN)					
V _{IH}	LVTTL High-level input voltage	2		V _{DD}	V
V _{IL}	LVTTL Low-level input voltage	GND		0.8	
DDC Pins (SCL_R, SCL_T, SDA_R, SDA_T)					
V _{I(DDC)}	Input voltage	GND		5.5	V
I ² C Pins (SCL_T, SDA_T)					
V _{IH}	High-level input voltage	0.7 x V _{DD}		5.5	V
V _{IL}	Low-level input voltage	-0.5		0.3 x V _{DD}	V
V _{ICL}	Low-level input voltage contention ⁽¹⁾	-0.5		0.4	V
I ² C Pins (SCL_R, SDA_R)					
V _{IH}	High-level input voltage	0.7 x V _{DD}		5.5	V
V _{IL}	Low-level input voltage	-0.5		0.3 x V _{DD}	V

Notes:

- V_{IL} specification is for the first low level seen by the SCL/SDA lines. V_{ICL} is for the second and subsequent low levels seen by the SCL_T/SDA_T lines.

TMDs Compliance Test Results

Item	HDMI 1.3 Spec	Pericom Product Spec
Operating Conditions		
Termination Supply Voltage, V_{DD}	$3.3V \leq 5\%$	$3.30 \pm 5\%$
Terminal Resistance	$50\text{-}\Omega \pm 10\%$	45 to 55- Ω
Source DC Characteristics at TP1		
Single-ended high level output voltage, V_H	$V_{DD} \pm 10mV$	$V_{DD} \pm 10mV$
Single-ended low level output voltage, V_L	$(V_{DD} - 600mV) \leq V_L \leq (V_{DD} - 400mV)$	$(V_{DD} - 600mV) \leq V_L \leq (V_{DD} - 400mV)$
Single-ended output swing voltage, V_{swing}	$400mV \leq V_{swing} \leq 600mV$	$400mV \leq V_{swing} \leq 600mV$
Single-ended standby (off) output voltage, V_{off}	$V_{DD} \pm 10mV$	$V_{DD} \pm 10mV$
Transmitter AC Characteristics at TP1		
Risetime/Falltime (20%-80%)	$75ps \leq \text{Risetime/Falltime} \leq 0.4 \text{ Tbit}$ ($75ps \leq tr/tf \leq 242ps$) @ 1.65 Gbps	240ps
Intra-Pair Skew at Transmitter Connector, max	0.15 Tbit (90.9ps @ 1.65 Gbps)	60ps max
Inter-Pair Skew at Transmitter Connector, max	0.2 Tpixel (1.2ns @ 1.65 Gbps)	100ps max
Clock Jitter, max	0.25 Tbit (151.5ps @ 1.65 Gbps)	82ps max
Sink Operating DC Characteristics at TP2		
Input Differential Voltage Level, V_{diff}	$150 \leq V_{diff} \leq 1200mV$	$150mV \leq V_{DIFF} \leq 1200mV$
Input Common Mode Voltage Level, V_{ICM}	$(V_{DD} - 300mV) \leq V_{icm} \leq (V_{DD} - 37.5mV)$ Or $V_{DD} \pm 10\%$	$(V_{DD} - 300mV) \leq V_{icm} \leq (V_{DD} - 37.5mV)$ Or $V_{DD} \pm 10\%$
Sink DC Characteristics When Source Disabled or Disconnected at TP2		
Differential Voltage Level	$V_{DD} \pm 10mV$	$V_{DD} \pm 10mV$

Electrical Characteristics (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
I _{CC}	Supply Current	V _{IH} = V _{DD} , V _{IL} = V _{DD} - 0.4V, R _T = 50-Ohm, V _{DD} = 3.3V		120		mA
P _D	Power Dissipation	Data Inputs = 1.65 Gbps HDMI data pattern CLK Inputs = 165 MHz clock OC_Sx = Low, x = 0,1,2,3		400		mW
I _{CCQ}	Standby Current	\overline{OE} = HIGH, V _{DD} = 3.3V, RxSense = LOW		8		mA

TMDS Differential Pins

V _{OH}	Single-ended high-level output voltage	V _{DD} = 3.3V, R _T = 50-Ohm Pre-emphasis/De-emphasis = 0dB	V _{DD} - 10		V _{DD} + 10	mV
V _{OL}	Single-ended low-level output voltage		V _{DD} - 600		V _{DD} - 400	
V _{swing}	Single-ended output swing voltage		400		600	
V _{OD(O)}	Overshoot of output differential voltage			6%	15%	2x V _{swing}
V _{OD(U)}	Undershoot of output differential voltage			12%	25%	
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage between logic states			0.5	5	mV
I _(OS)	Short circuit output current				12	mA
V _{ODE(SS)}	Steady state output differential voltage	OC_Sx = GND, Data Inputs = 250 Mbps HDMI data pattern, 25 MHz pixel clock	560		840	mVp-p
V _{ODE(PP)}	Peak-to-peak output differential voltage		800		1200	
V _{I(open)}	Single-ended input voltage under high impedance input or open input	I _I = 10μA	V _{DD} - 10		V _{DD} + 10	mV
R _{INT}	Input termination resistance	V _{IN} = 2.9V	45	50	55	ohm

Control Pins (\overline{OE} , DDC_EN, IADJ)

I _{IH}	High-level digital input current	V _{IH} = 2V or V _{DD}	-10		10	μA
I _{IL}	Low-level digital input current	V _I = GND or 0.8 V	-10		10	μA

I²C Pins (SCL_T, SDA_T) (T Port)

I _{ikg}	Input leakage current	V _I = 5.5 V	-50		50	μA
		V _I = V _{DD}	-20		20	
I _{OH}	High-level output current	V _O = 3.6 V	-10		10	μA
I _{IL}	Low-level input current	V _{IL} = GND	-40		40	μA
V _{OL}	Low-level output voltage	I _{OL} = 2.5 mA IADJ = H	0.65		0.9	V

(Table Continued)

Electrical Characteristics (Cont..)

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
C _{IO}	Input/output capacitance	V _I = 5.0 V or 0 V, Freq = 100kHz			25	pF
		V _I = 3.0 V or 0 V, Freq = 100kHz			10	
V _{OH(TTL)} ¹	TTL High-level output voltage	I _{OH} = -8 mA	2.4			V
V _{OL(TTL)} ¹	TTL Low-level output voltage	I _{OL} = 8 mA			0.4	V

Note:

1. V_{oh}/V_{ol} of external driver at the R and T ports.

I ² C Pins (SCL_R, SDA_R) (R Port)						
I _{ikg}	Input leakage current	V _I = 5.5 V	-50		50	μA
		V _I = V _{DD}	-20		20	
I _{OH}	High-level output current	V _O = 3.6 V	-10		10	μA
I _{IL}	Low-level input current	V _{IL} = GND	-10		10	μA
V _{OL}	Low-level output voltage	I _{OL} = 4 mA, I _{ADJ} = H			0.2	V
C _I	Input capacitance	V _I = 5.0 V or 0 V, Freq = 100kHz			25	pF
		V _I = 3.0 V or 0 V, Freq = 100kHz			10	

Switching Characteristics (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
TMDS Differential Pins						
tpd	Propagation delay	V _{DD} = 3.3V, R _T = 50-Ohm, pre-emphasis/de-emphasis = 0dB			2000	ps
t _r	Differential output signal rise time (20% - 80%)		75		240	
t _f	Differential output signal fall time (20% - 80%)		75		240	
t _{sk(p)}	Pulse skew			10	50	
t _{sk(D)}	Intra-pair differential skew			23	50	
t _{sk(o)}	Inter-pair differential skew ⁽²⁾				100	
t _{jit(pp)}	Peak-to-peak output jitter from TMDS clock channel	pre-emphasis/de-emphasis = 0dB, Data Inputs = 1.65 Gbps HDMI data pattern CLK input = 165 MHz clock		15	30	
t _{jit(pp)}	Peak-to-peak output jitter from TMDS data channel			18	50	
t _{DE}	De-emphasis duration	de-emphasis = -3.5dB, Data Inputs = 250 Mbps HDMI data pattern, CLK output = 25 MHz clock		240		

(Table Continued)

Switching Characteristics (Cont.)

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
t _{sx}	Select to switch output				10	ns
t _{en}	Enable time				200	
t _{dis}	Disable time				10	
I ² C PINS (SCL_R, SDA_R, SCL_T, SDA_T)						
t _{PLH}	Propagation delay time, low-to-high-level output SCL_T/SDA_T to SCL_R/SDA_R	I _{ADJ} = V _{DD} C _{LOAD} = 300 pF			500	ns
t _{PHL}	Propagation delay time, high-to-low-level output SCL_T/SDA_T to SCL_R/SDA_R	T _{buffer} : R _{pu} = 2K, V _{pu} = 3.0V			136	
t _{PLH}	Propagation delay time, low-to-high-level output SCL_T/SDA_T to SCL_R/SDA_R	R _{buffer} : R _{pu} = 1.2K, V _{pu} = 3.3V or R _{pu} = 1.8K, V _{pu} = 5V			450	
t _{PHL}	Propagation delay time, high-to-low-level output SCL_T/SDA_T to SCL_R/SDA_R	I _{ADJ} = GND C _{LOAD} = 100 pF			136	
t _r	SCL_T/SDA_T Output signal rise time	See Fig. A			999	
t _f	SCL_T/SDA_T Output signal fall time				90	
t _r	SCL_R/SDA_R Output signal rise time				999	
t _f	SCL_R/SDA_R Output signal fall time				90	

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{set}	Enable to start condition			6	10	ns
t_{hold}	Enable after stop condition			6	10	

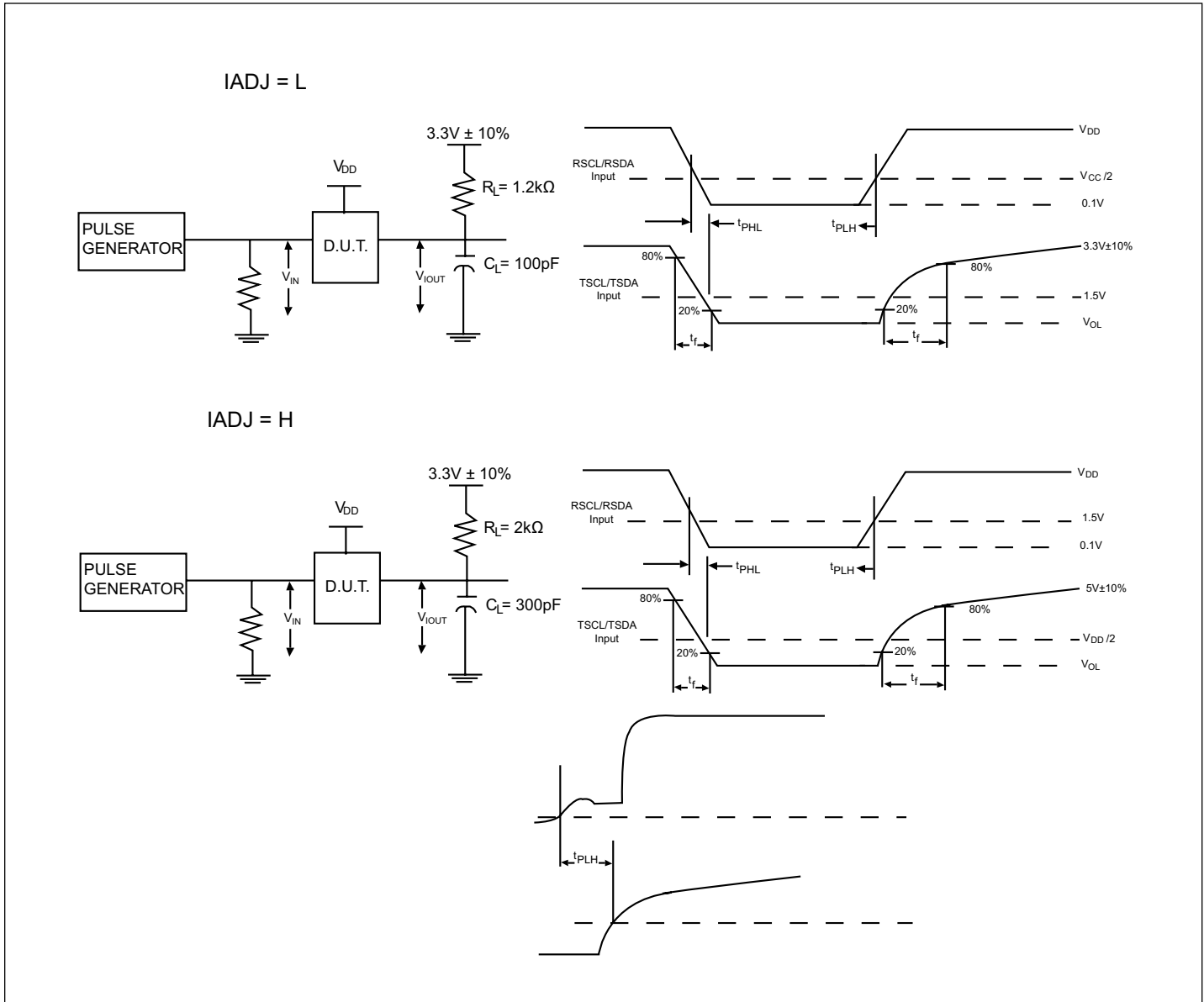
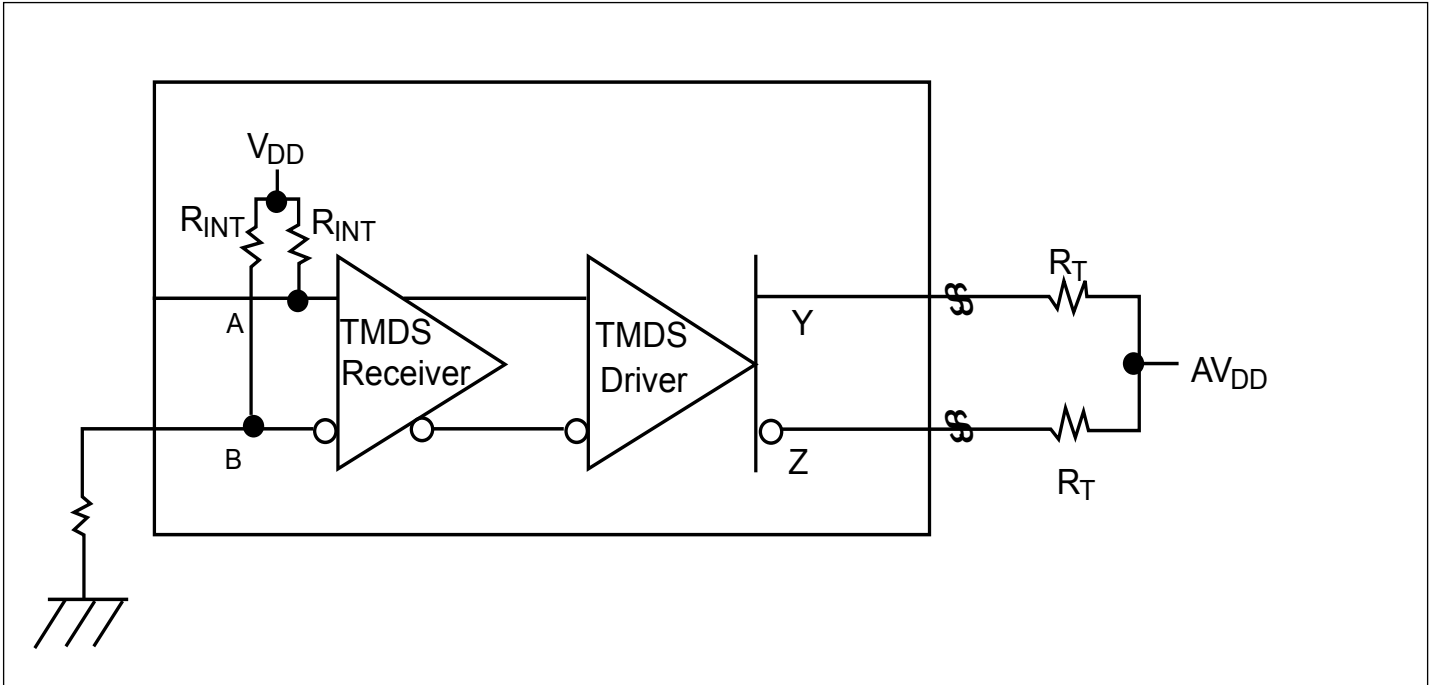


Figure A. I²C Timing Test Circuit and Definition

TMDS output oscillation elimination

The TMDS inputs do not incorporate a squelch circuit. Therefore, we recommend the input to be externally biased to prevent output oscillation. One pin will be pulled high to VDD with the other grounded through a 1.5K-Ohm resistor as shown.



TMDS Input Fail-Safe Recommendation

Recommended Power Supply Decoupling Circuit

Figure 1 is the recommended power supply decoupling circuit configuration. It is recommended to put 0.1μF decoupling capacitors on each VDD pins of our part, there are four 0.1μF decoupling capacitors are put in Figure 1 with an assumption of only four VDD pins on our part, if there is more or less VDD pins on our Pericom parts, the number of 0.1μF decoupling capacitors should be adjusted according to the actual number of VDD pins. On top of 0.1μF decoupling capacitors on each VDD pins, it is recommended to put a 10μF decoupling capacitor near our part's VDD, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.

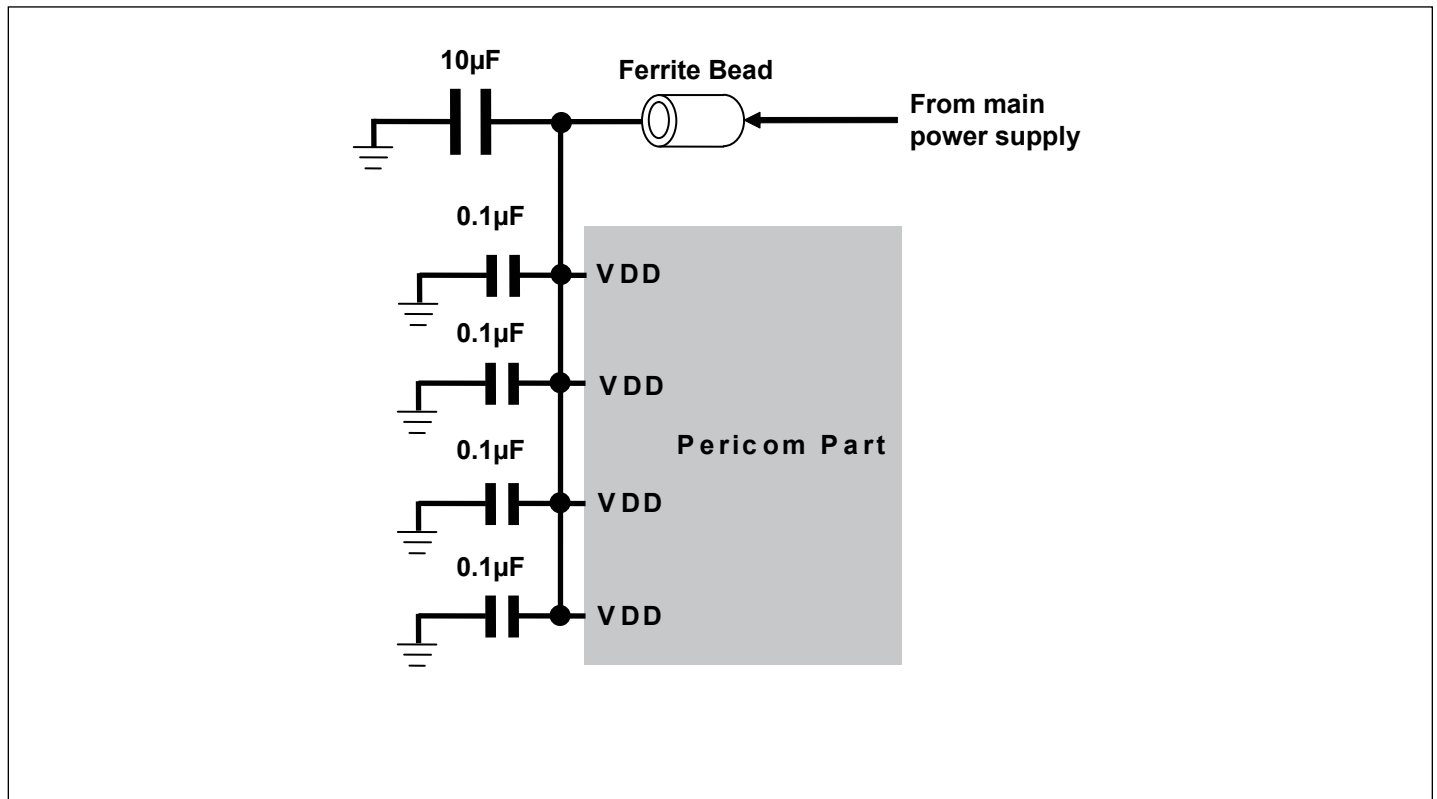


Figure 1 Recommended Power Supply Decoupling Circuit Diagram

Requirements on the Decoupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

Layout and Decoupling Capacitor Placement Consideration

- i. Each 0.1µF decoupling capacitor should be placed as close as possible to each V_{DD} pin.
- ii. V_{DD} and GND planes should be used to provide a low impedance path for power and ground.
- iii. Via holes should be placed to connect to V_{DD} and GND planes directly.
- iv. Trace should be as wide as possible
- v. Trace should be as short as possible.
- vi. The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
- vii. 10µF capacitor should also be placed closed to our part and should be placed in the middle location of 0.1µF capacitors.
- viii. Avoid the large current circuit placed close to our part; especially when it is shared the same V_{DD} and GND planes. Since large current flowing on our V_{DD} or GND planes will generate a potential variation on the V_{DD} or GND of our part.

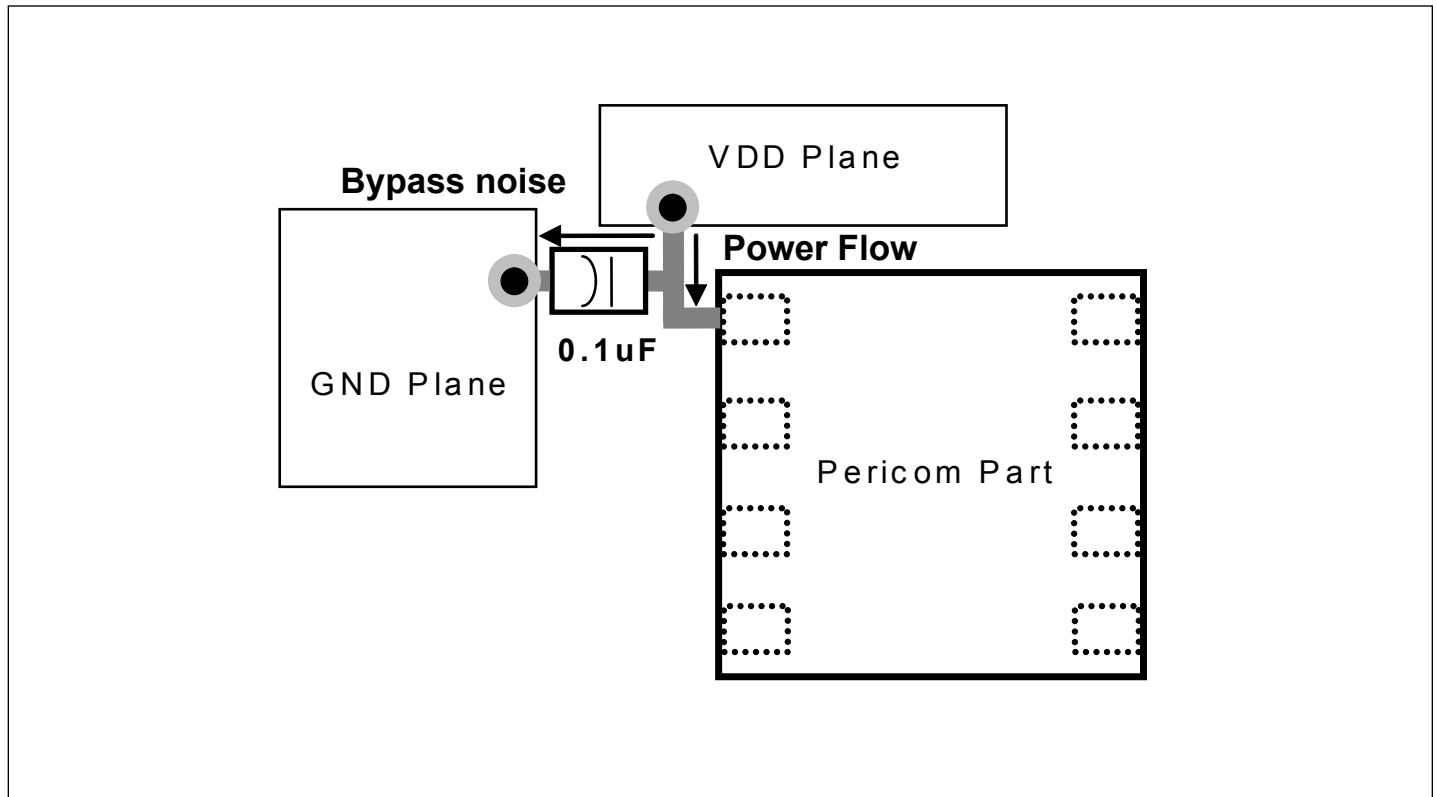


Figure 2 Layout and Decoupling Capacitor Placement Diagram

Application Information

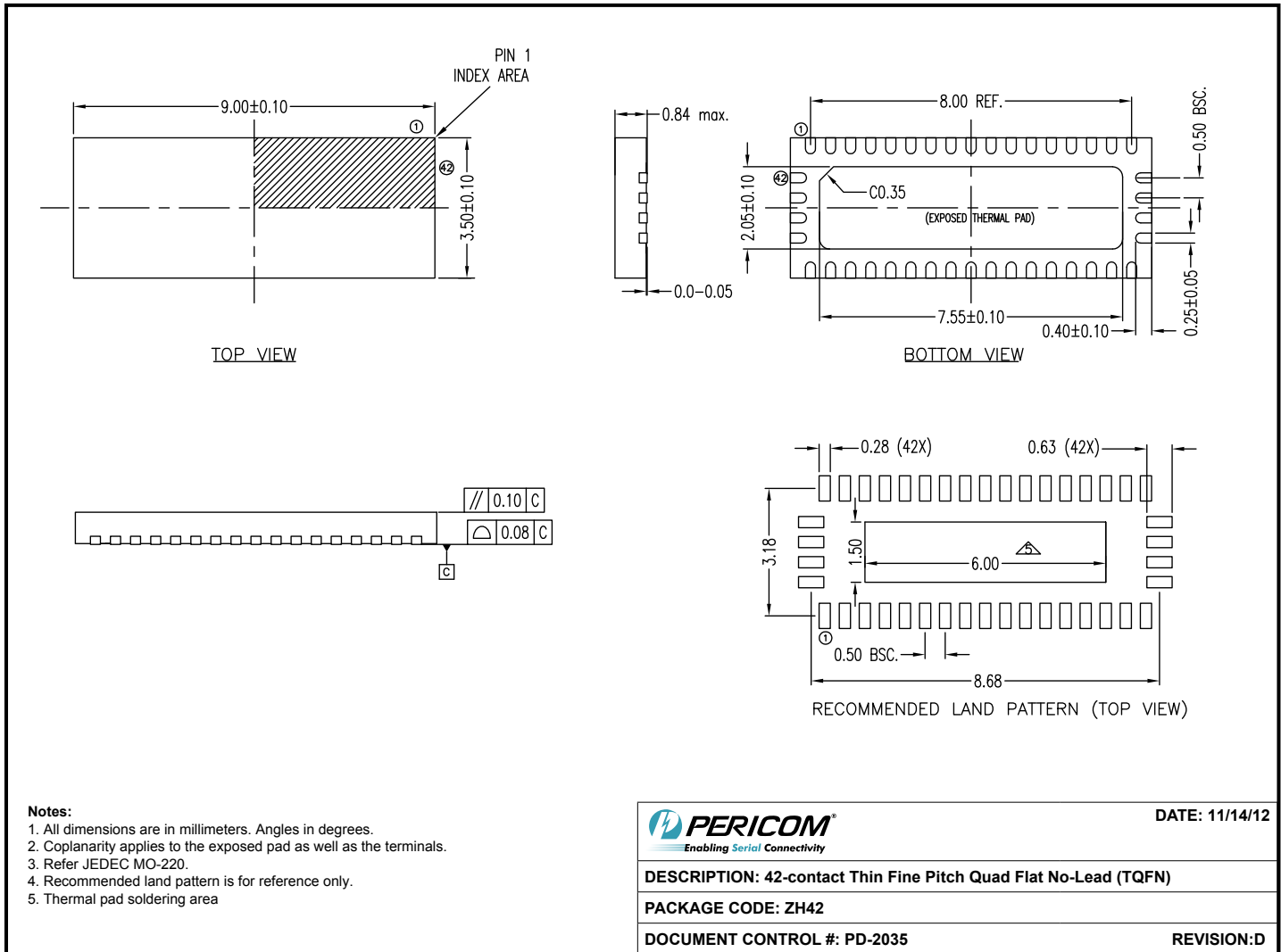
Supply Voltage

All V_{DD} pins are recommended to have a $0.01\mu\text{F}$ capacitor tied from V_{DD} to GND to filter supply noise

TMDS inputs

Standard TMDS terminations have already been integrated into Pericom's PI3HDMI101-A device. Therefore, external terminations are not required. Any unused port must be left floating and not tied to GND.

Package Mechanical: 42-pin, Low Profile Quad Flat Package (ZH42)



12-0529

Ordering Information

Ordering Code	Package Code	Package Description
PI3HDMI101-BZHE	ZH	42-pin, Pb-free & Green TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel
- HDMI & DeepColor are trademarks of Silicon Image