ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC}, COM.....-0.3V to +6.0V
OUT_.....-0.3V to (V_{COM} + 0.3V)
$\overline{CS}$, SCLK, DIN, $\overline{SET}$, $\overline{RESET}$, A0, A1, A2, LVL.....-0.3V to +6.0V
DOUT.....-0.3V to (V_{CC} + 0.3V)
Continuous OUT_ Current (all outputs turned on) 150mA
Continuous OUT_ Current (single output turned on) 300mA

Continuous Power Dissipation (T_A = +70°C)
20-Lead Thin QFN (derate 16.9mW/°C above +70°C)..1350mW
θ_{JA} (Note 1) .....59.3°C/W
20-Pin TSSOP (derate 21.7mW/°C above +70°C) 1739mW
θ_{JA} (Note 1) .....46°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (10s).....+300°C
Reflow Temperature.....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specifications. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3V to +5.5V, V_{COM} = V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage	V_{CC}			2.3		5.5	V
Quiescent Current	I_Q	$I_{OUT\_}$ = 0µA, logic inputs = 0V or V_{CC}	V_{CC} = 3.6V		15	50	µA
			V_{CC} = 5.5V		20	70	
Thermal Shutdown					160		°C
Power-On Reset				0.8	1.5	2.2	V
Power-On Reset Hysteresis					140		mV
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, LVL, A0, A1, A2, $\overline{RESET}$, $\overline{SET}$)							
Input Logic-High Voltage	V_{IH}	V_{CC} = 3.3V		2.0			V
		V_{CC} = 5V		2.4			
Input Logic-Low Voltage	V_{IL}	V_{CC} = 3.3V				0.6	V
		V_{CC} = 5V				0.8	
Input Logic Hysteresis	V_{HYST}				150		mV
Input Leakage Currents	I_{LEAK}	Input voltages = 0V or 5.5V		-1.0	0.01	+1.0	µA
C_{IN} Input Capacitance	C_{IN}				5		pF
DIGITAL OUTPUT (DOUT)							
DOUT Low Voltage	V_{OL}	I_{SINK} = 6mA				0.4	V
DOUT High Voltage	V_{OH}	I_{SOURCE} = 0.5mA		V_{CC} - 0.5			V
RELAY OUTPUT DRIVERS (OUT1–OUT8)							
OUT_ Drive Current		V_{CC} = 2.7V		70			mA
		V_{CC} = 4.5V		70			
OUT_ On-Resistance	R_{ON}	V_{CC} = 2.7V			2	6	Ω
OUT_ Voltage	$V_{OUT\_}$	V_{CC} = 3.0V, $I_{OUT\_}$ = 70mA				0.4	V
I_{OUT} Off-Leakage Current	I_{LEAK}	$V_{OUT\_}$ = V_{CC}, all outputs off		-1		+1	µA
Kickback Diode Forward Voltage	V_{FORW}	$I_{OUT\_}$ = 150mA (Note 3)				1.5	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3V to +5.5V, V_{COM} = V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI TIMING (MAX4820)						
Turn-On Time (OUT_)	t_{ON}	From rising edge of $\overline{CS}$, R_L = 50Ω, C_L = 50pF			1.0	µs
Turn-Off Time (OUT_)	t_{OFF}	From rising edge of $\overline{CS}$, R_L = 50Ω, C_L = 50pF			1.0	µs
SCLK Frequency	f_{SCLK}		0		2.1	MHz
Cycle Time	t_{CH} + t_{CL}		480			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		240			ns
$\overline{CS}$ Rise to SCLK Hold	t_{CSH}		240			ns
SCLK High Time	t_{CH}		190			ns
SCLK Low Time	t_{CL}		190			ns
Data Setup Time	t_{DS}		100			ns
Data Hold Time	t_{DH}		0			ns
SCLK Fall to DOUT Valid	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 50pF		85	120	ns
Rise Time (DIN, SCLK, $\overline{CS}$, $\overline{SET}$, $\overline{RESET}$)	t_{SCR}	20% of V_{CC} to 70% of V_{CC}, C_L = 50pF			2	µs
Fall Time (DIN, SCLK, $\overline{CS}$, $\overline{RESET}$, $\overline{SET}$)	t_{SCF}	20% of V_{CC} to 70% of V_{CC}, C_L = 50pF			2	µs
$\overline{RESET}$ Min Pulse Width	t_{RW}		70			ns
$\overline{SET}$ Min Pulse Width	t_{SW}		70			ns
PARALLEL TIMING (MAX4821)						
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$, R_L = 50Ω, C_L = 50pF			1	µs
Turn-Off Time	t_{OFF}	From rising edge of $\overline{CS}$, R_L = 50Ω, C_L = 50pF			1	µs
LVL Setup Time	t_{LS}		100			ns
LVL Hold Time	t_{LH}		0			ns
Address to $\overline{CS}$ Setup Time	t_{AH}		100			ns
Address to $\overline{CS}$ Hold Time	t_{AS}		0			ns
Rise Time (A2, A1, A0, LVL)	t_{SCR}	20% of V_{CC} to 70% of V_{CC}, C_L = 50pF			2	µs
Fall Time (A2, A1, A0, LVL)	t_{SCF}	20% of V_{CC} to 70% of V_{CC}, C_L = 50pF			2	µs
$\overline{RESET}$ Pulse Width	t_{RW}		70			ns
$\overline{SET}$ Pulse Width	t_{SW}		70			ns

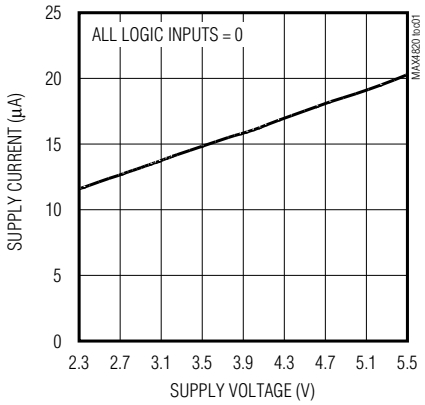
Note 2: Specifications at -40°C are guaranteed by design and not production tested.

Note 3: After relay turn-off, inductive kickback may momentarily cause the voltage at OUT_ to exceed V_{COM}. This is considered part of normal operation and will not damage the device.

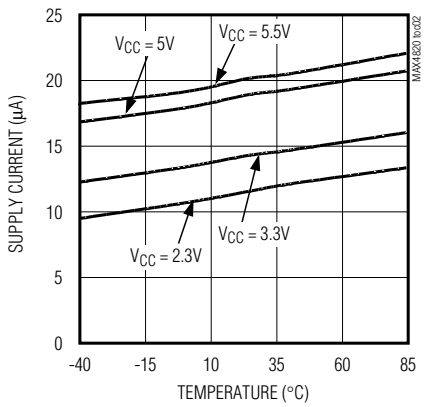
Typical Operating Characteristics

(V_{COM} = V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

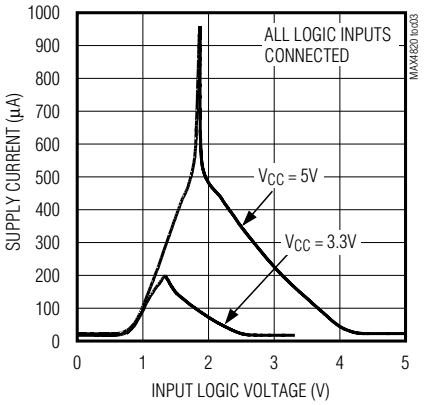
SUPPLY CURRENT vs. SUPPLY VOLTAGE



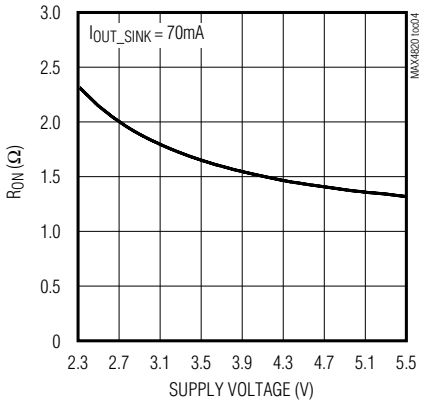
SUPPLY CURRENT vs. TEMPERATURE



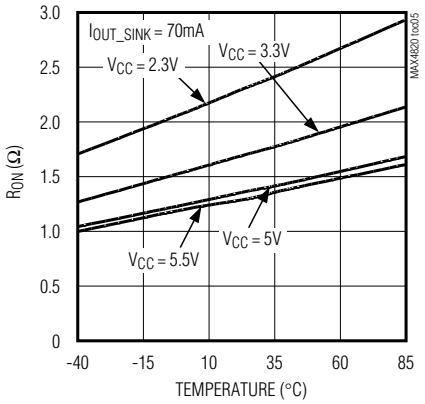
SUPPLY CURRENT vs. INPUT LOGIC VOLTAGE



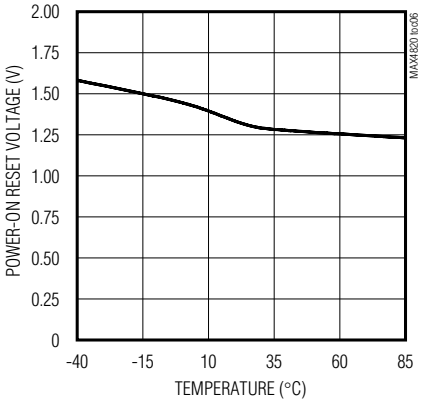
ON-RESISTANCE vs. SUPPLY VOLTAGE



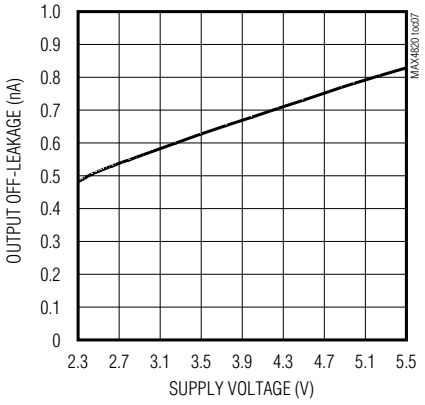
ON-RESISTANCE vs. TEMPERATURE



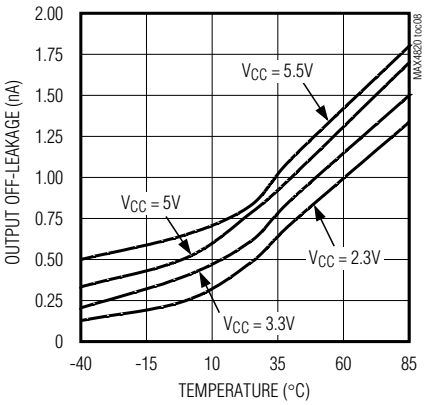
POWER-ON RESET VOLTAGE vs. TEMPERATURE



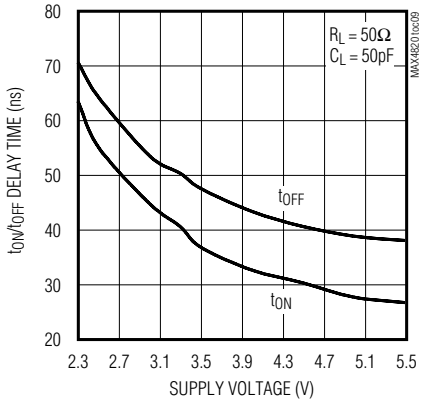
OUTPUT OFF-LEAKAGE CURRENT vs. SUPPLY VOLTAGE



OUTPUT OFF-LEAKAGE CURRENT vs. TEMPERATURE



OUT_ TURN-ON/TURN-OFF DELAY TIMES vs. SUPPLY VOLTAGE

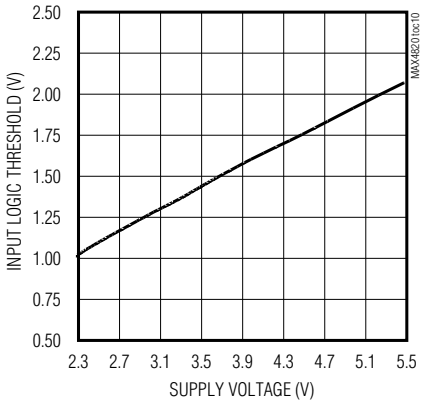


3.3V/+5V, 8-Channel, Cascadable Relay Drivers with Serial/Parallel Interface

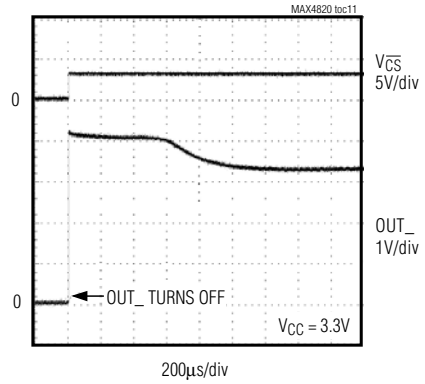
Typical Operating Characteristics (continued)

(V_{COM} = V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

INPUT LOGIC THRESHOLD vs. SUPPLY VOLTAGE



BACK EMF CLAMPING WITH STANDARD 3V RELAY



Pin Description

PIN				NAME	FUNCTION
MAX4820		MAX4821			
THIN QFN	TSSOP	THIN QFN	TSSOP		
1	3	1	3	$\overline{RESET}$	Reset Input. Drive $\overline{RESET}$ low to clear all latches and registers (all outputs are turned off). $\overline{RESET}$ overrides all other inputs. If $\overline{RESET}$ and $\overline{SET}$ are pulled low at the same time, then $\overline{RESET}$ takes precedence.
2	4	2	4	$\overline{CS}$	Chip-Select Input. **MAX4820:** Drive $\overline{CS}$ low to select the device. When $\overline{CS}$ is low, data at DIN is clocked into the 8-bit shift register on SCLK's rising edge. Drive $\overline{CS}$ from low to high to latch the data to the registers and activate the appropriate relays. **MAX4821:** Drive $\overline{CS}$ low to select the device and set level on LVL. Drive $\overline{CS}$ from low to high to latch the address and level data to the output.
3	5	—	—	DIN	Serial-Data Input
4	6	—	—	SCLK	Serial-Clock Input
5	7	—	—	DOUT	Serial-Data Output. DOUT is the output of the 8-bit shift register. This output can be used to daisy chain multiple MAX4820s. The data at DOUT appears synchronous to SCLK's falling edge.
6	8	—	—	N.C.	No Connection
7	9	7	9	GND	Ground
8	10	8	10	OUT8	Open-Drain Output 8. Connect OUT8 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.
9	11	9	11	OUT7	Open-Drain Output 7. Connect OUT7 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.
10, 16	12, 18	10, 16	12, 18	PGND	Power Ground. PGND is a return for the output sinks. Connect PGND pins together and to GND.
11	13	11	13	OUT6	Open-Drain Output 6. Connect OUT6 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.

Pin Description (continued)

PIN				NAME	FUNCTION
MAX4820		MAX4821			
THIN QFN	TSSOP	THIN QFN	TSSOP		
12	14	12	14	OUT5	Open-Drain Output 5. Connect OUT5 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.
13	15	13	15	COM	Common Free-Wheeling Diodes. Connect COM to V_{CC}. COM can also be connected to a separate supply that is higher than V_{CC}. In that case, bypass V_{CC} to GND with a 0.1µF capacitor.
14	16	14	16	OUT4	Open-Drain Output 4. Connect OUT4 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.
15	17	15	17	OUT3	Open-Drain Output 3. Connect OUT3 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.
17	19	17	19	OUT2	Open-Drain Output 2. Connect OUT2 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.
18	20	18	20	OUT1	Open-Drain Output 1. Connect OUT1 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.
19	1	19	1	V_{CC}	Input Supply Voltage. Bypass V_{CC} to GND with a 0.1µF capacitor.
20	2	20	2	$\overline{SET}$	Set Input. Drive $\overline{SET}$ low to set all latches and registers high (all outputs are turned on). $\overline{SET}$ overrides all parallel and serial control inputs. $\overline{RESET}$ overrides $\overline{SET}$ under all conditions.
—	—	3	5	LVL	Level Input. LVL determines whether the selected address is switched on or off. A logic high on LVL switches on the addressed output. A logic low on LVL switches off the addressed output.
—	—	4	6	A0	Digital Address “0” Input. (See Table 2 for address mapping.)
—	—	5	7	A1	Digital Address “1” Input. (See Table 2 for address mapping.)
—	—	6	8	A2	Digital Address “2” Input. (See Table 2 for address mapping.)
—	—	—	—	EP	Exposed Pad. Connect exposed pad to GND.

Detailed Description

The MAX4820/MAX4821 8-channel relay drivers offer built-in kickback protection and drive +3.3V/+5V non-latching or dual-coil-latching relays. These devices are especially useful when driving +3V relays. Each independent open-drain output features a 2Ω on-resistance and is guaranteed to sink 70mA (min) load current. Both devices consume less than 50µA (max) quiescent current and feature 1µA (min) output off-leakage current.

The MAX4820 features an SPI/QSPI/MICROWIRE-compatible serial interface. Input data is shifted into an 8-bit shift register and latched to the outputs when $\overline{CS}$ transitions from low to high. Each data bit in the shift register corresponds to a specific output, allowing independent control of all outputs.

The MAX4821 features a 4-bit (A0, A1, A2, LVL) parallel input interface. The three bits (A0, A1, A2) determine the output address, and LVL determines whether the selected output is switched on or off. Data is latched to the outputs when $\overline{CS}$ transitions from low to high.

Both devices feature separate set and reset functions that allow the user to turn on or turn off all outputs simultaneously with a single control line. Built-in hysteresis (Schmidt trigger) on all digital inputs allows this device to be used with slow rising and falling signals, such as those from optocouplers or RC power-up initialization circuits. The MAX4820/MAX4821 are available in 20-pin TSSOP and space-saving 20-pin Thin QFN packages.

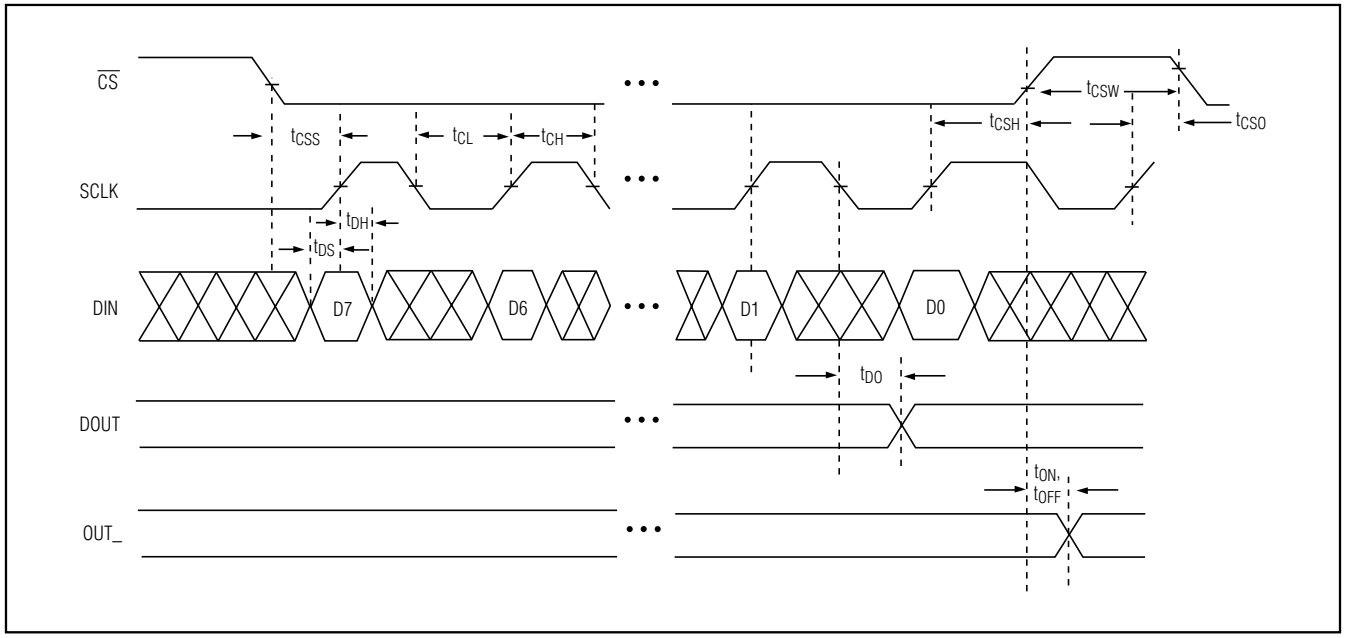


Figure 1. 3-Wire Serial-Interface Timing Diagram (MAX4820 only)

Table 1. Serial Input Address Map (MAX4820 Only)

DIN	D0	D1	D2	D3	D4	D5	D6	D7
OUT_	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7	OUT8

Digital Interface

Serial Interface (MAX4820)

The serial interface consists of an 8-bit shift register and parallel latch controlled by SCLK and $\overline{CS}$. The input to the shift register is an 8-bit word. Each data bit controls one of the eight outputs, with the most significant bit (D7) corresponding to OUT8 and the least significant bit (D0) corresponding to OUT1 (see Table 1). When $\overline{CS}$ is low (device is selected), data at DIN is clocked into the shift register synchronously with SCLK's rising edge. Driving $\overline{CS}$ from low to high latches the data in the shift register to the parallel latch.

DOUT is the output of the shift register. Data appears on DOUT synchronously with SCLK's falling edge and is identical to the data at DIN delayed by eight clock cycles. When shifting the input data, D7 is the first bit in and out of the shift register.

While $\overline{CS}$ is low, the switches always remain in their previous state. Drive $\overline{CS}$ high after 8 bits of data have been shifted in to update the output state and inhibit further data from entering the shift register. When $\overline{CS}$ is high, transitions at DIN and SCLK have no effect on the output, and the first input bit (D7) is present at DOUT.

If the number of data bits entered while $\overline{CS}$ is low is greater or less than 8, the shift register contains only the last 8 data bits, regardless of when they were entered.

The 3-wire serial interface is compatible with SPI, QSPI, and MICROWIRE standards. The latch that drives the analog switch is updated on the rising edge of $\overline{CS}$, regardless of SCLK's state.

Parallel Interface (MAX4821)

The parallel interface consists of three address bits (A0, A1, A2) and one level selector bit (LVL). The address bits determine which output is updated, and the level bit determines whether the addressed output is switched on (LVL = high) or off (LVL = low). When $\overline{CS}$ is high, the address and level bits have no effect on the state of the outputs. Driving $\overline{CS}$ from low to high latches the address and level data to the parallel register and updates the state of the outputs. Address data entered after $\overline{CS}$ is pulled low is not reflected in the state of the outputs following the next low-to-high transition on $\overline{CS}$ (Figure 2).

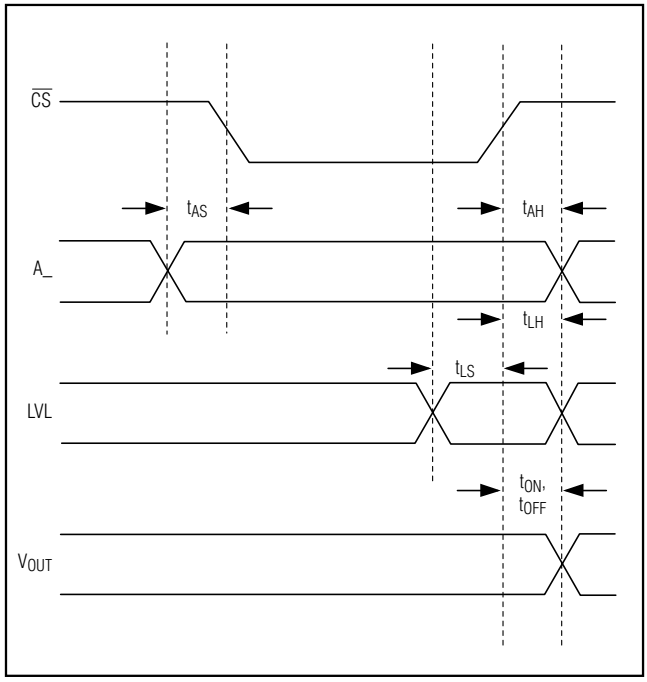


Figure 2. Parallel Interface Timing Diagram (MAX4821 only)

Table 2. Parallel Interface Address Map (MAX4821 Only)

A2	A1	A0	OUTPUT
Low	Low	Low	OUT1
Low	Low	High	OUT2
Low	High	Low	OUT3
Low	High	High	OUT4
High	Low	Low	OUT5
High	Low	High	OUT6
High	High	Low	OUT7
High	High	High	OUT8

SET/RESET Functions

The MAX4820/MAX4821 feature set and reset inputs that allow the user to simultaneously turn all outputs on or off using a single control line. Drive SET low to set all latches and registers to 1 and turn all outputs on. SET overrides all serial/parallel control inputs. Drive RESET low to clear all latches and registers and turn all outputs off. RESET overrides all other inputs, including SET.

Applications Information

Daisy Chaining

The MAX4820 features a digital output, DOUT, that provides a simple way to daisy chain multiple devices. This feature allows the user to drive large banks of relays using only a single serial interface. To daisy chain multiple devices, connect all CS pins together, and connect the DOUT of one device to the DIN of another device (see Figure 3). During operation, a stream of serial data

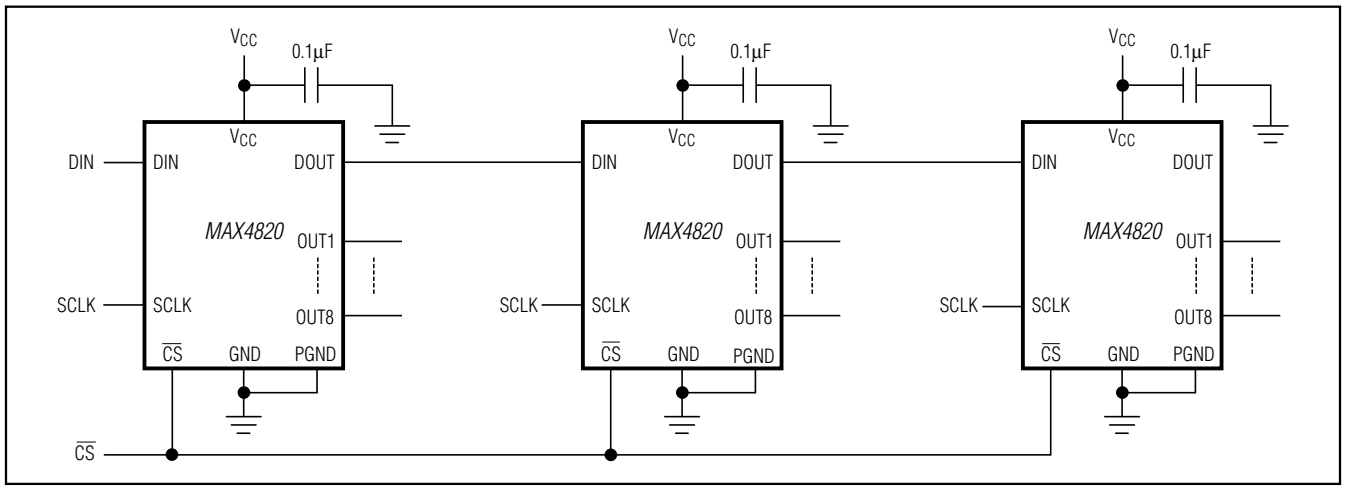


Figure 3. Daisy-Chain Configuration

is shifted through all the MAX4820s in series. When $\overline{CS}$ goes high, all outputs update simultaneously.

The MAX4820 can also be used in a slave configuration that allows the user to address individual devices. Connect all the DIN pins together, and use the $\overline{CS}$ input to address one device at a time. Drive $\overline{CS}$ low to select a slave and input the data into the shift register. Drive $\overline{CS}$ high to latch the data and turn on the appropriate outputs. Typically, in this configuration only one slave is addressed at a time.

Inductive Kickback Protection

The MAX4820/MAX4821 feature built-in inductive kickback protection to reduce the voltage spike on OUT_ generated by a relay's coil inductance when the output is suddenly switched off. Internal diodes connected from each output to COM allow the inductor current to flow back to the supply. Connect the common cathode (COM) of the internal protection diodes to V_{CC}.

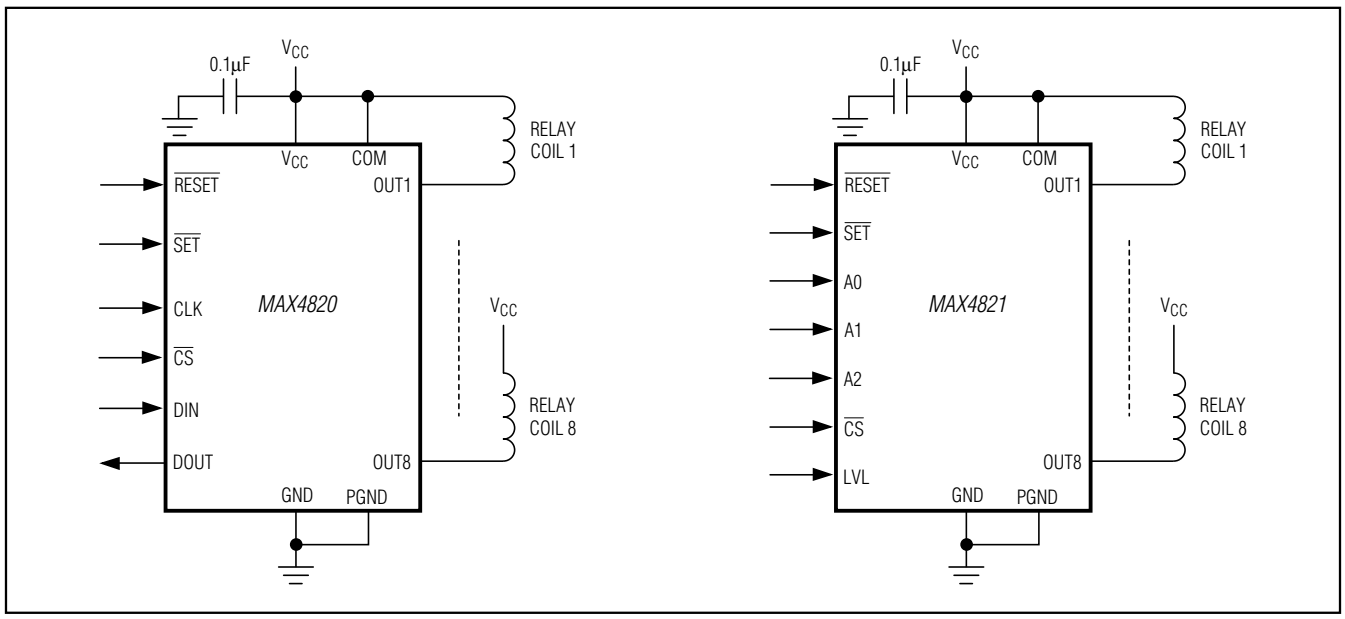
COM also can be connected to a higher voltage than V_{CC} (+6V max) for faster kickback recovery. In this configuration, bypass COM to PGND with a 0.1µF capacitor.

Relay Manufacturers

COMPANY	PHONE	WEBSITE
Aromat Corp.	310-524-9862	www.aromat.com
CP Clare Corp.	978-524-6700	www.crouzet.com
Coto Techonology	401-943-2686	www.cotorelay.com
Deustch Relays, Inc.	516-499-6000	www.deutschrelays.com
Fujitsu Takamisawa	408-745-4900	www.fujitsufta.com
Hella KG Hueck	734-414-0970	www.hella.com

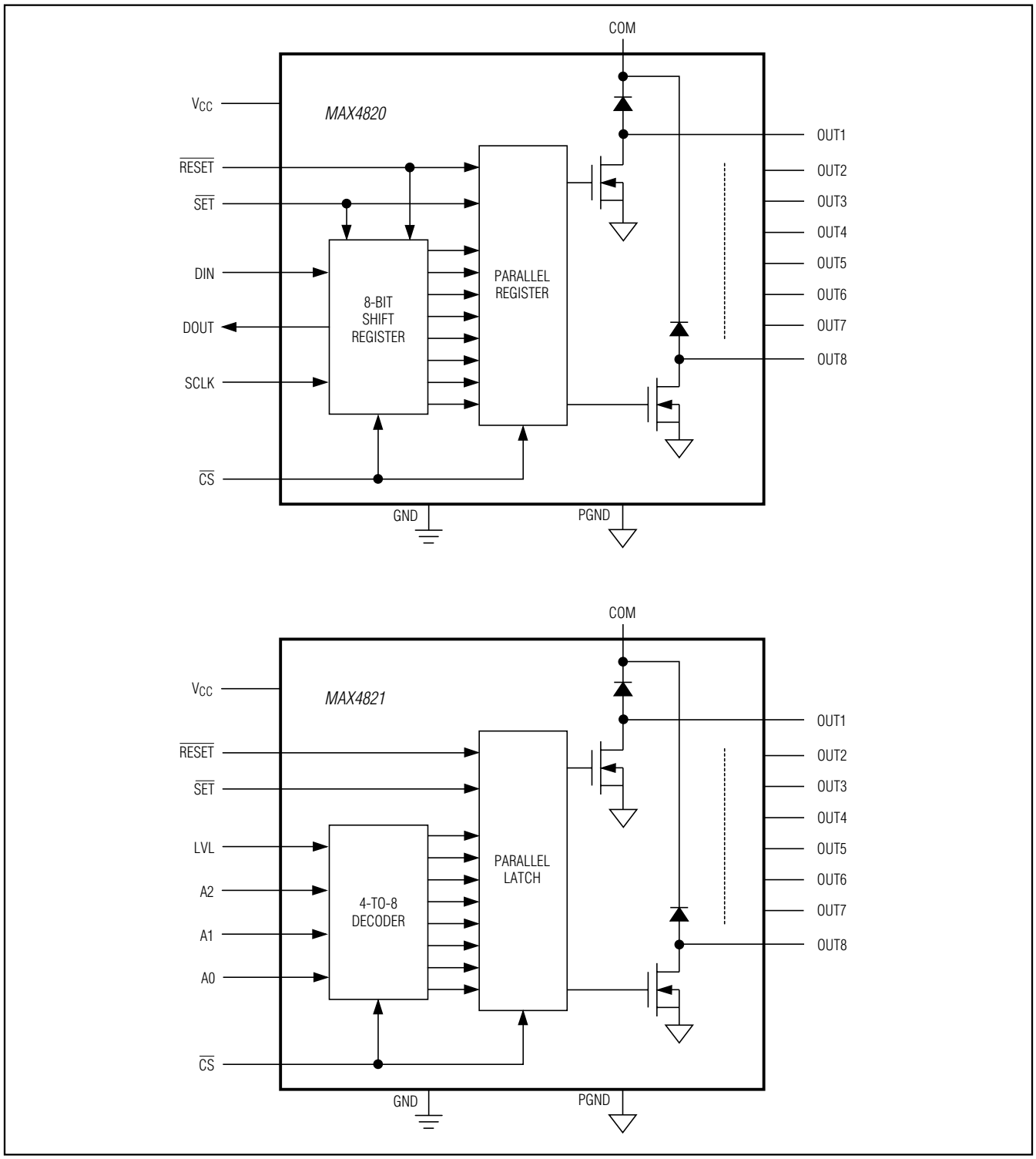
COMPANY	PHONE	WEBSITE
NEC Electronics, Inc.	800-366-9782	www.nec-global.com
Omron Electronics, Inc.	847-843-7900	www.oeiweb.omron.com
Rockwell/Allen-Bradley	414-382-2000	www.ab.com
Siemens Electromechanical Component, Inc.	770-371-3000	www.sec.siemens.com
Teledyne Relays	213-777-0077	www.teledynerelays.com

Typical Application Circuits



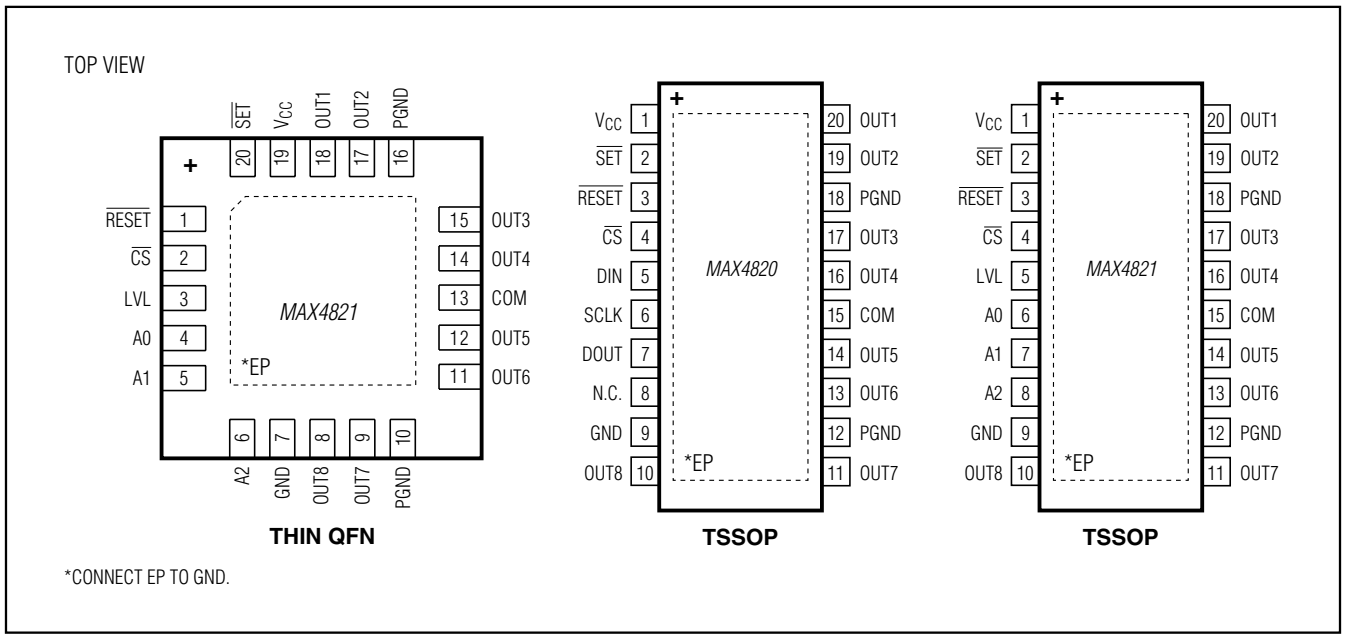
+3.3V/+5V, 8-Channel, Cascadable Relay Drivers with Serial/Parallel Interface

Functional Diagrams



3.3V/+5V, 8-Channel, Cascadable Relay Drivers with Serial/Parallel Interface

Pin Configurations (continued)



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 TQFN-EP	T2044+3	21-0139
20 TSSOP-EP	U20E+1	21-0108

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/03	Initial release.	—
1	4/09	Corrected error in the *Electrical Characteristics* table.	1, 2, 3, 5, 11, 12, 13
2	1/10	Added exposed pad to TSSOP package in the *Ordering Information*, *Pin Description*, and *Pin Configurations*.	1, 6, 11
		Added Reflow Temperature to the *Absolute Maximum Ratings* section.	2