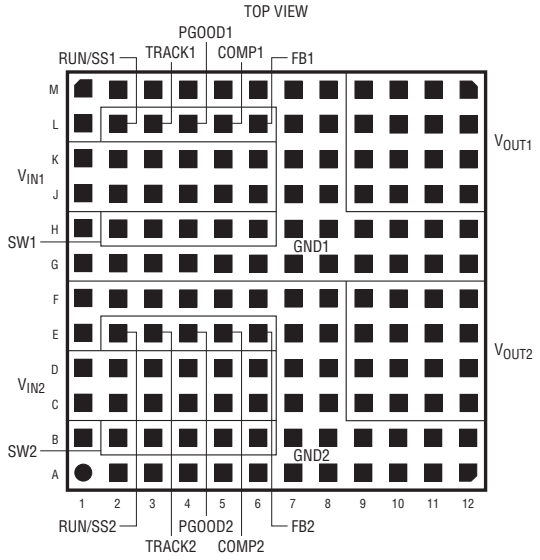
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1}, V_{IN2}, PGOOD1, PGOOD2 ..... –0.3V to 6V
COMP1, COMP2, RUN/SS1, RUN/SS2
FB1, FB2,TRACK1, TRACK2 ..... –0.3V to V_{IN}
SW1, SW2, V_{OUT1}, V_{OUT2} ..... –0.3V to (V_{IN} + 0.3V)
Internal Operating Temperature Range
(Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Body Temperature, Solder Reflow ..... 245°C

PIN CONFIGURATION

(See Pin Functions, Pin Configuration Table)



LGA PACKAGE
144-LEAD (15mm × 15mm × 2.82mm)

T_{JMAX} = 125°C, $\theta_{JCbottom}$ = 2-3°C/W, θ_{JA} = 15°C/W, θ_{JCtop} = 25°C/W, θ Values Determined Using a 4-Layer 95mm × 76mm PCB, Weight = 1.7g

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE (Note 2)
LTM4614EV#PBF	LTM4614EV#PBF	LTM4614V	144-Lead (15mm × 15mm × 2.82mm) LGA	–40°C to 125°C
LTM4614IV#PBF	LTM4614IV#PBF	LTM4614V	144-Lead (15mm × 15mm × 2.82mm) LGA	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C. V_{IN} = 5V unless otherwise noted. Refer to Figure 1. Specified as each channel (Note 5).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(DC)}$	Input DC Voltage		●	2.375		5.5	V
$V_{OUT(DC)}$	Output Voltage	C_{IN} = 22µF, C_{OUT} = 100µF, R_{FB} = 5.76k V_{IN} = 2.375V to 5.5V, I_{OUT} = 0A to 4A (Note 4) 0°C ≤ T_J ≤ 125°C	 ●	 1.460 1.45	 1.49 1.49	 1.508 1.512	 V V
$V_{IN(UVLO)}$	Undervoltage Lockout Threshold	I_{OUT} = 0A		1.6	2	2.3	V
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	I_{OUT} = 0A, C_{IN} = 22µF, C_{OUT} = 100µF, V_{OUT} = 1.5V V_{IN} = 5.5V			0.35		A
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 2.375V, V_{OUT} = 1.5V, Switching Continuous V_{IN} = 5.5V, V_{OUT} = 1.5V, Switching Continuous Shutdown, RUN = 0, V_{IN} = 5V			20 35 7	 12	mA mA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C. V_{IN} = 5V unless otherwise noted. Refer to Figure 1. Specified as each channel (Note 5).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 2.375V, V_{OUT} = 1.5V, I_{OUT} = 4A V_{IN} = 5.5V, V_{OUT} = 1.5V, I_{OUT} = 4A			3.15 1.35		A A
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 3.3V, V_{OUT} = 1.5V (Note 4)		0		4	A
$\frac{\Delta V_{OUT(LINE)}}{V_{OUT}}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} from 2.375V to 5.5V, I_{OUT} = 0A	●		0.1	0.3	%
$\frac{\Delta V_{OUT(LOAD)}}{V_{OUT}}$	Load Regulation Accuracy	V_{OUT} = 1.5V, 0A to 4A (Note 4), V_{IN} = 2.375V to 5.5V 0°C ≤ T_J ≤ 125°C	 ●		0.7 1.2	1.25 1.5	% %
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF (X5R) V_{IN} = 5V, V_{OUT} = 1.5V			12		mV_{P-P}
f_s	Output Ripple Voltage Frequency	I_{OUT} = 4A, V_{IN} = 5V, V_{OUT} = 1.5V			1.25		MHz
$\Delta V_{OUT(START)}$	Turn-On Overshoot	C_{OUT} = 100µF, V_{OUT} = 1.5V, RUN/SS = 10nF, I_{OUT} = 0A V_{IN} = 3.3V V_{IN} = 5V			 20 20		 mV mV
t_{START}	Turn-On Time	C_{OUT} = 100µF, V_{OUT} = 1.5V, I_{OUT} = 1A Resistive Load, TRACK = V_{IN} and RUN/SS = Float V_{IN} = 5V			 0.5		 ms
$\Delta V_{OUT(LS)}$	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF, V_{IN} = 5V, V_{OUT} = 1.5V			25		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, V_{IN} = 5V, V_{OUT} = 1.5V			10		µs
$I_{OUT(PK)}$	Output Current Limit	C_{OUT} = 100µF V_{IN} = 5V, V_{OUT} = 1.5V			 8		 A
V_{FB}	Voltage at FB Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	 ●	0.792 0.788	0.8 0.8	0.808 0.810	V V
I_{FB}					0.2		µA
V_{RUN}	RUN Pin On/Off Threshold			0.6	0.75	0.9	V
I_{TRACK}	TRACK Pin Current				0.2		µA
$V_{TRACK(OFFSET)}$	Offset Voltage	TRACK = 0.4V			30		mV
$V_{TRACK(RANGE)}$	Tracking Input Range			0		0.8	V
R_{FBHI}	Resistor Between V_{OUT} and FB Pins			4.96	4.99	5.025	kΩ
ΔV_{PGOOD}	PGOOD Range				±7.5		%
R_{PGOOD}	PGOOD Resistance	Open-Drain Pull-Down			90	150	Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4614 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4614E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4614I is guaranteed to meet specifications over the full internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

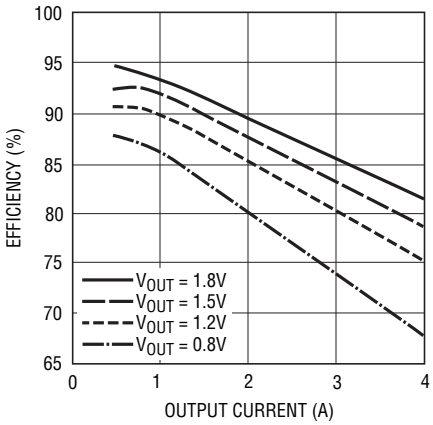
Note 3: The IC has overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 125°C when overtemperature is activated. Continuous overtemperature activation can impair long-term reliability.

Note 4: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

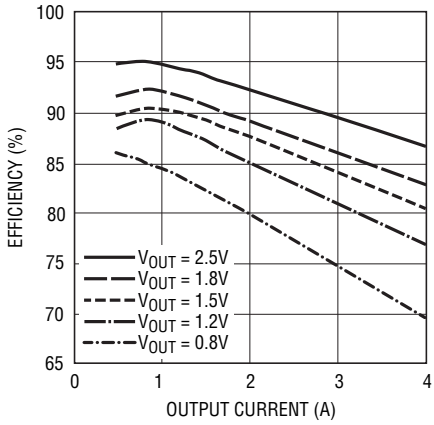
Note 5: Two channels are tested separately and the specified test conditions are applied to each channel.

TYPICAL PERFORMANCE CHARACTERISTICS

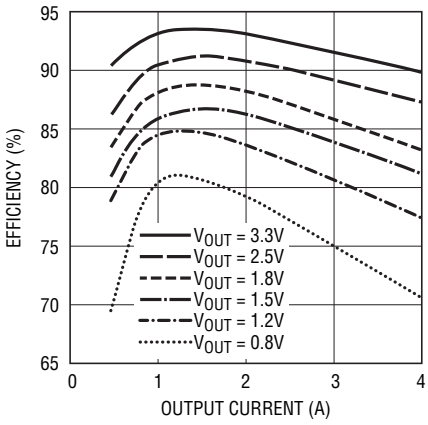
Efficiency vs Output Current V_{IN} = 2.5V



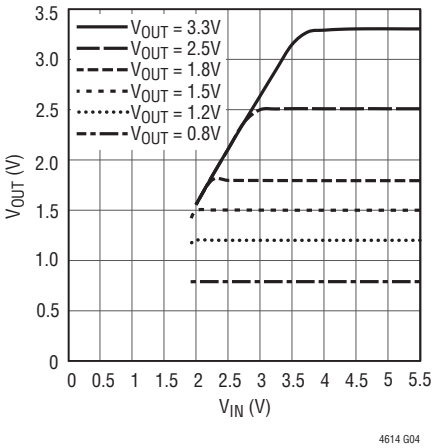
Efficiency vs Output Current V_{IN} = 3.3V



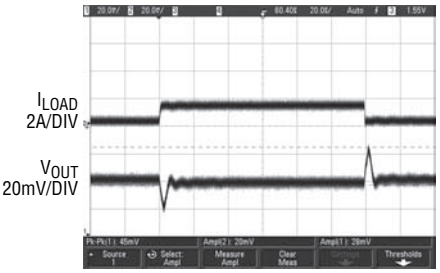
Efficiency vs Output Current V_{IN} = 5V



Minimum Input Voltage at 4A Load

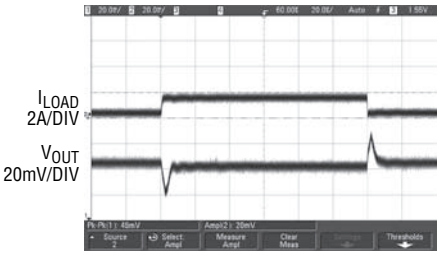


Load Transient Response



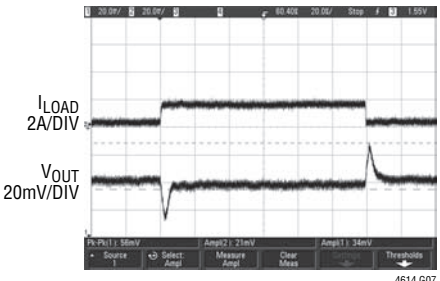
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.2V
C_{OUT} = 100µF, 6.3V CERAMICS

Load Transient Response



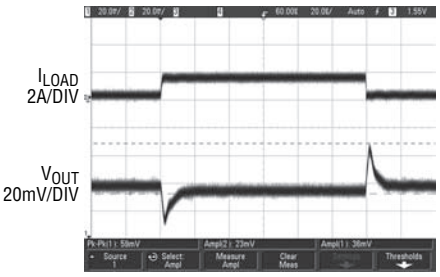
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.5V
C_{OUT} = 100µF, 6.3V CERAMICS

Load Transient Response



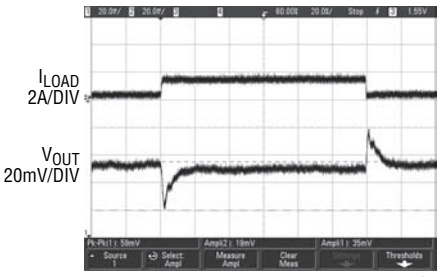
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.8V
C_{OUT} = 100µF, 6.3V CERAMICS

Load Transient Response



V_{IN} = 5V 20µs/DIV
V_{OUT} = 2.5V
C_{OUT} = 100µF, 6.3V CERAMICS

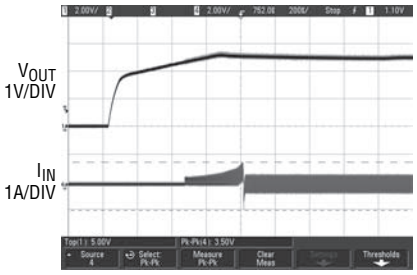
Load Transient Response



V_{IN} = 5V 20µs/DIV
V_{OUT} = 3.3V
C_{OUT} = 100µF, 6.3V CERAMICS

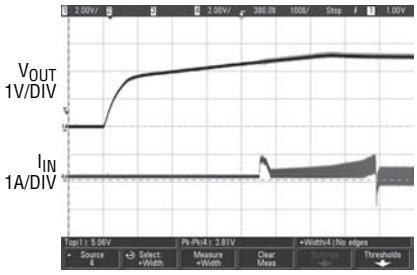
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up



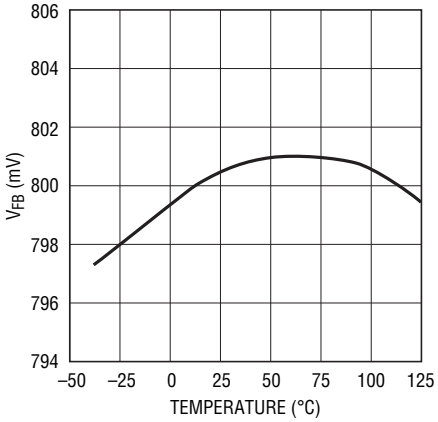
V_{IN} = 5V 200µs/DIV
V_{OUT} = 2.5V
C_{OUT} = 100µF
NO LOAD
(0.01µF SOFT-START CAPACITOR)

Start-Up

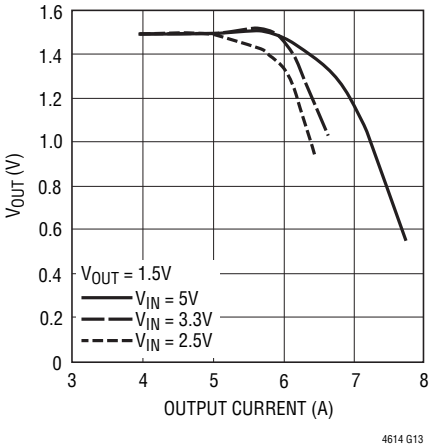


V_{IN} = 5V 200µs/DIV
V_{OUT} = 2.5V
C_{OUT} = 100µF
4A LOAD
(0.01µF SOFT-START CAPACITOR)

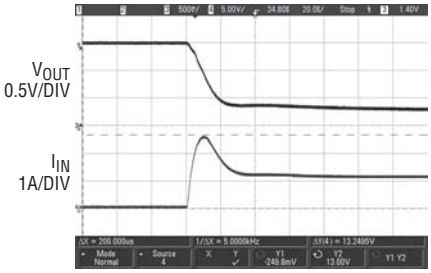
V_{FB} vs Temperature



Current Limit Foldback

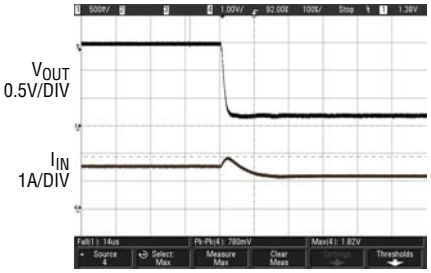


Short-Circuit Protection
1.5V Short, No Load



20µs/DIV

Short-Circuit Protection
1.5V Short, 4A Load



100µs/DIV

PIN FUNCTIONS

V_{IN1}, V_{IN2} (J1-J6, K1-K6); (C1-C6, D1-D6): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

V_{OUT1}, V_{OUT2} (J9-J12, K9-K12, L9-L12, M9-M12); (C9-C12, D9-D12, E9-E12, F9-F12): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 4.

GND1, GND2, (G1-G12, H1, H7-H12, J7-J8, K7-K8, L1, L7-L8, M1-M8); (A1-A12, B1, B7-B12, C7-C8, D7-D8, E1, E7-E8, F1-F8): Power Ground Pins for Both Input and Output Returns.

TRACK1, TRACK2 (L3, E3): Output Voltage Tracking Pins. When the module is configured as a master output, then a soft-start capacitor is placed on the RUN/SS pin to ground to control the master ramp rate, or an external ramp can be applied to the master regulator's track pin to control it.

PIN FUNCTIONS

Slave operation is performed by putting a resistor divider from the master output to the ground, and connecting the center point of the divider to this pin on the slave regulator. If tracking is not desired, then connect the TRACK pin to V_{IN}. Load current must be present for tracking. See the Applications Information section.

FB1, FB2 (L6, E6): The Negative Input of the Switching Regulators' Error Amplifier. Internally, these pins are connected to V_{OUT} with a 4.99k precision resistor. Different output voltages can be programmed with an externally connected resistor between the FB and GND pins. Two power modules can current share when this pin is connected in parallel with the adjacent module's FB pin. See the Applications Information section.

COMP1, COMP2 (L5, E5): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Two power modules can current share when this pin is connected in parallel with the adjacent module's COMP pin. Each channel has been internally compensated. See the Applications Information section.

PGOOD1, PGOOD2 (L4, E4): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±7.5% of the regulation point.

RUN/SS1, RUN/SS2 (L2, E2): Run Control and Soft-Start Pins. A voltage above 0.9V will turn on the module, and below 0.6V will turn off the module. This pin has a 1M resistor to V_{IN} and a 1000pF capacitor to GND. The voltage on the RUN/SS pin clamps the control loop's current comparator threshold. A RUN/SS pin voltage of 2.375V upon completion of soft-start guarantees the regulator can deliver full output current. To turn off the module while V_{IN} remains active, the RUN/SS pin should be pulled low with a falling edge ≤ 1µs to ensure the device does not transition slowly through the internal undervoltage lockout threshold. See Applications Information section for soft-start information.

SW1, SW2 (H2-H6, B2-B6): The switching node of the circuit is used for testing purposes. This can be connected to copper on the board for improved thermal performance.

SIMPLIFIED BLOCK DIAGRAM

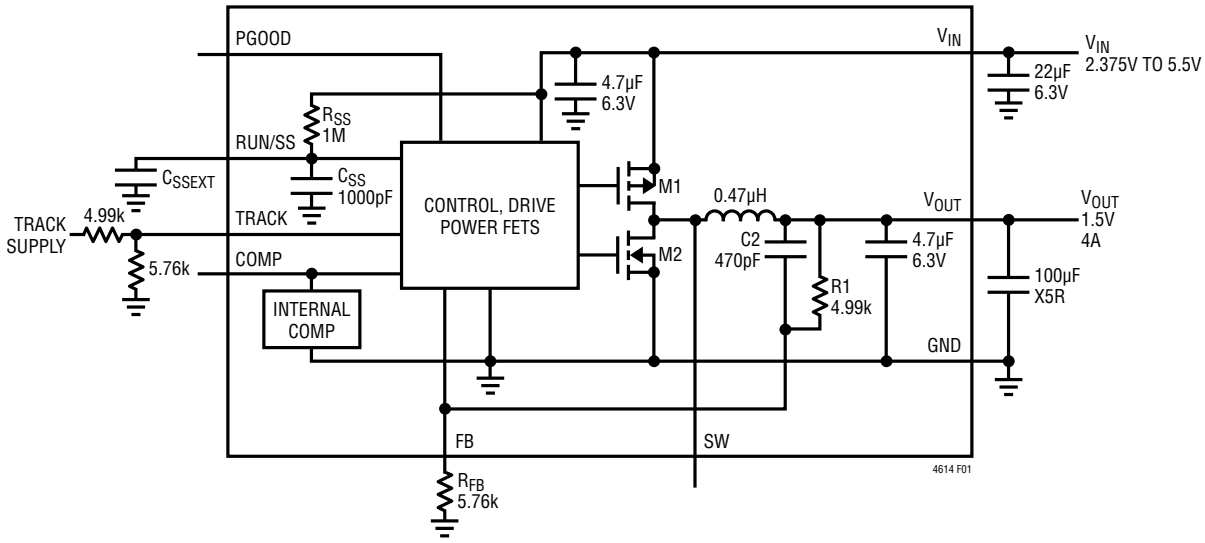


Figure 1. Simplified LTM4614 Block Diagram of Each Switching Regulator Channel

DECOUPLING REQUIREMENTS T_A = 25°C. Use Figure 1 configuration for each channel.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 2.375V to 5.5V, V_{OUT} = 1.5V)	I_{OUT} = 4A		22		µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 2.375V to 5.5V, V_{OUT} = 1.5V)	I_{OUT} = 4A		100		µF

OPERATION

LTM4614 POWER MODULE DESCRIPTION

The LTM4614 is a standalone dual nonisolated switching mode DC/DC power supply. It can deliver up to 4A of DC output current for each channel with few external input and output capacitors. This module provides two precisely regulated output voltages programmable via one external resistor for each channel from 0.8V DC to 5V DC over a 2.375V to 5.5V input voltage. The typical application schematic is shown in Figure 12.

The LTM4614 has two integrated constant frequency current mode regulators, with built-in power MOSFETs with fast switching speed. The typical switching frequency is 1.25MHz. With current mode control and internal feedback loop compensation, these switching regulators have sufficient stability margins and good transient performance under a wide range of operating conditions and with a wide range of output capacitors, even all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit. Besides, current limiting is provided in an overcurrent condition with thermal shutdown. In addition, internal overvoltage and undervoltage comparators pull the open-drain PGOOD outputs low if the particular output feedback voltage exits a ±7.5% window around the regulation point. Furthermore, in an overvoltage condition, internal top FET, M1, is turned off and bottom FET, M2, is turned on and held on until the overvoltage condition clears, or current limit is exceeded.

Pulling each specific RUN pin below 0.8V forces the specific regulator controller into its shutdown state, turning off both M1 and M2 for each power stage. At low load current, each regulator works in continuous current mode by default to achieve minimum output voltage ripple.

The TRACK and RUN/SS pins are used for power supply tracking and soft-start programming for each specific regulator. See the Applications Information section.

The LTM4614 is internally compensated to be stable over the operating conditions. Table 4 provides a guideline for input and output capacitance for several operating conditions. The LTpowerCAD™ GUI is available for transient and stability analysis.

The FB pins are used to program the specific output voltage with a single externally connected resistor to ground.

APPLICATIONS INFORMATION

Dual Switching Regulator

A typical LTM4614 application circuit is shown in Figure 12. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 4 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio than can be achieved for a given input voltage on the two switching regulators. The LTM4614 is 100% duty cycle capable, but the V_{IN} to V_{OUT} minimum dropout will be a function the load current. A typical 0.5V minimum is sufficient. See Typical Performance Characteristics.

Output Voltage Programming

Each regulator channel has an internal 0.8V reference voltage. As shown in the Block Diagram, a 4.99k internal feedback resistor connects the V_{OUT} and FB pins together. The output voltage will default to 0.8V with no externally applied feedback resistor. Adding a resistor R_{FB} from the FB pin to GND programs the output voltage:

$$V_{OUT} = 0.8V \bullet \frac{4.99k + R_{FB}}{R_{FB}}$$

Table 1. FB Resistor Table vs Various Output Voltages

V_{OUT}	0.8V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V
R_{FB}	Open	20k	10k	5.76k	3.92k	2.37k	1.62k

Input Capacitors

The LTM4614 module should be connected to a low AC impedance DC source. One 4.7µF ceramic capacitor is included inside the module for each regulator channel. Additional input capacitors are needed if a large load step is required up to the full 4A level and for RMS ripple current requirements. A 47µF bulk capacitor can be used for more input bulk capacitance. This 47µF capacitor is only needed if the input source impedance is compromised by long inductive leads or traces.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

In the above equation, η% is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated aluminum electrolytic OS-CON or polymer capacitor. If a low inductance plane is used to power the device, then no input capacitance is required. The internal 4.7µF ceramics on each channel input are typically rated for 1A of RMS ripple current up to 85°C operation. The worst-case ripple current for the 4A maximum current is 2A or less. An additional 10µF or 22µF local ceramic capacitor can be used to supplement the internal capacitor with an additional 1A to 2A ripple current rating. See Figure 11 for recommended PCB layout.

Output Capacitors

The LTM4614 switchers are designed for low output voltage ripple on each channel. The bulk output capacitors are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. The output capacitors can be low ESR tantalum capacitors, low ESR polymer capacitors or ceramic capacitors. The typical output capacitance range is 66µF to 100µF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. Table 4 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 2A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to maximize transient performance. See Figure 11 for recommended PCB layout.

APPLICATIONS INFORMATION

Fault Conditions: Current Limit and Overcurrent Foldback

The LTM4614 has current mode control, which inherently limits the cycle-by-cycle inductor current not only in steady-state operation, but also in transient.

Along with foldback current limiting in the event of an overload condition, the LTM4614 has overtemperature shutdown protection that inhibits switching operation around 150°C for each channel.

Run Enable and Soft-Start

The RUN/SS pins provide a dual function of enable and soft-start control for each channel. The RUN/SS pins are used to control turn on of the LTM4614. While each enable pin is below 0.6V, the LTM4614 will be in a low quiescent current state. At least a 0.9V level applied to the enable pins will turn on the LTM4614 regulators. The voltage on the RUN/SS pins clamp the control loop's current comparator threshold. A RUN/SS pin voltage of 2.375V upon completion of soft-start guarantees the regulator can deliver full output current. These pins can be used to sequence the regulator channels. Soft-start control is provided by a 1M pull-up resistor (R_{SS}) and a 1000pF capacitor (C_{SS}) as shown in the Block Diagram for each channel. Optionally, an external capacitor (C_{SSEXT}) can be applied to the RUN/SS pin to increase soft-start time. A typical value is 0.01µF. Soft-start time is approximately given by:

$$t_{SOFTSTART} = \ln\left(\frac{V_{IN}}{V_{IN}-1.8V}\right) \bullet R_{SS} \bullet (C_{SS} + C_{SSEXT})$$

where R_{SS} and C_{SS} are shown in the Block Diagram of Figure 1, and 1.8V is the soft-start upper range. The soft-start function can also be used to control the output ramp-up time, so that another regulator can be easily tracked to it. To turn off the module while V_{IN} remains active, the RUN/SS pin should be pulled low with a falling edge ≤ 1µs to ensure the device does not transition slowly through the internal undervoltage lockout threshold.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK pins. Either output can be tracked up or down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. The LTM4614 uses a very accurate 4.99k resistor for the internal top feedback resistor. Figure 2 shows an example of coincident tracking.

Equations:

$$TRACK1 = \left(\frac{R_{FB1}}{4.99k + R_{FB1}}\right) \bullet Master$$

$$Slave = \left(1 + \frac{4.99k}{R_{FB1}}\right) \bullet TRACK1$$

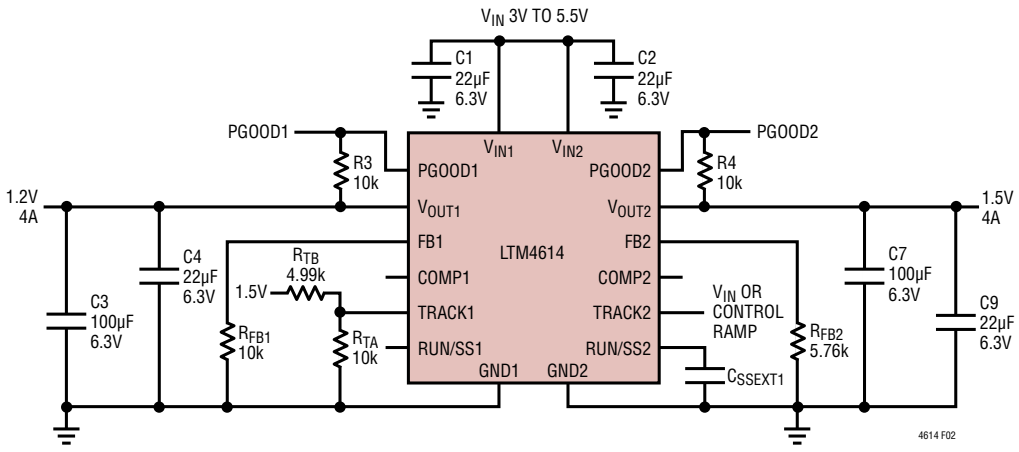


Figure 2. Dual Outputs (1.5V and 1.2V) with Tracking

APPLICATIONS INFORMATION

TRACK1 is the track ramp applied to the slave's track pin. TRACK1 applies the track reference for the slave output up to the point of the programmed value at which TRACK1 proceeds beyond the 0.8V reference value. The TRACK1 pin must go beyond the 0.8V to ensure the slave output has reached its final value.

Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the master's TRACK pin. As mentioned above, the TRACK pin has a control range from 0V to 0.8V. The control ramp slew rate applied to the master's TRACK pin is directly equal to the master's output slew rate in Volts/Time.

The equation:

$$\frac{MR}{SR} \bullet 4.99k = R_{TB}$$

where MR is the master's output slew rate and SR is the slave's output slew rate in Volts/Time. When coincident tracking is desired, then MR and SR are equal, thus R_{TB} is equal to 4.99k. R_{TA} is derived from equation:

$$R_{TA} = \frac{0.8V}{\frac{V_{FB}}{4.99k} + \frac{V_{FB}}{R_{FB}} - \frac{V_{TRACK}}{R_{TB}}}$$

where V_{FB} is the feedback voltage reference of the regulator, and V_{TRACK} is 0.8V. Since R_{TB} is equal to the 4.99k top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then R_{TA} is equal to R_{FB} with $V_{FB} = V_{TRACK}$. Therefore R_{TB} = 4.99k and R_{TA} = 10k in Figure 2. Figure 3 shows the output voltage tracking waveform for coincident tracking.

In ratiometric tracking, a different slew rate maybe desired for the slave regulator. R_{TB} can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach it final value before the master output.

For example, MR = 2.5V/ms and SR = 1.8V/1ms. Then R_{TB} = 6.98k. Solve for R_{TA} to equal to 3.24k. The master output must be greater than the slave output for the tracking to work. Output load current must be present for tracking to operate properly during power down.

Power Good

PGOOD1 and PGOOD2 are open-drain pins that can be used to monitor valid output voltage regulation. These pins monitor a ±7.5% window around the regulation point.

COMP Pin

This pin is the external compensation pin. The module has already been internally compensated for all output voltages. Table 4 is provided for most application requirements. The LTpowerCAD GUI is available for other control loop optimization.

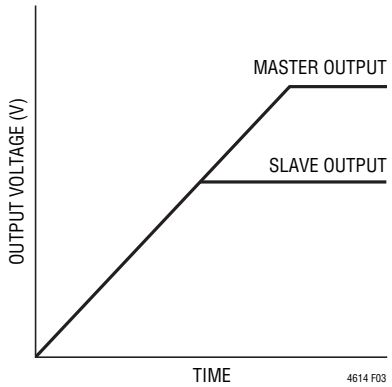


Figure 3. Output Voltage Coincident Tracking

APPLICATIONS INFORMATION

Parallel Switching Regulator Operation

The LTM4614 switching regulators are inherently current mode control. Paralleling will have very good current sharing. This will balance the thermals on the design. Figure 13 shows a schematic of a parallel design. The voltage feedback equation changes with the variable N as channels are paralleled.

The equation:

$$V_{OUT} = 0.8V \bullet \frac{\frac{4.99k}{N} + R_{FB}}{R_{FB}}$$

N is the number of paralleled channels.

Thermal Considerations and Output Current Derating

The power loss curves in Figures 5 and 6 can be used in coordination with the load current derating curves in Figures 7 to 10 for calculating an approximate θ_{JA} thermal resistance for the LTM4614 with various heat sinking and airflow conditions. Both of the LTM4614 outputs are at full 4A load current, and the power loss curves in Figures 5 and 6 are combined power losses plotted for both output voltages up to 4A each. The 4A output voltages are 1.2V and 3.3V. These voltages are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The junctions are maintained at ~120°C while lowering output current or power while increasing ambient temperature. The 120°C is chosen to allow for a 5°C margin window relative to the maximum 125°C. The decreased output current will decrease the internal module loss as ambient temperature is increased. The power loss curves in Figures 5 and 6 show this amount of power loss as a function of load current that is specified for both channels. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much

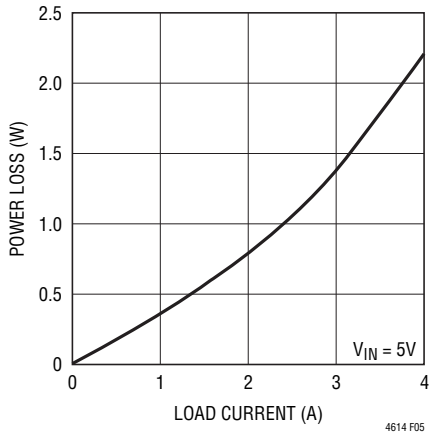


Figure 5. 1.2V Power Loss

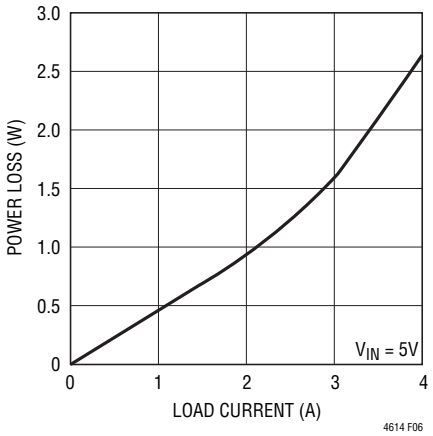


Figure 6. 3.3V Power Loss

APPLICATIONS INFORMATION

module temperature rise can be allowed. As an example, in Figure 7 the load current is derated to 3A for each channel with 0LFM at ~ 90°C and the total combined power loss for both channels at 5V to 1.2V at 3A output is ~1.5 watts. If the 90°C ambient temperature is subtracted from the 120°C maximum junction temperature, then the difference of 30°C divided by 1.5W equals a 20°C/W thermal resistance. Table 2 specifies a 15°C/W value which is close. Table 2 and Table 3 provide equivalent thermal resistances for 1.2V and 3.3V outputs with and without air flow and heat sinking. The combined power loss for the two 4A outputs can be summed together and multiplied by the thermal resistance values in Tables 2 and 3 for module temperature rise under the specified conditions. The printed circuit board is a 1.6mm thick four layer board with 2 ounce copper for the two outer layers and 1 ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm. The data sheet lists the θ_{JA} (junction to ambient) and θ_{JC} (junction to case) thermal resistances under the Pin Configuration diagram.

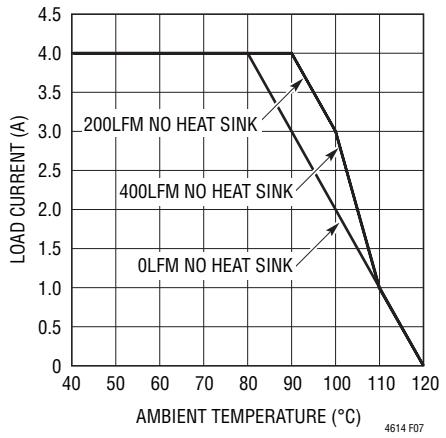


Figure 7. 1.2V No Heat Sink (V_{IN} = 5V)

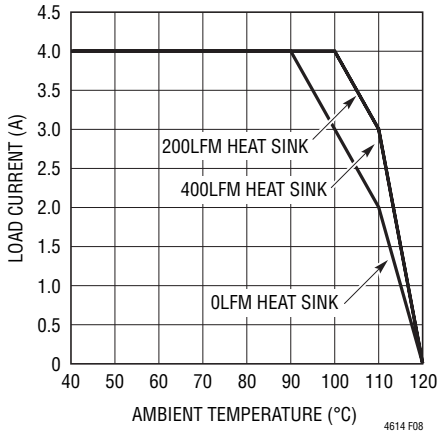


Figure 8. 1.2V Heat Sink (V_{IN} = 5V)

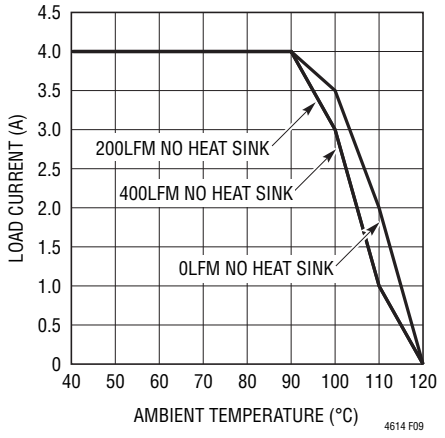


Figure 9. 3.3V No Heat Sink (V_{IN} = 5V)

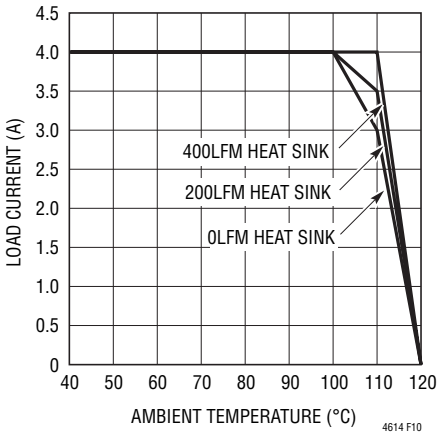


Figure 10. 3.3V Heat Sink (V_{IN} = 5V)

APPLICATIONS INFORMATION

Table 2. 1.2V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 7	5	Figure 5	0	None	15
Figure 7	5	Figure 5	200	None	12
Figure 7	5	Figure 5	400	None	10
Figure 8	5	Figure 5	0	BGA Heat Sink	12
Figure 8	5	Figure 5	200	BGA Heat Sink	9
Figure 8	5	Figure 5	400	BGA Heat Sink	7

Table 3. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 9	5	Figure 6	0	None	15
Figure 9	5	Figure 6	200	None	12
Figure 9	5	Figure 6	400	None	10
Figure 10	5	Figure 6	0	BGA Heat Sink	12
Figure 10	5	Figure 6	200	BGA Heat Sink	9
Figure 10	5	Figure 6	400	BGA Heat Sink	7

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Aavid Thermalloy	375424b00034G	www.aavid.com

APPLICATIONS INFORMATION

Safety Considerations

The LTM4614 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

Layout Checklist/Example

The high integration of LTM4614 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Refer to http://www.linear.com/docs/29812 for device land pattern and stencil design.
- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between the top layer and other power layers.
- Do not put vias directly on pads unless they are capped.

Figure 11 gives a good example of the recommended layout.

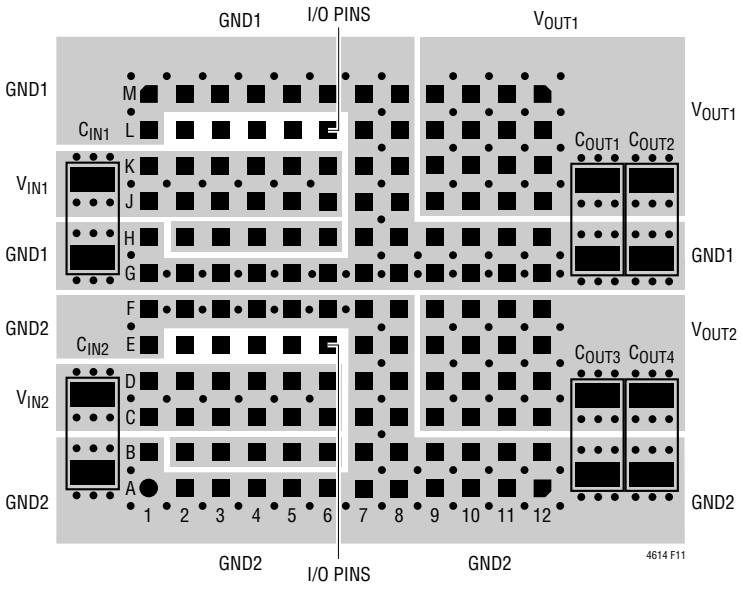


Figure 11. Recommended PCB Layout

APPLICATIONS INFORMATION

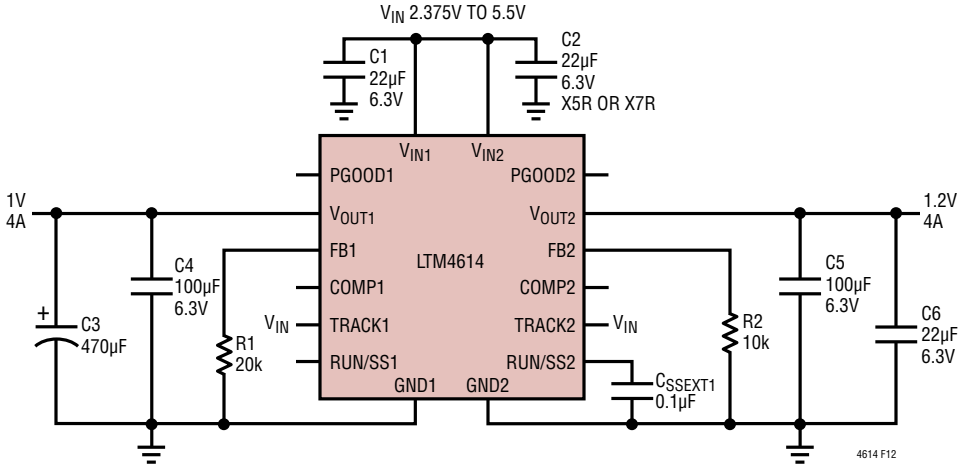


Figure 12. Typical 2.375V_{IN} to 5.5V_{IN}, 1.2V and 1V at 4A

Table 4. Output Voltage Response vs Component Matrix (Refer to Figure 12) 0A to 2.5A Load Step Typical Measured Values

C_{OUT1} AND C_{OUT2} CERAMIC VENDORS	VALUE	PART NUMBER	C_{OUT1} AND C_{OUT2} BULK VENDORS	VALUE	PART NUMBER
TDK	22µF 6.3V	C3216X7SOJ226M	Sanyo POSCAP	150µF 10V	10TPD150M
Murata	22µF 16V	GRM31CR61C226KE15L	Sanyo POSCAP	220µF 4V	4TPE220MF
TDK	100µF 6.3V	C4532X5R0J107MZ	**C_{IN} BULK VENDORS**	**VALUE**	**PART NUMBER**
Murata	100µF 6.3V	GRM32ER60J107M	SUNCON	100µF 10V	10CE100FH

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)*	C_{OUT1} AND C_{OUT2} (CER) EACH	C_{OUT1} AND C_{OUT2} (POSCAP) EACH	I_{TH}	V_{IN} (V)	DROOP (mV)	PEAK-TO-PEAK DEVIATION	RECOVERY TIME (µs)	LOAD STEP (A/µs)	R_{FB} (kΩ)
1.2	10µF ×2	100µF	100µF, 22µF ×2	None	None	5	33	68	11	2.5	10
1.2	10µF ×2	100µF	22µF ×1	220µF	None	5	25	50	9	2.5	10
1.2	10µF ×2	100µF	100µF, 22µF ×2	None	None	3.3	33	68	8	2.5	10
1.2	10µF ×2	100µF	22µF ×1	220µF	None	3.3	25	50	10	2.5	10
1.5	10µF ×2	100µF	100µF, 22µF ×2	None	None	5	30	60	11	2.5	5.76
1.5	10µF ×2	100µF	22µF ×1	220µF	None	5	28	60	11	2.5	5.76
1.5	10µF ×2	100µF	100µF, 22µF ×2	None	None	3.3	30	60	10	2.5	5.76
1.5	10µF ×2	100µF	22µF ×1	220µF	None	3.3	27	56	10	2.5	5.76
1.8	10µF ×2	100µF	100µF, 22µF ×2	None	None	5	34	68	12	2.5	3.92
1.8	10µF ×2	100µF	22µF ×1	220µF	None	5	30	60	12	2.5	3.92
1.8	10µF ×2	100µF	22µF ×1	220µF	None	3.3	30	60	12	2.5	3.92
2.5	10µF ×2	None	22µF ×1	None	None	5	50	90	10	2.5	2.37
2.5	10µF ×2	100µF	22µF ×1	150µF	None	5	33	60	10	2.5	2.37
2.5	10µF ×2	100µF	22µF ×1	150µF	None	3.3	50	95	12	2.5	2.37
3.3	10µF ×2	100µF	22µF ×1	150µF	None	5	50	90	12	2.5	1.62

*Bulk capacitance is optional if V_{IN} has very low input impedance.

APPLICATIONS INFORMATION

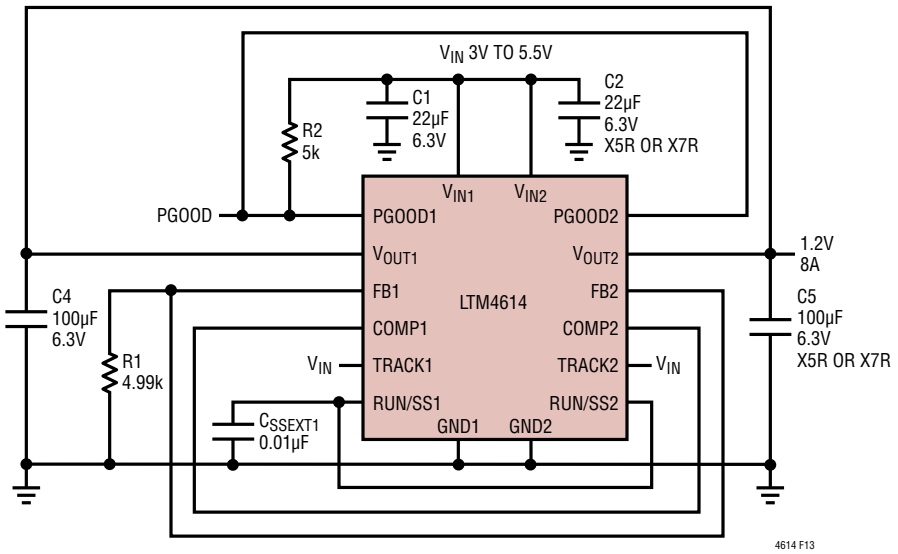


Figure 13. LTM4614 Parallel 1.2V at 8A Design (Also, See the LTM4608A)

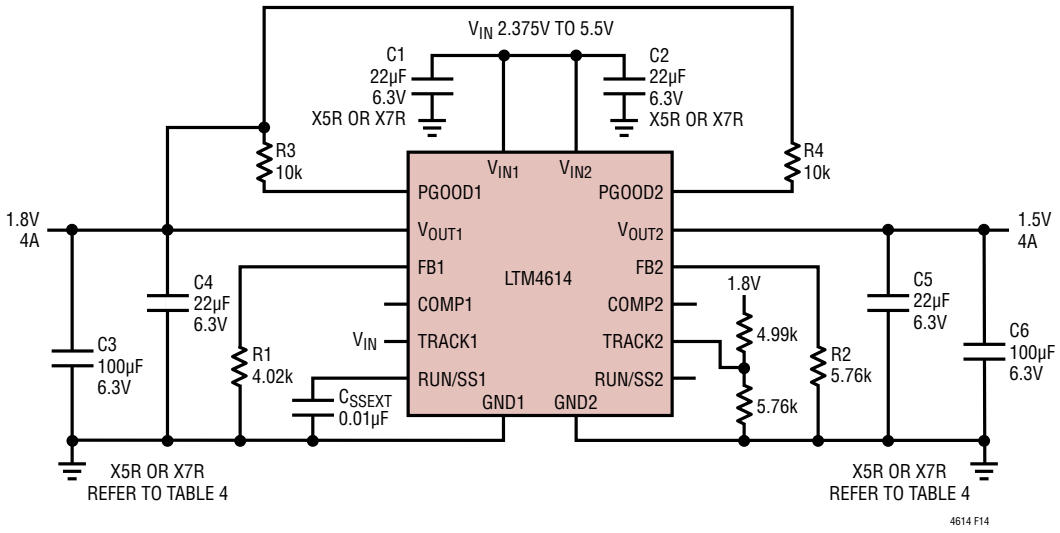
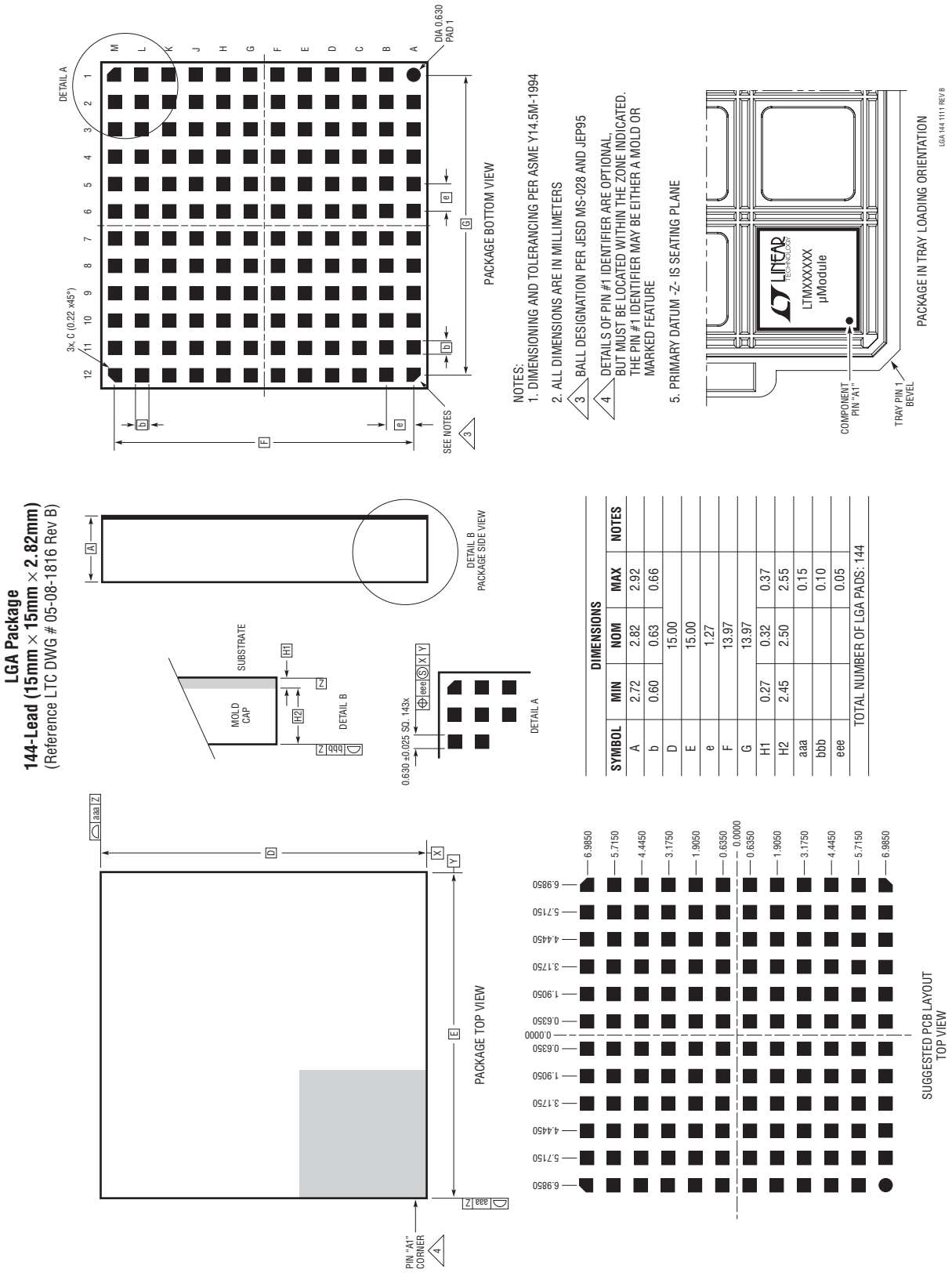


Figure 14. 1.8V and 1.5V at 4A with Output Voltage Tracking Design

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.72	2.82	2.92	
b	0.60	0.63	0.66	
D		15.00		
E		15.00		
e		1.27		
F		13.97		
G		13.97		
H1	0.27	0.32	0.37	
H2	2.45	2.50	2.55	
aaa			0.15	
bbb			0.10	
eee			0.05	

PACKAGE DESCRIPTION

LTM4614 Component LGA Pinout

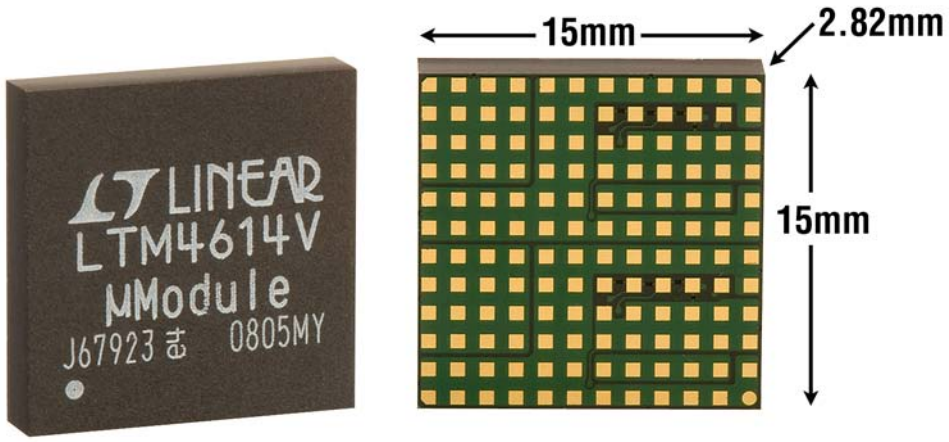
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GND2	B1	GND2	C1	V_{IN2}	D1	V_{IN2}	E1	GND2	F1	GND2
A2	GND2	B2	SW2	C2	V_{IN2}	D2	V_{IN2}	E2	RUN/SS2	F2	GND2
A3	GND2	B3	SW2	C3	V_{IN2}	D3	V_{IN2}	E3	TRACK2	F3	GND2
A4	GND2	B4	SW2	C4	V_{IN2}	D4	V_{IN2}	E4	PGOOD2	F4	GND2
A5	GND2	B5	SW2	C5	V_{IN2}	D5	V_{IN2}	E5	COMP2	F5	GND2
A6	GND2	B6	SW2	C6	V_{IN2}	D6	V_{IN2}	E6	FB2	F6	GND2
A7	GND2	B7	GND2	C7	GND2	D7	GND2	E7	GND2	F7	GND2
A8	GND2	B8	GND2	C8	GND2	D8	GND2	E8	GND2	F8	GND2
A9	GND2	B9	GND2	C9	V_{OUT2}	D9	V_{OUT2}	E9	V_{OUT2}	F9	V_{OUT2}
A10	GND2	B10	GND2	C10	V_{OUT2}	D10	V_{OUT2}	E10	V_{OUT2}	F10	V_{OUT2}
A11	GND2	B11	GND2	C11	V_{OUT2}	D11	V_{OUT2}	E11	V_{OUT2}	F11	V_{OUT2}
A12	GND2	B12	GND2	C12	V_{OUT2}	D12	V_{OUT2}	E12	V_{OUT2}	F12	V_{OUT2}

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND1	H1	GND1	J1	V_{IN1}	K1	V_{IN1}	L1	GND1	M1	GND1
G2	GND1	H2	SW1	J2	V_{IN1}	K2	V_{IN1}	L2	RUN/SS1	M2	GND1
G3	GND1	H3	SW1	J3	V_{IN1}	K3	V_{IN1}	L3	TRACK1	M3	GND1
G4	GND1	H4	SW1	J4	V_{IN1}	K4	V_{IN1}	L4	PGOOD1	M4	GND1
G5	GND1	H5	SW1	J5	V_{IN1}	K5	V_{IN1}	L5	COMP1	M5	GND1
G6	GND1	H6	SW1	J6	V_{IN1}	K6	V_{IN1}	L6	FB1	M6	GND1
G7	GND1	H7	GND1	J7	GND1	K7	GND1	L7	GND1	M7	GND1
G8	GND1	H8	GND1	J8	GND1	K8	GND1	L8	GND1	M8	GND1
G9	GND1	H9	GND1	J9	V_{OUT1}	K9	V_{OUT1}	L9	V_{OUT1}	M9	V_{OUT1}
G10	GND1	H10	GND1	J10	V_{OUT1}	K10	V_{OUT1}	L10	V_{OUT1}	M10	V_{OUT1}
G11	GND1	H11	GND1	J11	V_{OUT1}	K11	V_{OUT1}	L11	V_{OUT1}	M11	V_{OUT1}
G12	GND1	H12	GND1	J12	V_{OUT1}	K12	V_{OUT1}	L12	V_{OUT1}	M12	V_{OUT1}

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	08/12	Update Pin Configuration drawing.	2
		Remove reference to obsolete Application Note.	3
		Correct typical performance curves.	4 and 5
		Clarify RUN/SS and FB Pin Function information.	6
		Update Block Diagram.	6
		Clarify RUN/SS Applications Information.	9
		Correct feedback resistor value.	15

PACKAGE PHOTOGRAPH



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC®2900	Quad Supply Monitor with Adjustable Reset Timer	Monitors Four Supplies, Adjustable Reset Timer
LTC2923	Power Supply Tracking Controller	Tracks Both Up and Down, Power Supply Sequencing
LTM4600HV	10A DC/DC µModule Regulator	$4.5V \le V_{IN} \le 28V$, $0.6V \le V_{OUT} \le 5V$, LGA Package
LTM4600HVMP	Wide Temperature Range 10A DC/DC µModule Regulator	Guaranteed Operation from –55°C to 125°C Ambient, LGA Package
LTM4601A	12A DC/DC µModule Regulator with PLL, Output Tracking/Margining and Remote Sensing	Synchronizable PolyPhase® Operation, LTM4601-1/LTM4601A-1 Version Has No Remote Sensing, LGA Package
LTM4602	6A DC/DC µModule Regulator	Pin Compatible with the LTM4600, LGA Package
LTM4603	6A DC/DC µModule Regulator with PLL and Output Tracking/Margining and Remote Sensing	Synchronizable, PolyPhase Operation, LTM4603-1 Version Has No Remote Sensing, Pin Compatible with the LTM4601, LGA Package
LTM4604A	Low V_{IN} 4A DC/DC µModule Regulator	$2.375V \le V_{IN} \le 5.5V$, $0.8V \le V_{OUT} \le 5V$, 9mm × 15mm × 2.32mm LGA Package
LTM4605	5A to 12A Buck-Boost µModule Regulator	$4.5V \le V_{IN} \le 20V$, $0.8V \le V_{OUT} \le 16V$, 15mm × 15mm × 2.82mm LGA Package
LTM4607	5A to 12A Buck-Boost µModule Regulator	$4.5V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 25V$, 15mm × 15mm × 2.82mm LGA Package
LTM4608A	Low V_{IN} 8A DC/DC Step-Down µModule Regulator	$2.7V \le V_{IN} \le 5.5V$, $0.6V \le V_{OUT} \le 5V$, 9mm × 15mm × 2.82mm LGA Package
LTM4615	Triple Low V_{IN} DC/DC µModule Regulator	Two 4A Outputs and One 1.5A Output; 15mm × 15mm × 2.82mm
LTM4616	Dual 8A DC/DC µModule Regulator	Current Share Inputs or Outputs; 15mm × 15mm × 2.82mm
LTM8020	High V_{IN} 0.2A DC/DC Step-Down µModule Regulator	$4V \le V_{IN} \le 36V$, $1.25V \le V_{OUT} \le 5V$, 6.25mm × 6.25mm × 2.32mm LGA Package
LTM8021	High V_{IN} 0.5A DC/DC Step-Down µModule Regulator	$3V \le V_{IN} \le 36V$, $0.4V \le V_{OUT} \le 5V$, 6.25mm × 11.25mm × 2.82mm LGA Package
LTM8022	High V_{IN} 1A DC/DC Step-Down µModule Regulator	$3.6V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 10V$, 11.25mm × 9mm × 2.82mm LGA Package
LTM8023	High V_{IN} 2A DC/DC Step-Down µModule Regulator	$3.6V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 10V$, 11.25mm × 9mm × 2.82mm LGA Package

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