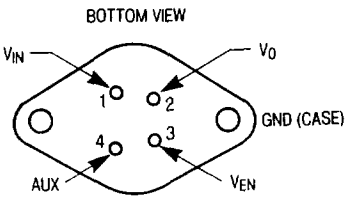
ABSOLUTE MAXIMUM RATINGS

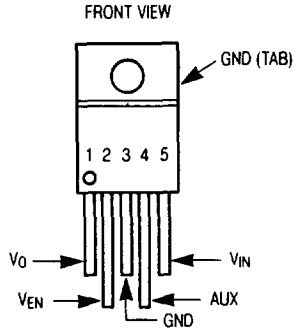
Power Dissipation ..... Internally Limited
Input Voltage (V_{IN}) 20V
Enable Voltage (V_{EN}) 20V
Operating Junction Temperature
LT1005M ..... −55°C to 150°C
LT1005C ..... 0°C to 125°C
Storage ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



4 LEAD TO-3

LT1005MK
LT1005CK



5 LEAD TO-220

LT1005CT

PRECONDITIONING:

100% Burn-in in thermal limit

ELECTRICAL CHARACTERISTICS — MAIN REGULATOR (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1005M MIN	LT1005M TYP	LT1005M MAX	LT1005C MIN	LT1005C TYP	LT1005C MAX	UNITS
V_O	Output Voltage	$T_j = 25°C$		4.9	5.0	5.1	4.9	5.0	5.1	V
	High	$7.4V \leq V_{IN} \leq 20V$ $P_d \leq 10W$ $0mA \leq I_O \leq 1A$	●	4.8	5.0	5.2	4.8	5.0	5.2	V
	Low	$7.2V \leq V_{IN} \leq 20V$ $I_O = 0$	●		0.1	0.3		0.1	0.3	V
$\frac{\Delta V_O}{\Delta I_O}$	Load Regulation	$7.5V \leq V_{IN} \leq 15V$ $0mA \leq I_O \leq 1A$ (Note 2)	●		5	25		5	25	mV
$\frac{\Delta V_O}{\Delta V_{IN}}$	Line Regulation	$7.4V \leq V_{IN} \leq 20V$ (Note 2)			0.3	2		0.3	2	mV/V
	Ripple Rejection	$50Hz \leq f \leq 500Hz$			66			66		dB
	Thermal Regulation	$\Delta P_d = 10W$ (Note 4)			0.005	0.02		0.005	0.02	%/W
I_O	Available Load Current	$7.4V \leq V_{IN} \leq 15V$ $V_{IN} = 20V$		1 0.7	1.7 1.3		1 0.7	1.7 1.0		A A
I_{SC}	Short Circuit Current	$7.0V \leq V_{IN} \leq 15V$ $V_{IN} = 20V$			1.5 1.2	2.5 2.0		1.5 1.2	2.5 2.0	A A
V_{IN}	Minimum Input Voltage to Maintain Regulation	(Note 5) $I_O = 0.2A$ $I_O = 1.0A$	 ● ●	 7.0 7.5	 6.5 7.0		 6.9 7.5	 6.5 7.0		 V V
I_Q	Quiescent Current	Output High Output Low			2 1.5	4 3		2 1.5	4 4	mA mA
Θ_{JC}	Thermal Resistance Junction to Case	TO-3 TO-220			3	4		3 3	4 5	°C/W °C/W

ELECTRICAL CHARACTERISTICS — AUXILIARY REGULATOR (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1005M MIN	LT1005M TYP	LT1005M MAX	LT1005C MIN	LT1005C TYP	LT1005C MAX	UNITS
V_O	Output Voltage	$T_j = 25°C$		4.9	5.0	5.1	4.9	5.0	5.1	V
		$7.0V \leq V_{IN} \leq 20V$ $0mA \leq I_O \leq 35mA$	●	4.8	5.0	5.2	4.8	5.0	5.2	V
$\frac{\Delta V_O}{\Delta I_O}$	Load Regulation	$7.0V \leq V_{IN} \leq 20V$ $0mA \leq I_O \leq 35mA$ (Note 2)	●		5	15		5	15	mV
$\frac{\Delta V_O}{\Delta V_{IN}}$	Line Regulation	$7.0V \leq V_{IN} \leq 20V$ (Note 2)			0.2	1		0.2	1	mV/V
	Ripple Rejection	$50Hz \leq f \leq 500Hz$			74			74		dB
I_{SC}	Short Circuit Current	$7.0V \leq V_{IN} \leq 20V$			90	150		90	150	mA
V_{IN}	Minimum Input Voltage to Maintain Regulation	(Note 5) $I_O = 1mA$ $I_O = 35mA$	 ● ●	 6.5 6.9	 6.1 6.5	 	 6.5 6.9	 6.1 6.5	 	 V V

4

ELECTRICAL CHARACTERISTICS — LOGIC CONTROL (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1005M MIN	LT1005M TYP	LT1005M MAX	LT1005C MIN	LT1005C TYP	LT1005C MAX	UNITS
V_{EN}	Enable Threshold Voltage	$7.0V \leq V_{IN} \leq 20V$ $T_j = 25°C$	 ●	 1.45 1.3	 1.6 1.6	 1.75 1.85	 1.45 1.3	 1.6 1.6	 1.75 1.85	 V V
	Enable Pin Current	$V_{EN} \leq 1V$ (See Note 3)		0		150	0		150	μA
		$V_{EN} \geq 2.4V$			0	1		0	1	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise indicated, these specifications apply for $V_{IN} = 10V$, $I_O = 0mA$, and $T_J = 25°C$.

Note 2: Line and load regulation are measured using a low duty cycle pulse, causing little change in the junction temperature. Effects due to thermal gradients and device heating must be taken into account separately.

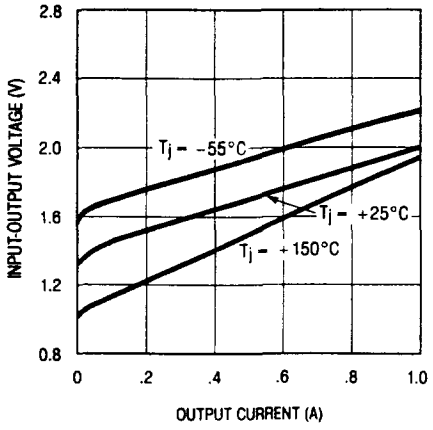
Note 3: When the enable pin is at a low logic level, current flows out of the enable pin.

Note 4: Pulse length for this measurement is 20msec.

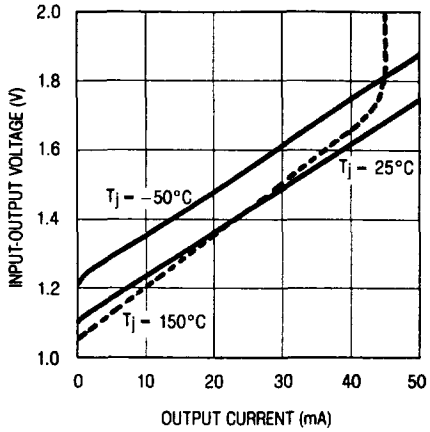
Note 5: Input Voltage is reduced until output drops by 100mV from its initial value.

TYPICAL PERFORMANCE CHARACTERISTICS

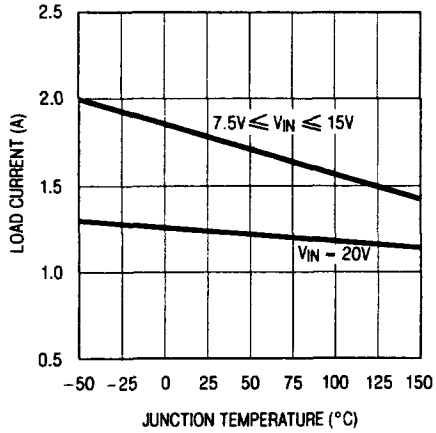
Minimum Input-Output Differential of Main Output



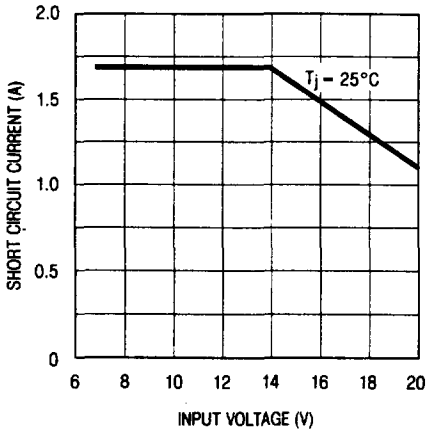
Minimum Input-Output Differential of Auxiliary Output



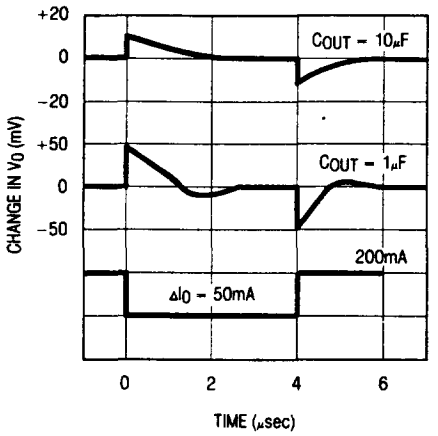
Maximum Available Load Current—Main Output



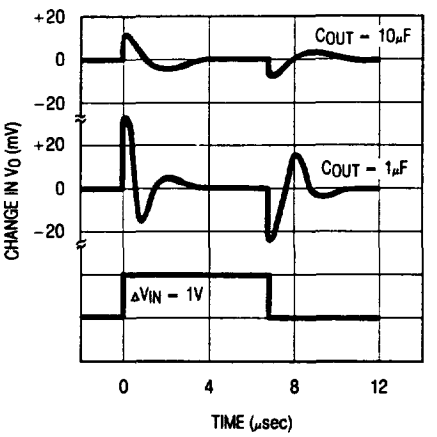
Short Circuit Output Current



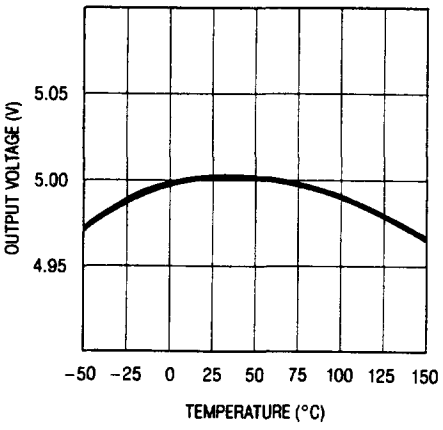
Load Transient Response of Main Output



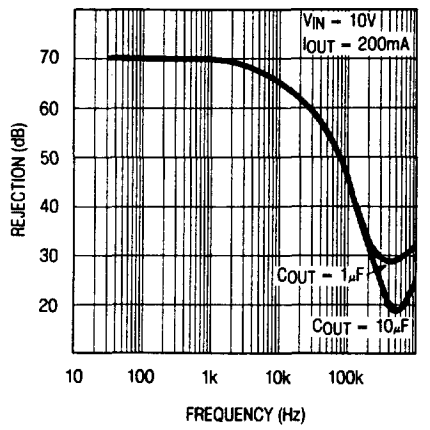
Line Transient Response of Main Output



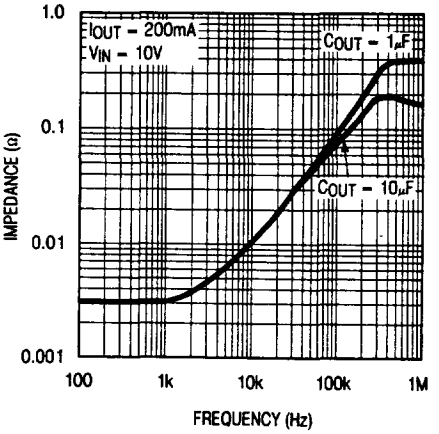
Output Voltage as Function of Temperature



Ripple Rejection

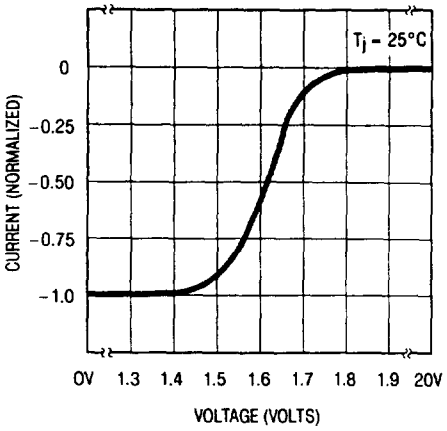


Output Impedance

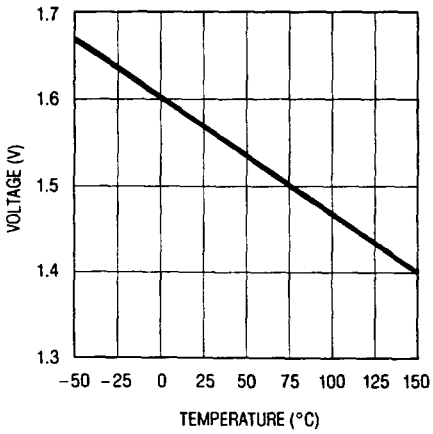


TYPICAL PERFORMANCE CHARACTERISTICS

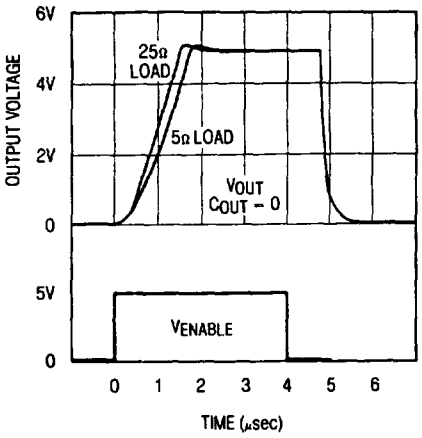
Enable Pin Characteristics



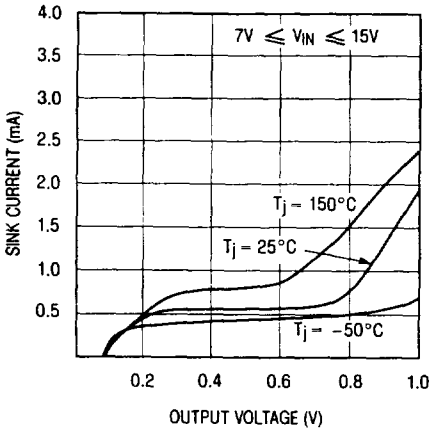
Enable Threshold



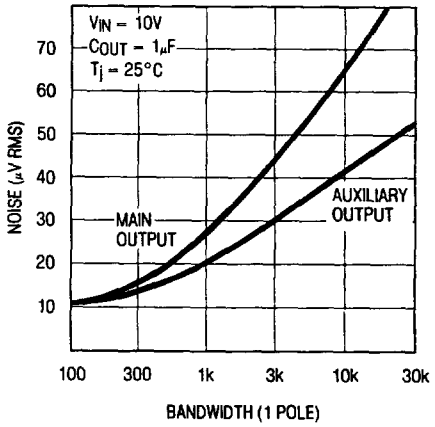
Switching Characteristics



Output Characteristics in Low State



Output Noise



4

APPLICATIONS INFORMATION

General Information

The LT1005 is a dual output 5V regulator. The main output is capable of delivering up to 1 amp of load current and can be shut down with a logic signal. The auxiliary output supplies a minimum of 35mA and is unaffected by the logic signal. The outputs are trimmed to ±2% initial tolerance and exhibit excellent line and load regulation.

The logic control feature makes the LT1005 ideal for many system applications where it is desirable to power up a portion of the system for a period of time and then power the system down during a standby operation. As an example, the LT1005 could be used to activate various memory space locations only as needed, thus saving substantial power dissipation and other cooling costs. The LT1005 could also be used to power micro-computers, such as the 8048 series. The auxiliary supply can be used for RAM keep-alive during power down operation. Additional power savings can be accomplished by using the LT1005 to power PROM, EPROM, and E^2PROM devices. During program load, or look-up table operations the ROM type device can be activated and its' contents placed in RAM, and then the ROM power can be removed. Or for high speed but low power data acquisition systems, the power could be applied to fast memory, then the data transferred to CMOS memory. The main regulator can then be shutdown and the CMOS memory can be powered by the auxiliary for lower power dissipation. Other applications, such as multiple power supply sequencing, elimination of expensive AC and DC power switches, delayed start applications, switching 5V DC loads, and many others are now easily accomplished.

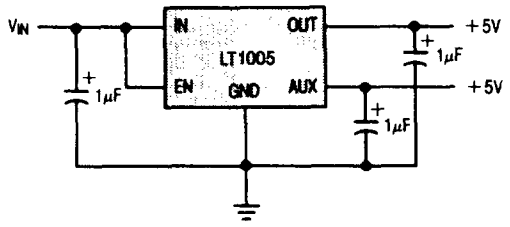
Timing functions can also be performed directly at the enable pin, such as delayed power-up or power-down.

Because a logic low on the enable pin shuts down the main regulator, feedback from output to enable can be used to generate hysterisis or latching functions.

The low quiescent current drain of the LT1005 makes it useful in battery powered or battery back-up applications. The enable pin can be used as a "low battery" detector or to shut down major portions of system power, allowing memory portions to continue to operate from the auxiliary output. At low output currents, the auxiliary output will regulate with input voltage typically as low as 6.1V, giving maximum battery life.

Good design practice with all regulators is to bypass the input and output terminals. A 1μF solid tantalum at the input and at both outputs is suggested. For the applications which follow, the bypass capacitors are still recommended, but are not shown on the diagram for simplicity. It is also recommended that for maximum noise immunity, the voltage enable pin be tied high if it is unused. It can be tied directly to V_{IN} as shown in Figure 1, or to the auxiliary output. If the enable pin is left open, it will float to a high logic level of approximately 1.6V and the main output regulator will be at 5V.

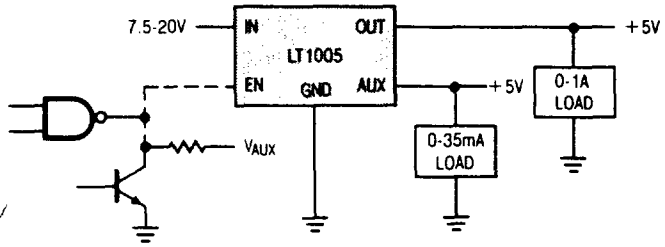
Figure 1.



The enable pin is fully protected against input voltages up to 20 volts, even if the power input voltage is zero.

The basic shutdown control circuit uses a direct gate drive or an open collector driver and a pull-up resistor which is tied to V_{AUX} as shown in Figure 2.

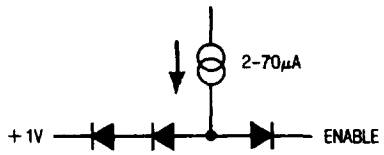
Figure 2.



Driving the Enable Pin

The enable pin equivalent schematic is shown in Fig. 3. Basically, enable pin current is zero above the threshold, and between 2 and 70μA below the threshold, flowing out of the pin. Standard logic, such as TTL & CMOS will interface directly to the enable pin, even if the logic output swing is higher than the input voltage (V_{IN}) to the regulator. 15V CMOS can be used to drive the enable pin even if the regulator is not powered up, without loading the CMOS output.

Figure 3.



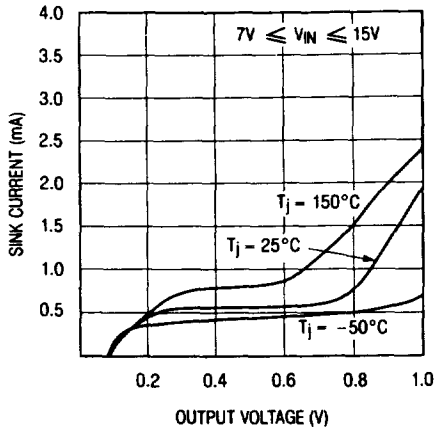
Timing functions, such as delayed power-up or power-down can be implemented by driving the enable pin with an RC network. The current flowing out of the enable pin should not be used as the timing current in delayed power up applications, as it is temperature sensitive and varies somewhat from device to device. Instead, a resistor tied to the auxiliary output, the input, or to a logic signal should be used. The timing resistor chosen should provide at least 500μA of current to "swamp-out" the effects of the internal current.

Main Output Current/Voltage Characteristics

Following a high to low transition at the enable pin, the main regulator output will begin to drop after a delay of approximately 1μsec. With no capacitive load, the output will fall to zero in approximately 0.5μsec (R_L = 5–100Ω). With a capacitive load, fall time is limited by the RC product of the load and the output capacitance. For light loads (R_L > 100Ω), the discharge time is controlled by an internal *equivalent* load of 200Ω for output voltages down to 1 volt. Below 1 volt, the output decays linearly, with a slope equivalent to the load capacitance and a pull down current of approximately 0.5mA. The DC output voltage in the shutdown mode is approximately 0.1 volt for input voltages (V_{IN}) up to 15V. If V_{IN} is 20V, the output during shutdown will be approximately 0.2V due to an internal current path in the regulator (see Figure 4).

Figure 4.

Output Characteristics in Low State



The user should note that the output in the low state can only sink about 0.5mA. If current is forced into the output, the output voltage will rise to 0.8V at 1mA and above 1V at 10mA. With no output capacitor, the rise time of the main output is about 1.5μs. With an output capacitor, rise time is limited by the short circuit current of the LT1005 and the load capacitance; $t_r \approx (C)(5V)/(1.5A)$. A 1μF output capacitor slows the output rise time to approximately 3μs and a 10μF output capacitor slows the output rise time to 30μs.

Output Current

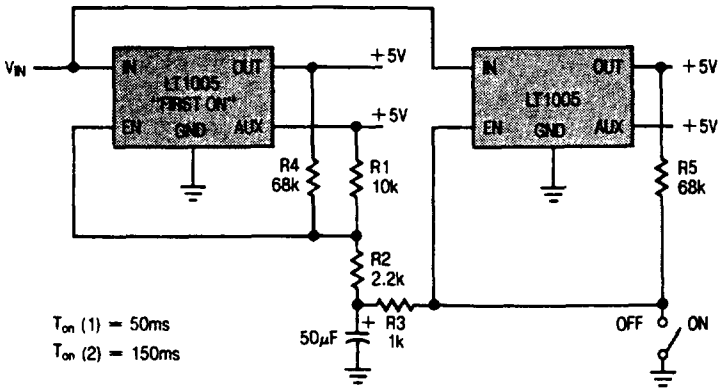
The main output current limits at about 1.7A for input voltages below 19V. Internal foldback, or "power limiting" circuitry detects the input-output voltage differential and reduces current limit for input to output voltages exceeding 14V. With 20V input, for instance, short circuit current is reduced to ≈ 1.1A.

An additional feature of the LT1005 is that the auxiliary supply does not incorporate nor is it affected by thermal shutdown. Any fault condition of the main regulator will not affect the auxiliary output voltage.

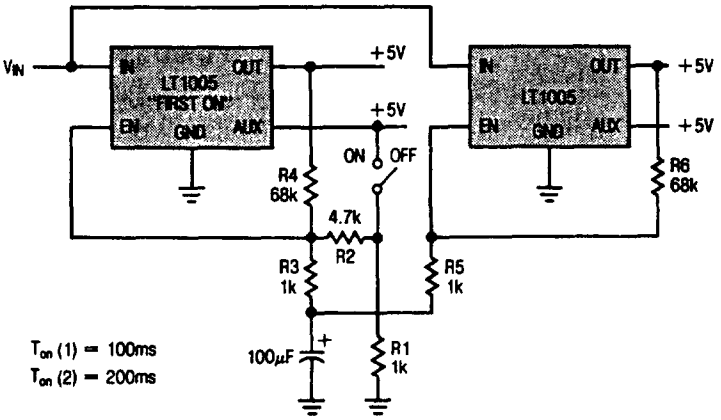
The following applications circuits will serve to indicate the versatility of the LT1005.

TYPICAL APPLICATIONS

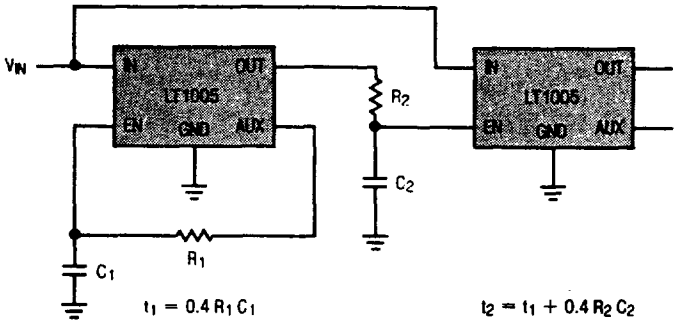
First-On, Last-Off Sequencing



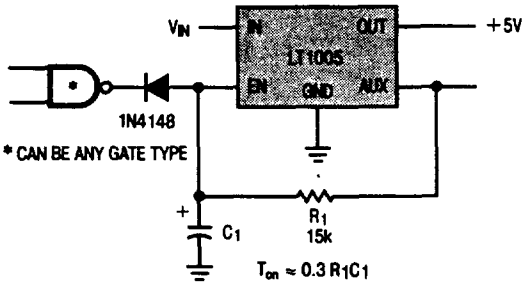
First-On, First-Off Sequencing



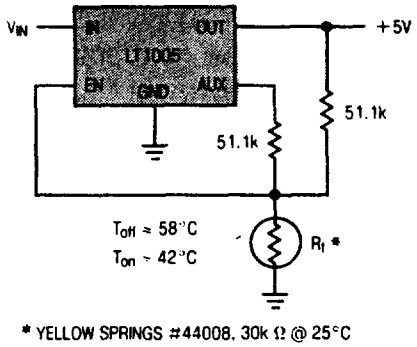
Power Supply Turn-On Sequencing



Fast Turn-Off, Delayed Turn-On

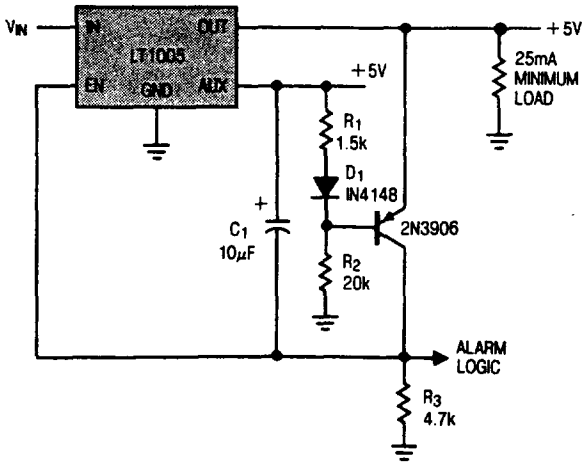


Thermal Cutoff at High Ambient Temperature



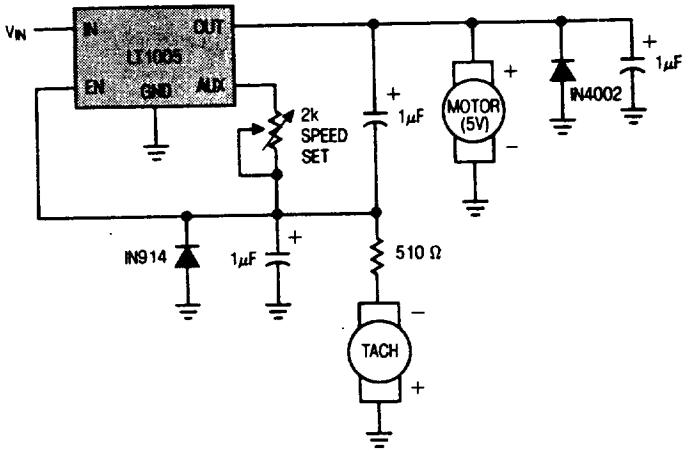
* YELLOW SPRINGS #44008, 30k Ω @ 25°C

Latch-Off for $V_{OUT} \leq 4.7V$

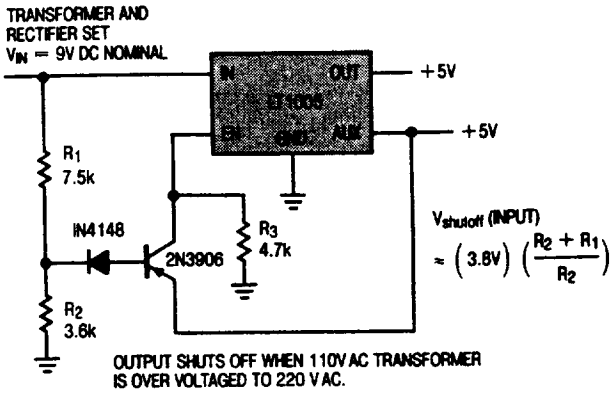


TYPICAL APPLICATIONS

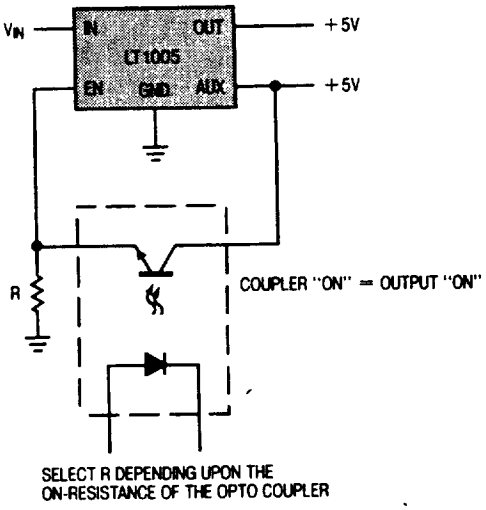
Proportional Motor Speed Controller



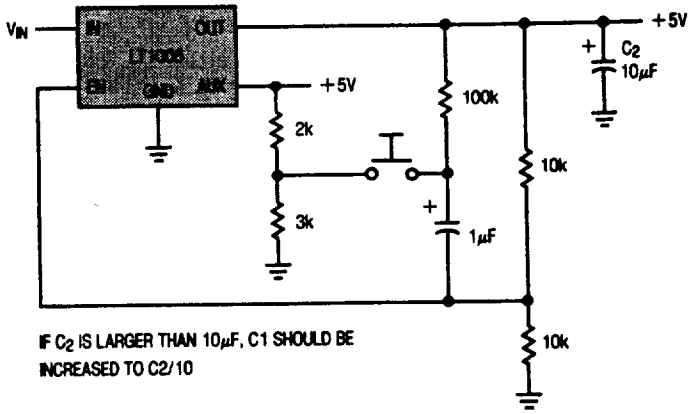
High Input Voltage Detection



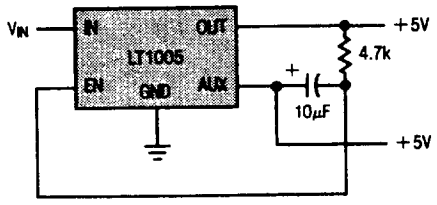
Opto-Coupled Output Control



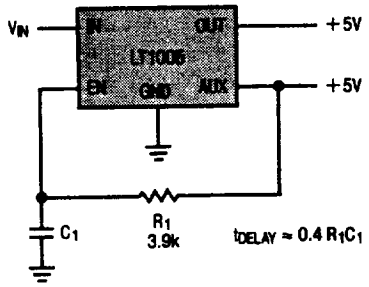
Push-On, Push-Off



Latch-Off When Output Short

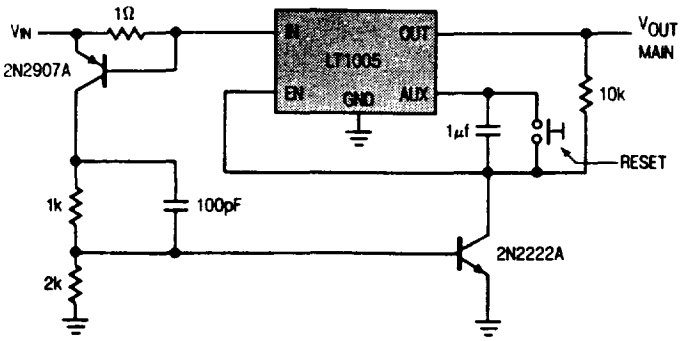


Delayed Power Up

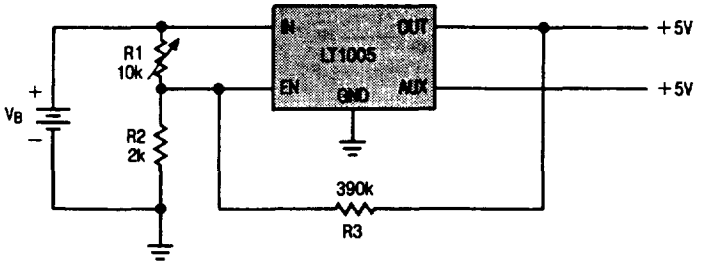


TYPICAL APPLICATIONS

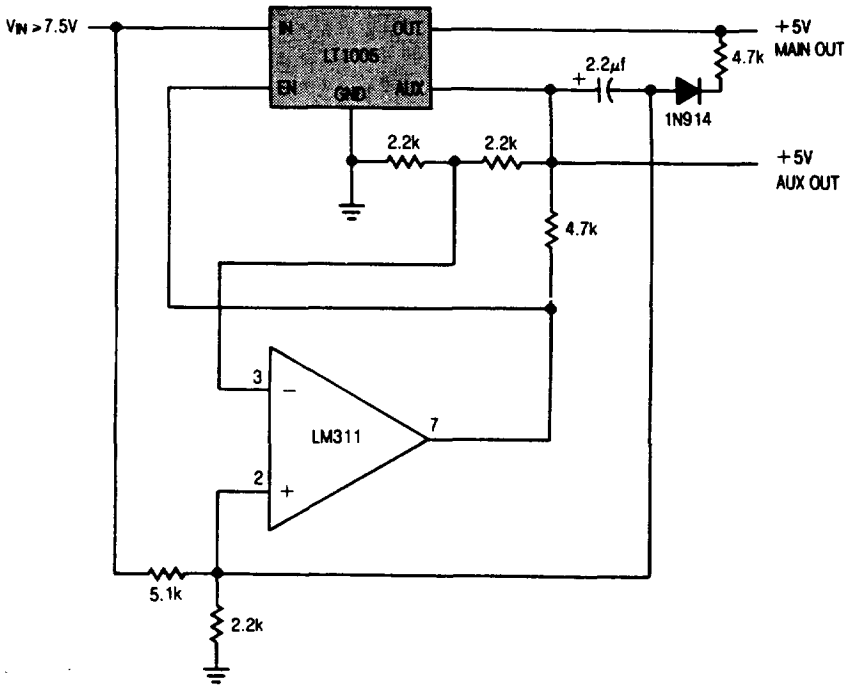
Fast Electronic Circuit Breaker



Battery Voltage Sensing Circuit



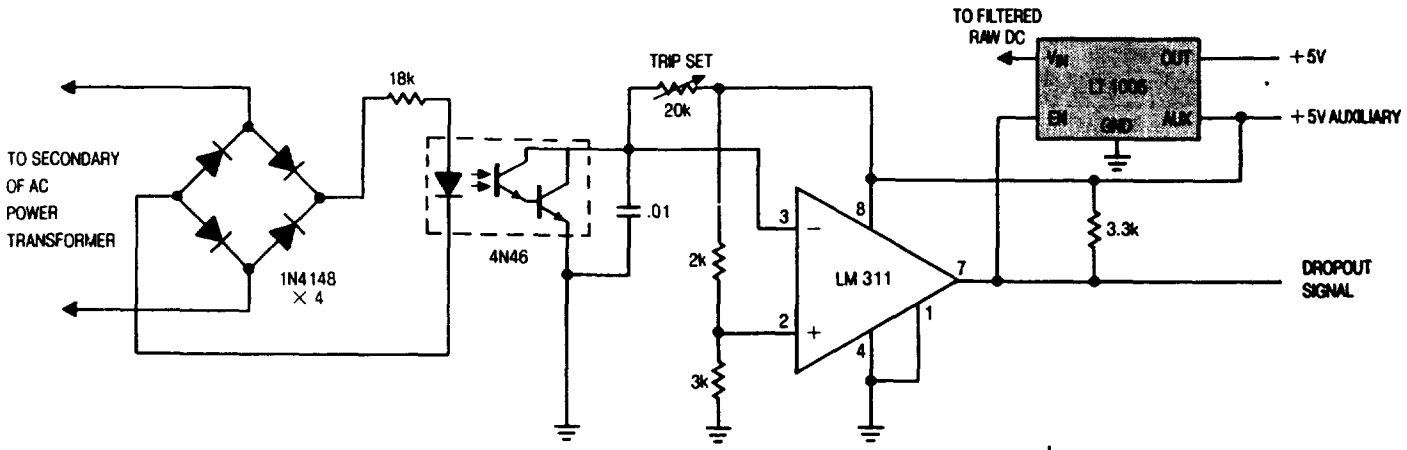
Memory Save-on-Power-Down



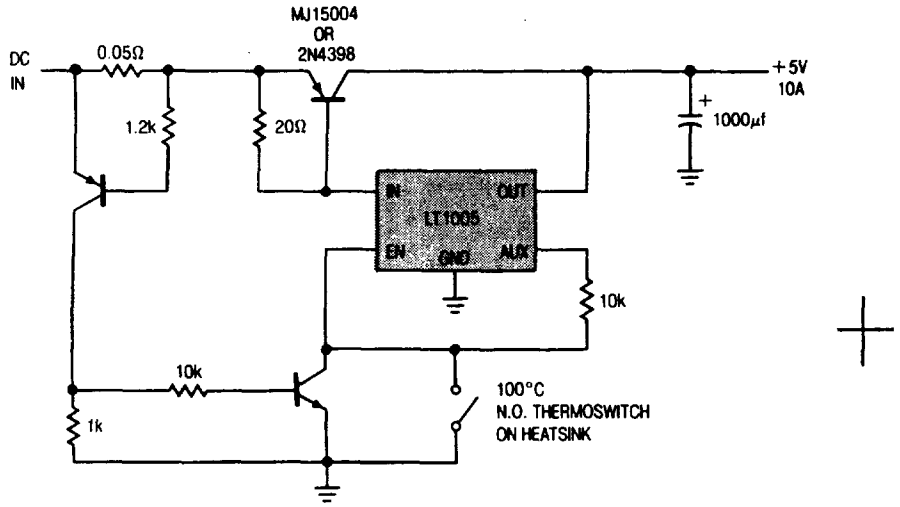
The auxiliary output powers the memory, while the main output powers the system and is connected to the memory store pin. When power goes down, the main output goes low, commanding the memory to store. The auxiliary output then drops out.

TYPICAL APPLICATIONS

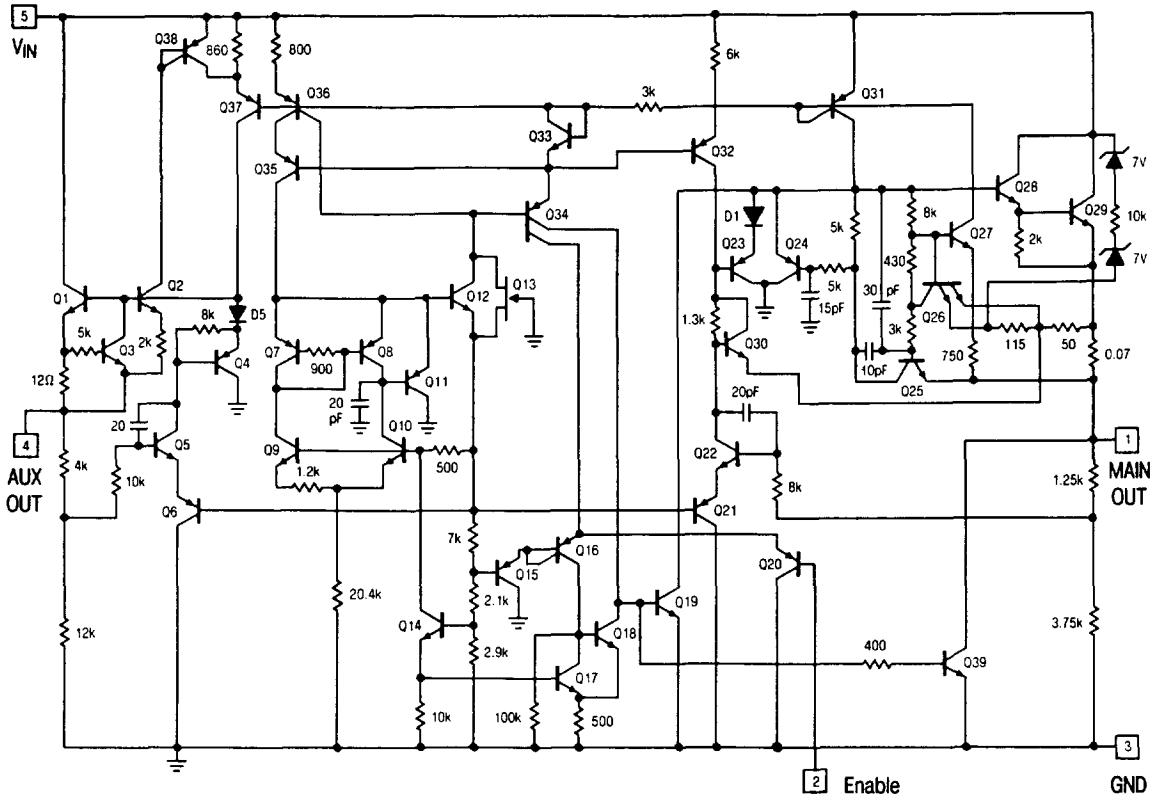
Line Dropout Detector



10 Amp Regulator with Current and Thermal Protection

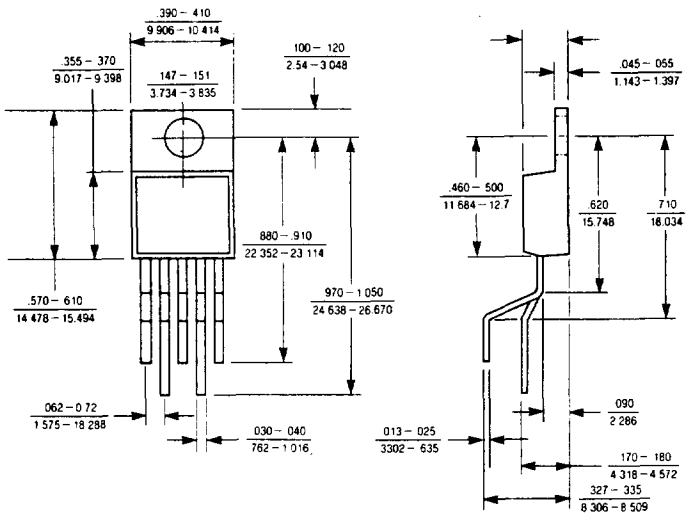


SCHEMATIC DIAGRAM



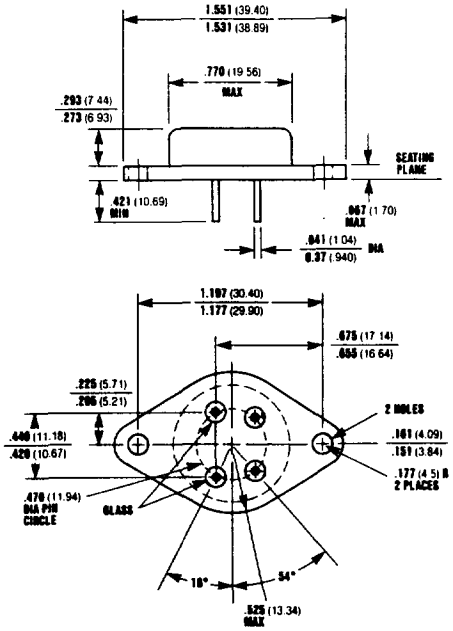
PACKAGE DESCRIPTION

TO-220 PACKAGE (5 LEAD)



	T_{JMAX}	Θ_{JC}
LT1005C	125°C	5°C/W

4-Pin Metal Package Similar to JEDEC TO-3



All dimensions in inches **bold** and millimeters (parentheses)

	T_{JMAX}	Θ_{JC}
LT1005M	150°C	4°C/W
LT1005C	125°C	4°C/W