

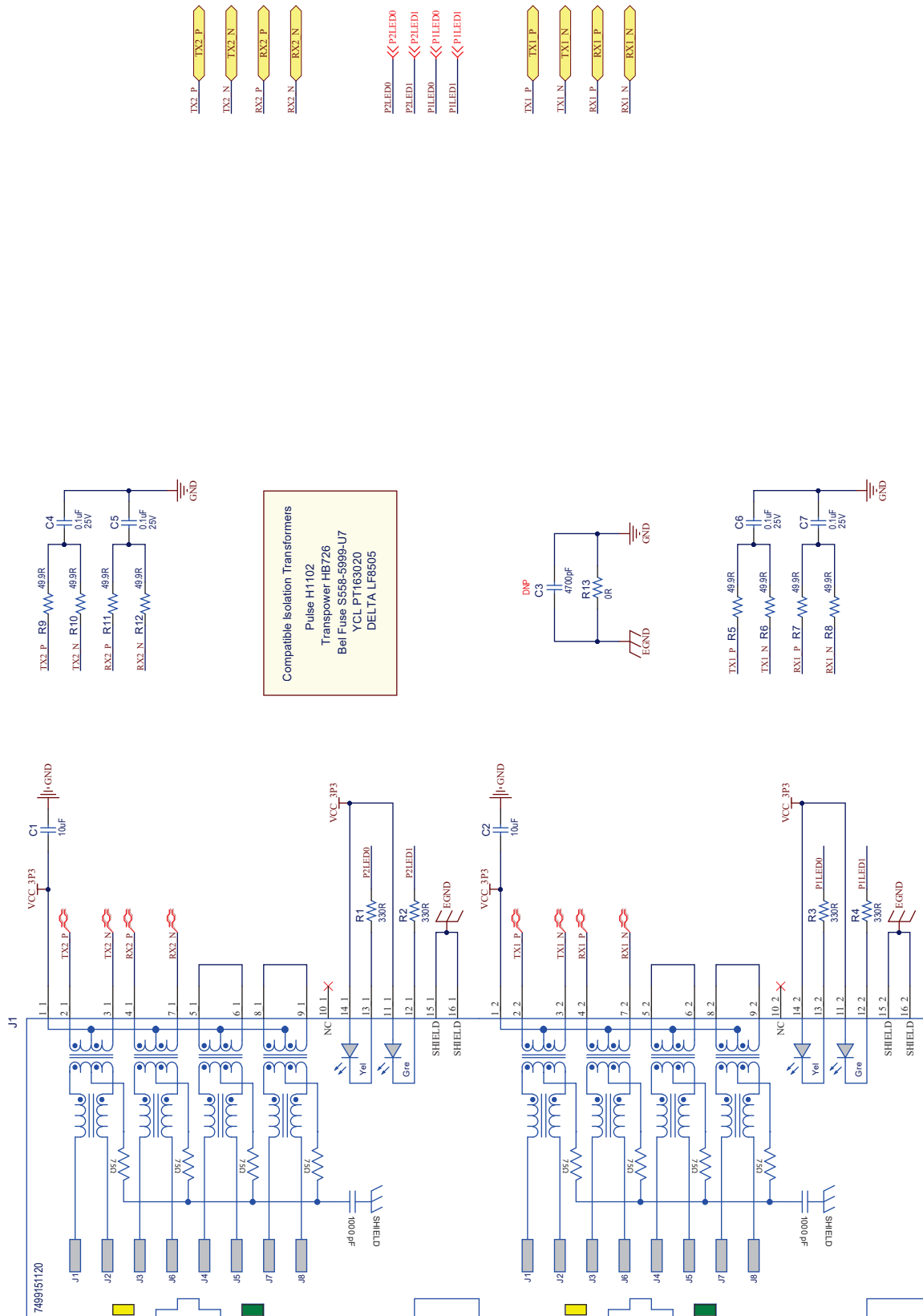
- Wireless LAN Access Point + Gateway
- Standalone 10/100 Switch

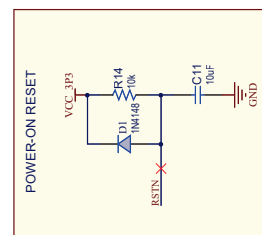
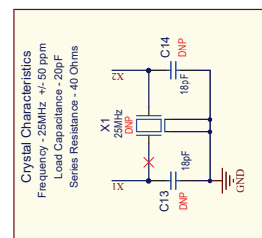
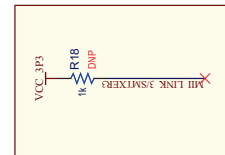
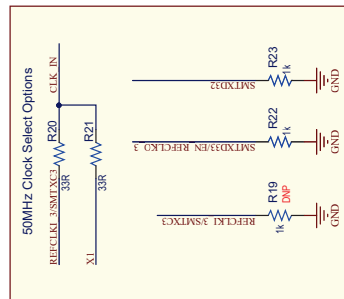
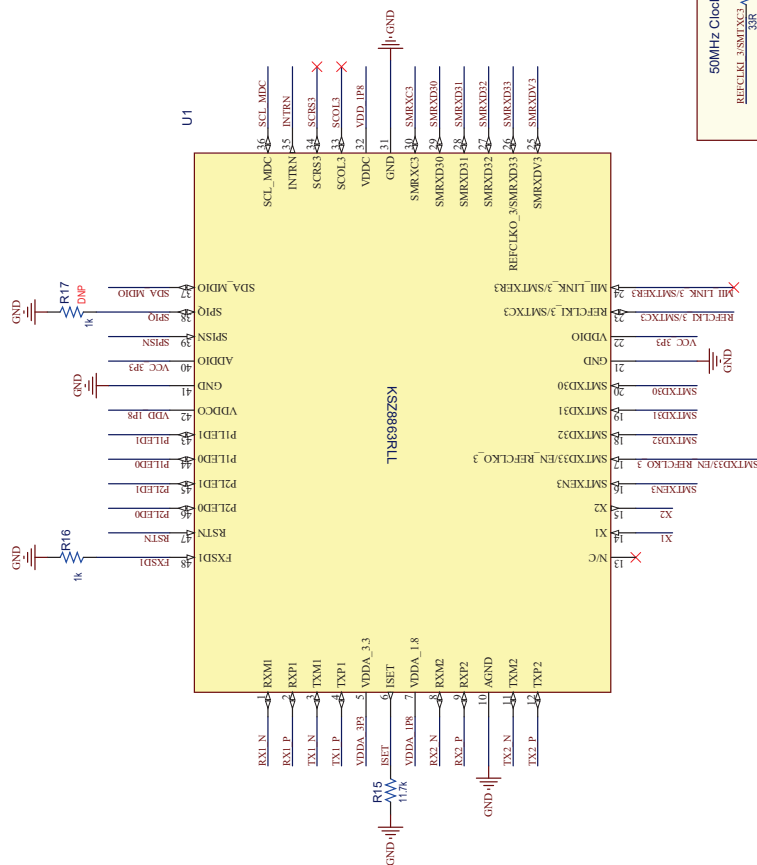
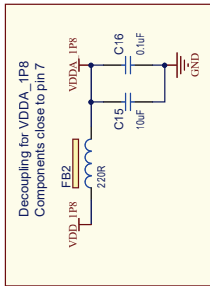
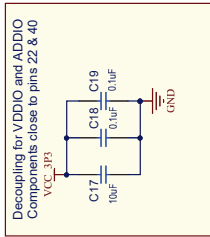
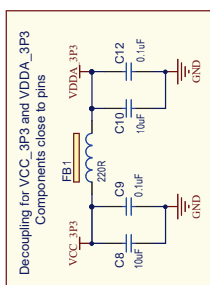
3 Additional Information

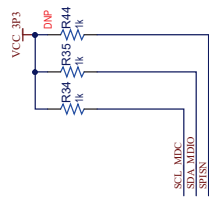
For additional information on drivers and examples, follow these links:

- <https://www.microchip.com/wwwproducts/en/KSZ8863>
- <http://www.microchip.com/mplab/mplab-harmony>

1. Schematics

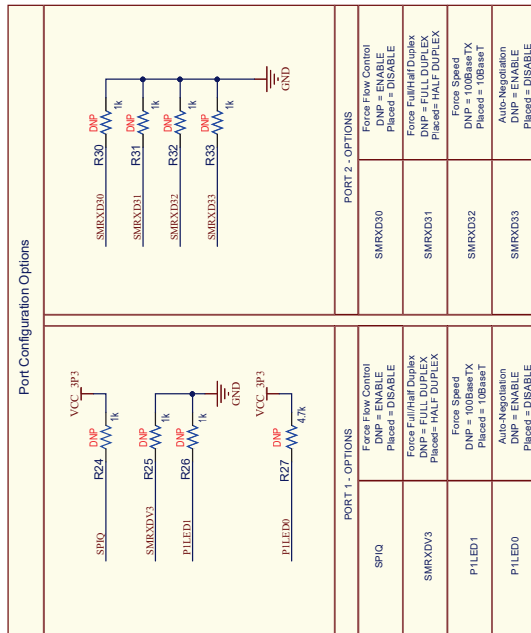






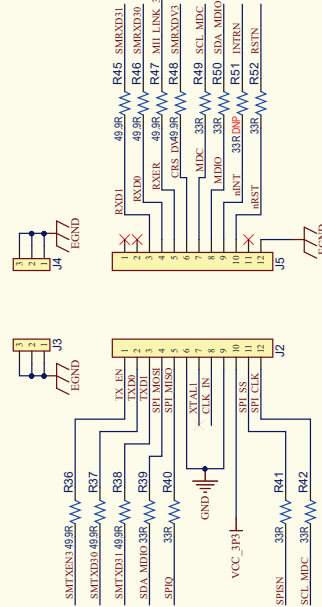
SPI Communication Option	
SPI SN	R44 = Placed
SPI Q	R24 = Placed

I2C Communication	
R34 & R35	Replace with 4.7k



NOTE ii

Signals INTRN and RSTN, Pins 35 and 47 have internal pull-up resistors integrated into the pad structure



Clock Source Configuration			
Ph: 17 SATV0333 Internal Pull-Up	Ph: 18 SATV0332 Internal Pull-Up	Clock Source	Note
0	0	External 50MHz OSC input to REFCLK0_3 and X1 pin identity	EN_REFCLK0_3 = 0 to Disable REFCLK0_3 for better EMI
1	0	50MHz on X1 pin is clock source. REFCLK0_3 to REFCLK3 externally	EN_REFCLK0_3 = 1 to Enable REFCLK0_3
0	1	25MHz on X1 pin is clock source. REFCLK0_3 to REFCLK3 externally	EN_REFCLK0_3 = 1 to Enable REFCLK0_3
0	1	25MHz on X1 pin. 50MHz DMI to REFCLK0_3 internally	EN_REFCLK0_3 = 0 to Disable REFCLK0_3
0	1	0 or 1	EN_REFCLK0_3 = 0 to Disable REFCLK0_3

Bus Communication Configuration		Serial Bus Configuration
		I2C (master mode) EEPROM
		I2C Slave Mode
		SPI Slave Mode
		EEPROM

2. Revision History

Revision B - March 2019

The following changes were implemented for this release:

- Updated the schematics:
 - Added the property and notation DNP to the resistor R51
- Updated document format

Revision A - June 2018

Initial release of this document.

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