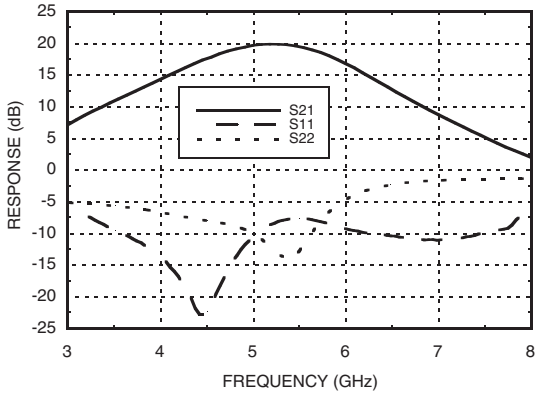
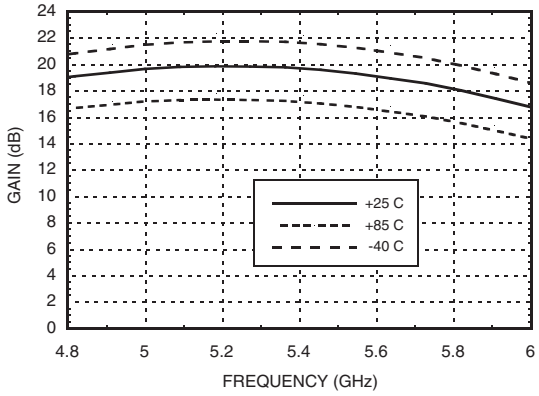
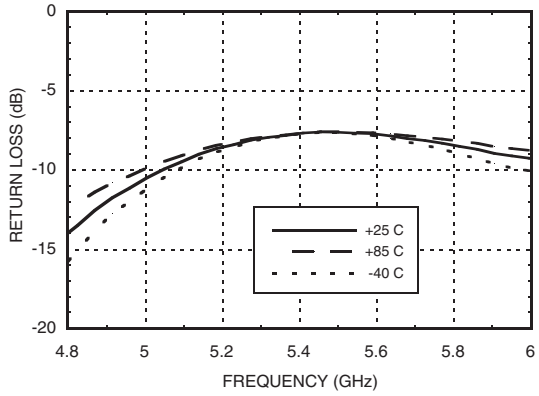
Broadband Gain & Return Loss



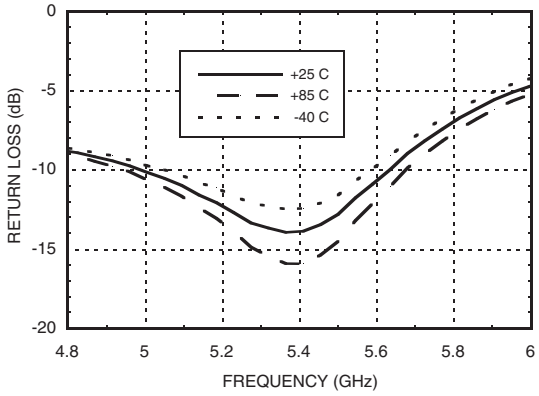
Gain vs. Temperature



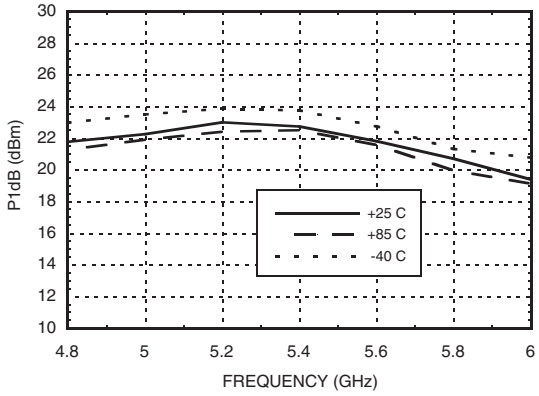
Input Return Loss vs. Temperature



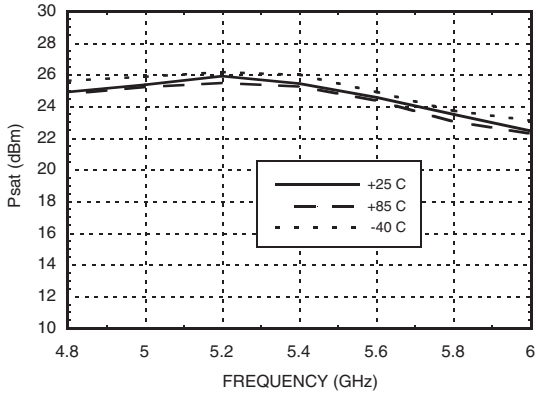
Output Return Loss vs. Temperature



P1dB vs. Temperature



Psat vs. Temperature



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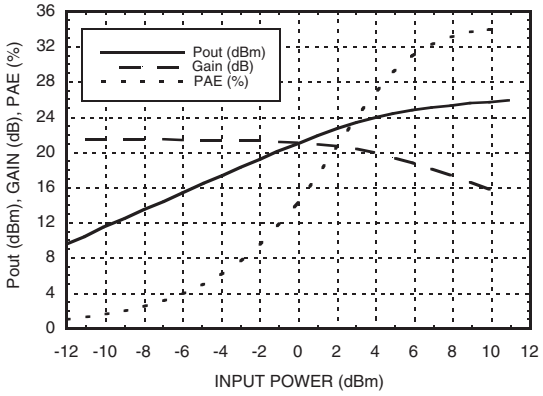
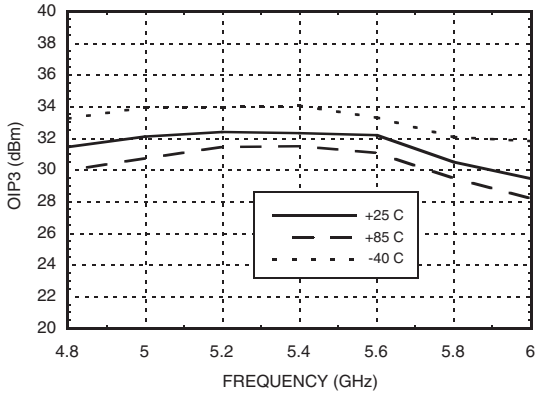
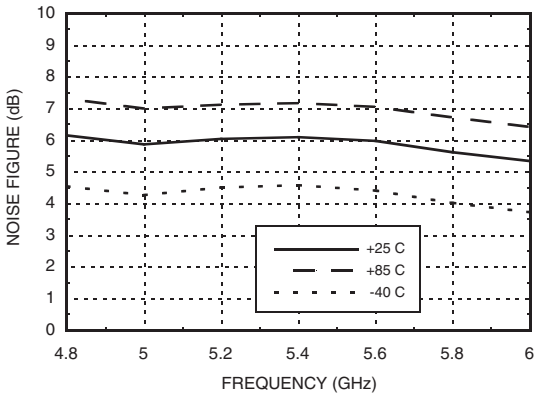
Power Compression @ 5.2 GHz



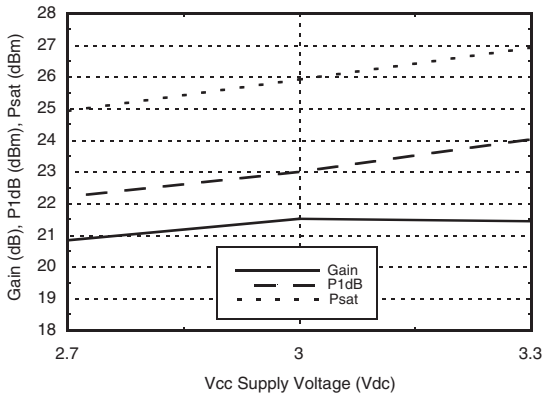
Output IP3 vs. Temperature



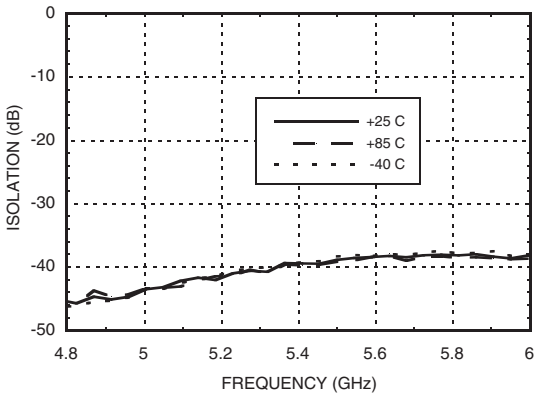
Noise Figure vs. Temperature



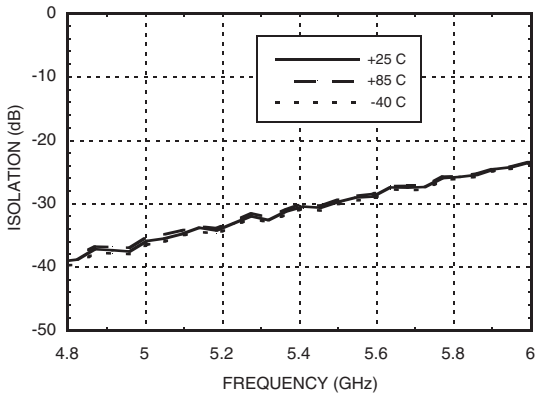
Gain & Power vs. Supply Voltage



Reverse Isolation vs. Temperature



Power Down Isolation vs. Temperature



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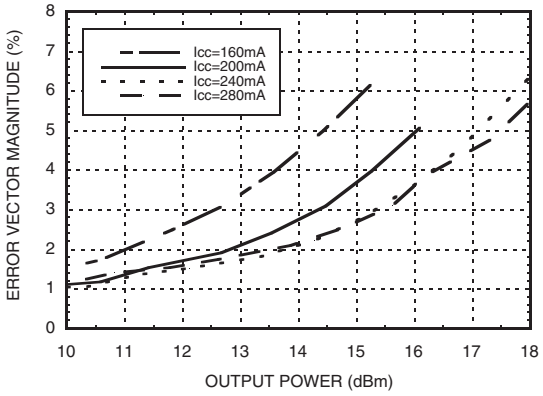
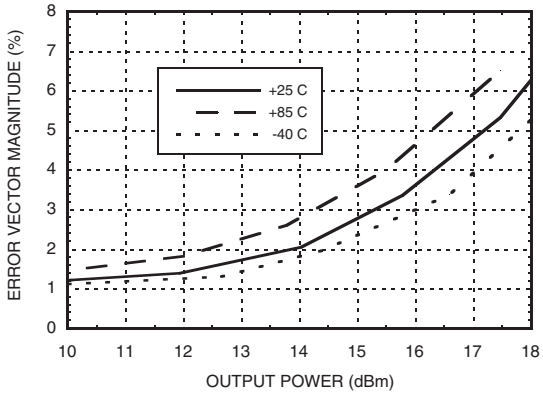
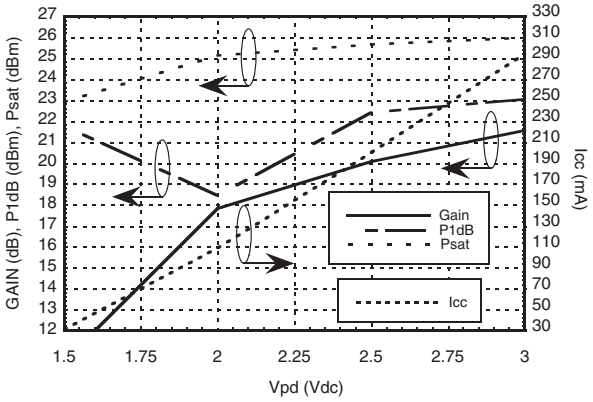
EVM vs. Supply Current, F = 5.2 GHz



EVM vs. Temperature, Icc = 240 mA, F = 5.2 GHz



Gain, Power & Quiescent Supply Current vs. Vpd @ 5.2 GHz



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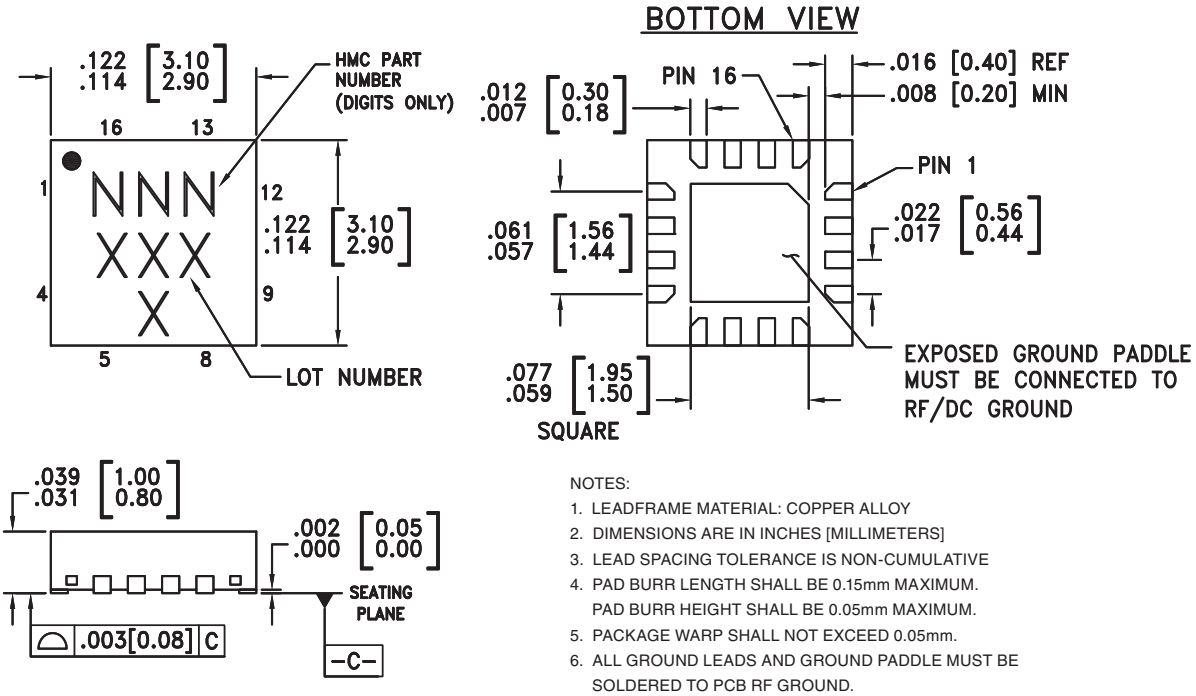
Absolute Maximum Ratings

Collector Bias Voltage (Vcc)	+5Vdc
Control Voltage (Vpd)	+3.5 Vdc
RF Input Power (RFIN)(Vs = Vpd = +3.0 Vdc)	+13 dBm
Junction Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C)	1.105 W
Thermal Resistance (junction to ground paddle)	59 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC415LP3	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	415 XXXX
HMC415LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	415 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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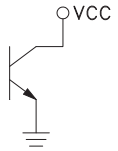
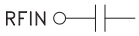
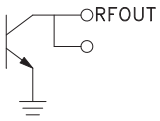
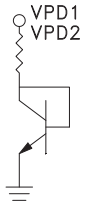
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	Vcc	Power supply voltage for the first amplifier stage. An external bypass capacitor of 330 pF is required as shown in the application schematic.	
2, 3, 5, 6, 7, 8, 9, 12, 13, 15, 16	GND	Ground: Backside of package has exposed metal ground slug that must be connected to ground thru a short path. Vias under the device are required.	
4	RFIN	This pin is AC coupled and matched to 50 Ohms from 5.0 to 6.0 GHz.	
10, 11	RFOUT	RF output and DC bias for the output stage.	
14	Vpd	Power control pin. For maximum power, this pin should be connected to 3.0V. A higher voltage is not recommended. For lower idle current, this voltage can be reduced.	

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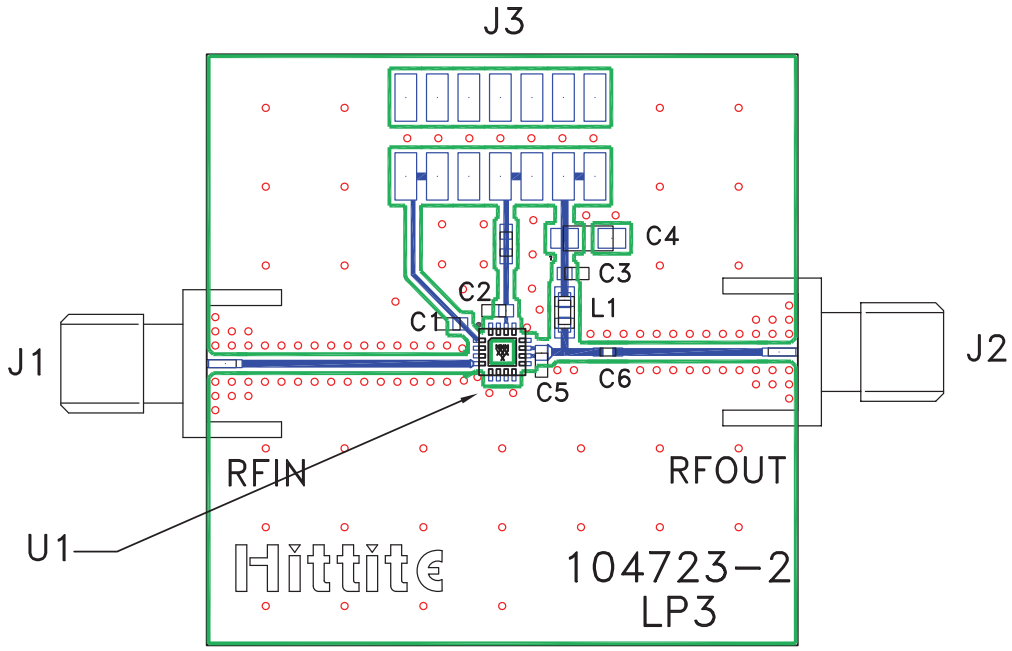
Evaluation PCB



List of Materials for Evaluation PCB 105173 [1]

Item	Description
J1 - J2	PCB Mount SMA RF Connector
J3	2 mm DC Header
C1 - C3	330 pF Capacitor, 0603 Pkg.
C4	2.2 µF Capacitor, Tantalum
C5	0.5 pF Capacitor, 0603 Pkg.
C6	7.0 pF Capacitor, 0402 Pkg.
L1	3.0 nH Inductor, 0805 Pkg.
U1	HMC415LP3 / HMC415LP3E Amplifier
PCB [2]	104723 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.

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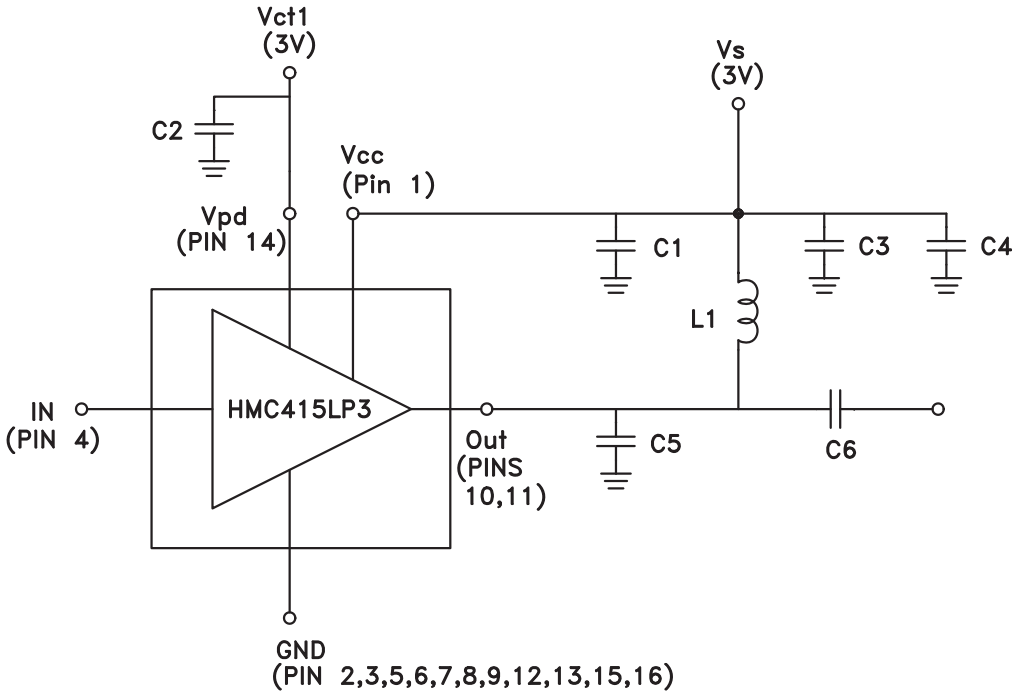
Application Circuit



Recommended Component Values	
L1	3.0 nH
C1, C2, C3	330 pF
C4	2.2 µF
C5	0.5 pF
C6	7.0 pF

Note 1: C1 should be located < 0.1" (2.54mm) from Pin 1 (Vcc)

Note 2: C3 should be located < 0.1" (2.54mm) from L1.

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