ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} and V_{CH} Pins with Respect to V_{SS}	-0.3V to +18V
Voltage on LED1 Pin	-0.3V to +18V
Voltage on SNS-	-0.3V to +0.3V
Voltage on C_{BIAS}	-0.3V to 6V
Voltage on all Other Pins	-0.3V to V_{Cbias}
Continuous Sink Current V_{CH} and LED1	28mA
Operating Temperature Range	-20°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020
Human Body Model (HBM) ESD Limit of V_{CH} Pin	500V
HBM ESD Limit of all Other Pins	2KV

**This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

RECOMMENDED DC OPERATING CONDITIONS

($4.5V \le V_{DD} \le 16.5V$; T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	(Note 1)	4.5		16.5	V
LED1 Voltage	V_{LED}	(Note 1)	0.0		16.5	V
Mode Voltage	V_{MODE}	(Note 1)	0.0		V_{Cbias}	V
V_{CH} Voltage	V_{VCH}	(Note 1)	0.0		16.5	V
C_{BIAS} Capacitor Range	C_{Cbias}		.02		.15	µF
R_T Resistor Range	R_{Rt}		20		240	KΩ

DC ELECTRICAL CHARACTERISTICS

($4.5V \le V_{DD} \le 16.5V$, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Current (Note 2)	I_{DDA}	Linear Mode, V_{DD} = 16.5V		1.3	1.6	mA
		Comparator Mode, V_{DD} = 16.5V		150	250	µA
Idle Current	I_{DDS}	$V_{DD} < V_{UVLO}$			10	µA
Discharge Current	I_{DDD}	Discharge latch set (Note 2)			200	µA
UVLO Threshold	V_{UVLO}	V_{DD} Rising (Note 3)	3.8	3.9	4.0	V
UVLO Hysteresis	$V_{UVLO-HYS}$	V_{DD} Falling		35		mV
V_{CH} Sink Current	I_{OL-Vch}	V_{OL} = 1.5V	20			mA
LED1 Sink Current	I_{OL-LED}	V_{OL} = 1.0V	20			mA
Leakage Current, V_{CH}, LED1	I_{LKG}	Pin Inactive or Device Idle	-1		+1	µA
THM Pin Leakage Current	$I_{LKG-THM}$		-1		+1	µA
V_{BATT} Pin Leakage Current	$I_{LKG-Vbatt}$		-50		+50	nA
C_{BIAS} Voltage	V_{Cbias}	$0 < I_{Cbias} < 0.4mA$	3.9	4.0	4.3	V
DIV Pin Load Current	I_{Div}				500	uA
Current Sense Amplifier Gain	G_{ERR}	$100µA < I_{Vch} < 20mA$	5	6.25	7.5	$\tilde{\Omega}^{-1}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Comparator Gain	G_{COMP}	(Note 7)	10			Ω^{-1}

AC ELECTRICAL CHARACTERISTICS

($4.5V \le V_{DD} \le 16.5V$, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Debounce Time	t_{UVLO}		10			µs
Current Sense Comparator Propagation Delay	t_{COMP}	(Note 7)			250	ns
Discharge Detect Propagation Delay	t_{DD}	From detection of current reversal			1	µs
Return To Normal Function (Op-Amp or Comparator Mode)	t_{RNF}	Time from reset of discharge latch			1	µs
R_T Timing Accuracy	t_{Rt}	(Note 4)	-10		+10	%
Internal Clock Accuracy	t_{BASE}		-10		+10	%

ELECTRICAL CHARACTERISTICS: CHARGING

($4.5V \le V_{DD} \le 16.5V$, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FAST-CHARGE Comparator Threshold	V_{FC}	FAST-CHARGE	-127	-121	-115	mV
FAST-CHARGE Comparator Hysteresis	V_{HYS-FC}	FAST-CHARGE	31	28	25	mV
TOPOFF and PRECHARGE Comparator Threshold	V_{TO}	TOPOFF and PRECHARGE	-38	-33	-28	mV
TOPOFF and PRECHARGE Comparator Hysteresis	V_{HYS-TO}	TOPOFF and PRECHARGE	10	8	6	mV
Discharge Latch Reset Threshold	$V_{DCHG-RST}$		-15	-10	-5	mV
Discharge Latch Set Threshold	$V_{DCHG-SET}$	Reverse current through sense resistor	5	10	15	mV
Low Battery Detect Threshold	V_{LB}	From presence detect into PRECHARGE	0.95	1.0	1.05	V
Cell Detect Threshold	V_{DET}		1.50	1.55	1.60	V
No Cell Detect Threshold	V_{OPEN}		1.60	1.65	1.70	V
Presence Detect Threshold Hysteresis	V_{HYS-PD}		90	100	110	mV
Minimum Charge Temp	$V_{THM-MIN}$	(Note 5, 6)	2.88	2.92	2.96	V
				0		ºC
Maximum Charge Temp	$V_{THM-MAX}$	(Note 5, 6)	1.28	1.32	1.36	V
				45		ºC
Over Temp	$V_{THM-STOP}$	(Note 5, 6)	1.12	1.16	1.20	V
				50		ºC
dT/dt Detect	T_{TERM}		0.425	0.5	0.575	ºC/min

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
dT/dt Blanking Time	t_{BLANK}		3.85	4.3	4.75	Min
PRECHARGE Timeout	t_{PC-TO}			30		Min
FAST-CHARGE Timer Range	t_{FC}		0.5		6	Hours
TOPOFF to FAST-CHARGE Duration Ratio		DS2715		1:2		
		DS2715B		1:4		

Note 1: Voltages relative to V_{SS}.
Note 2: Does not include current through V_{CH}, R_T, and DIV pins.
Note 3: Below this voltage no I/O pins are active.
Note 4: Does not include tolerance of R_T resistor.
Note 5: V_{BIAS} and resistor tolerances must be added to determine actual threshold.
Note 6: Specified temperature thresholds are only valid if recommended thermistor types are used.
Note 7: Specification is guaranteed by design.

DETAILED PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	C_{BIAS}	Bypass for Internal Voltage Regulator
2	V_{CH}	Cell Stack Charge Control Output
3	V_{SS}	Chip Supply Return and Local Ground Reference
4	LED1	Charging Indicator Output
5	DNC	Do Not Connect
6	V_{SS}	Chip Supply Return and Local Ground Reference
7	CTG	Connect to Local Ground (V_{SS})
8	CTG	Connect to Local Ground (V_{SS})
9	MODE	Mode Select. Connect to V_{SS} for linear mode of operation or C_{BIAS} for comparator mode of operation.
10	DIV	Thermistor Divider. Stable output to form a resistor divider for measuring temperature on THM
11	SNS+	Positive Current Sense. Connect to the charge source side of the sense resistor
12	SNS-	Negative Current Sense. Connect to the cell stack side of the sense resistor
13	V_{DD}	Chip Supply Input: +4.5V to +16.5V range
14	R_T	Failsafe Timeout. Timeout is selected by an external resistor from R_T to V_{SS}
15	THM	Thermistor Input. Connect to a thermistor located in the cell pack and a divider resistor from the Div pin
16	V_{BATT}	Battery Voltage Sense Input. Connect to a divider from the positive terminal of the cell stack to measure the voltage of a single cell

Figure 1. BLOCK DIAGRAM

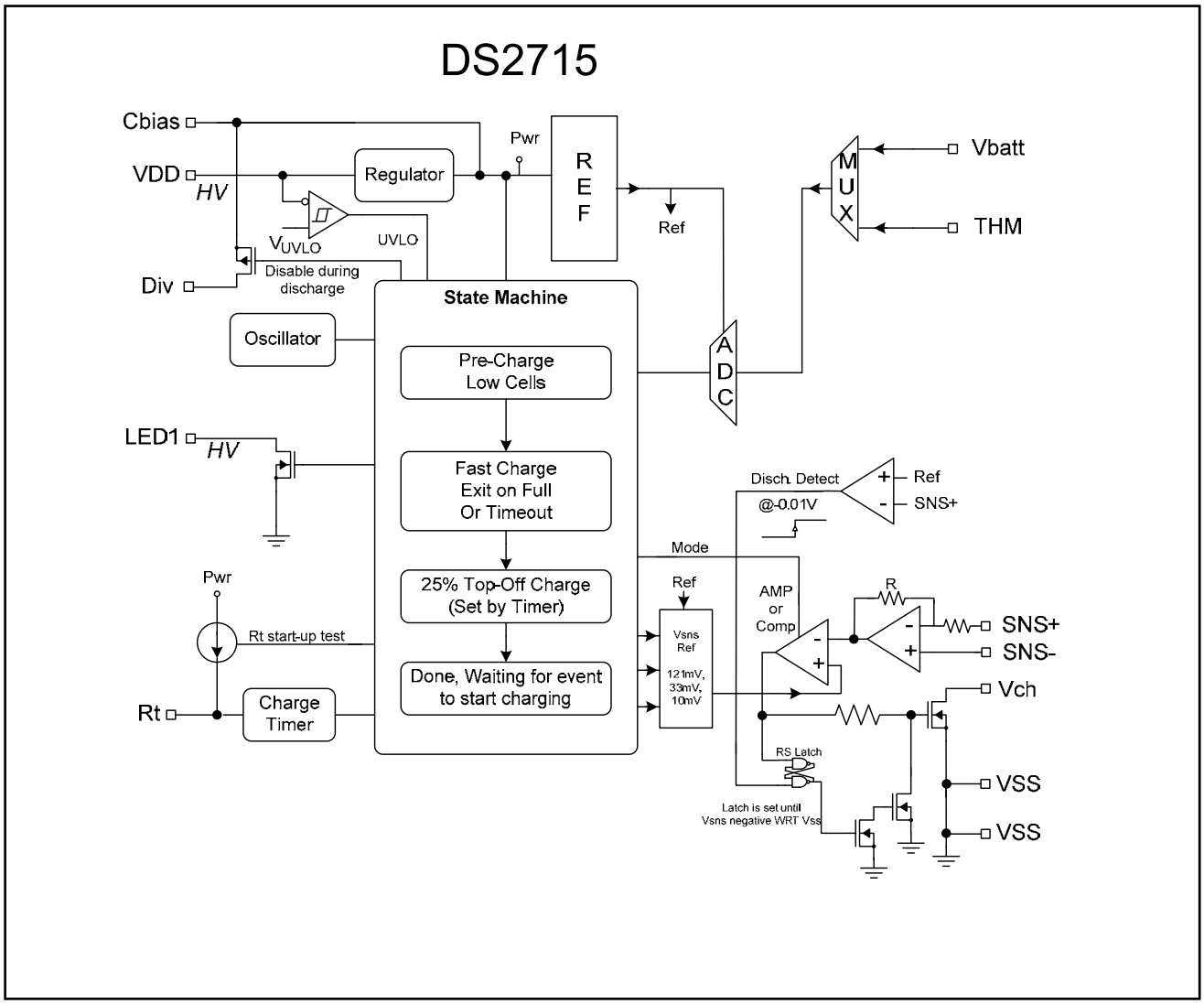
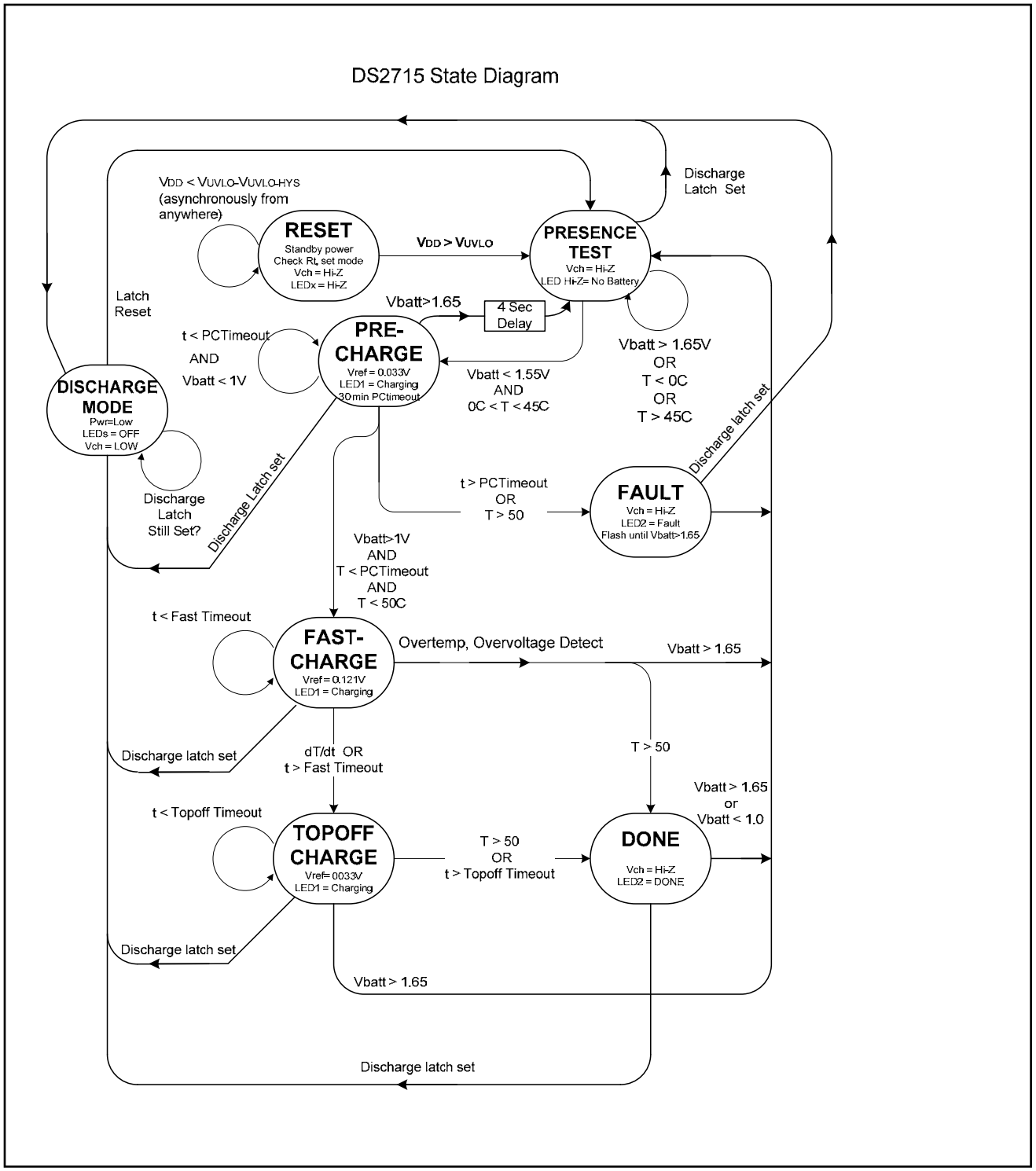


Figure 2. STATE DIAGRAM



DETAILED DESCRIPTION

Charge Cycle Overview

The DS2715 regulates the charge of up to 10 NiMH cells in a series configuration. With the mode select pin, the DS2715 can be configured to regulate either as an error amplifier in linear mode or as a comparator in switched mode. A charge cycle begins in one of two ways: with the application of power to the DS2715 while the cell pack is already inserted, or with the detection of cell insertion after power-up.

After cell presence confirmation, PRECHARGE qualification occurs to prevent fast charging of deeply depleted cells or charging under extreme temperature conditions. Pre-charging is performed at a reduced rate of approximately ¼ the FAST-CHARGE current until each cell reaches 1V. The algorithm then proceeds to the FAST-CHARGE phase. Fast charging continues as long as the cell pack temperature is less than 50°C based on the THM voltage, and the cell voltage as measured at the V_{BATT} pin in the middle of the resistor divider remains below 1.65V, indicating the cell pack is still present. Fast charging terminates normally by measuring the cell pack's thermal rate of change, dT/dt. When the cell pack's thermal rate of change exceeds 0.5°C per minute, the DS2715 enters TOPOFF. The DS2715 has an internal charge timer as secondary overcharge protection if the charge is not terminated properly by the dT/dt method. The charge termination timer duration is user selectable from 30 minutes up to 6 hours by an external resistor on the R_T pin.

Following a normally terminated or timed-out FAST-CHARGE phase, the DS2715 enters TOPOFF. It remains in this state for one-half (one-quarter for DS2715B) of the period of the FAST-CHARGE timeout as selected by the external resistor on R_T. After the TOPOFF charge timer expires, the DONE phase continues indefinitely until the cell pack is removed from the charger or DISCHARGE mode is entered. For the standard application circuit configuration, when a load drawing at least Vdchg-set across the sense resistor is attached to the cell pack, the DS2715 switches to DISCHARGE mode. All charge functions are disabled and the regulation FET is driven on to allow the cell pack to discharge. Throughout the charging process, the open-drain LED1 output indicates the charge status to the user.

Undervoltage Lockout (Reset)

The UVLO circuit serves as a power-up and brownout detector by monitoring V_{DD} to prevent charging until V_{DD} rises above V_{UVLO}, or when V_{DD} drops below V_{UVLO} - $V_{UVLO-HYS}$. If UVLO is active, charging is prevented, the state machine is forced to the RESET state, and all charge timers are reset. A 10µs deglitch circuit provides noise immunity. Once V_{DD} reaches an acceptable operating voltage, the DS2715 enters the PRESENCE state.

PRESENCE

The DS2715 enters the PRESENCE state whenever $V_{DD} > V_{UVLO}$ and $V_{BATT} > V_{OPEN}$ indicating that the charge source is present, but no cell is available to charge. The DS2715 will remain in the PRESENCE state until a cell is inserted into the circuit causing the voltage on V_{BATT} to fall below 1.55V (V_{DET}) and the cell temperature is inside a valid charging range between 0°C and 45°C ($T_{THM-MIN}$ and $T_{THM-MAX}$ when used with recommended thermistor and resistor values). If both of these conditions are met, the DS2715 will enter PRE-CHARGE. If cells are inserted, but the temperature is outside the valid charging range, the DS2715 will remain in the PRESENCE state until the cell temperature falls within the valid charging range.

PRE-CHARGE

The DS2715 enters the PRECHARGE state when a valid cell voltage is applied to V_{BATT} and the cell temperature as measured by the DS2715 thermistor circuit is within the valid charging range. PRE-CHARGE mode has a 4 second filter to suppress noise on V_{BATT} caused by cell insertion that may cause a premature return to PRESENCE state. The DS2715 precharges the cell by regulating the voltage drop across the sense resistor to -33mV (V_{TO}) in linear mode or -29mV (V_{TO} + 0.5 x V_{HYS-TO}) in comparator mode. The polarity of the voltage drop across the sense resistor is referenced to the polarity relationship indicated by the SNS+ and SNS- pins on the device. Precharging will last until the cell voltage measured by V_{BATT} exceeds 1.0V ($V_{BATT} > V_{LB}$), at which time the DS2715 will enter the FAST-CHARGE state. If the cell voltage does not exceed V_{LB} within 30 minutes or if the cell temperature exceeds 50°C at any time during PRECHARGE, the DS2715 enters the FAULT state. If at any time during PRECHARGE the voltage on V_{BATT} exceeds 1.65V (V_{OPEN}), the DS2715 determines that the cell pack has been removed and returns to the PRESENCE state.

FAST-CHARGE

In FAST-CHARGE mode, the DS2715 regulates the voltage across the sense resistor to -121mV (V_{FC}) in linear mode or about -107mV (V_{FC} + 0.5 x V_{HYS-FC}) in comparator mode. LED1 indicates the cell pack is being charged. During FAST-CHARGE, the DS2715 constantly measures the rate of change of the cell temperature (dT/dt). When the cell pack's dT/dt exceeds 0.5°C per minute (T_{TERM}) the DS2715 enters the TOPOFF state. The DS2715 ignores changes in the cell temperature caused by charge initiation for the first 4.3 minutes (t_{BLANK}). As secondary overcharge protection, the DS2715 will terminate FAST-CHARGE and enter TOPOFF based on a time delay set by the external resistor on the R_T pin. This resistor value can set the secondary charge termination delay to anywhere from 30 minutes up to 6 hours. If the cell temperature exceeds 50°C at any time during FAST-CHARGE, the DS2715 enters the DONE state. If at any time during FAST-CHARGE the voltage on V_{BATT} exceeds 1.65V (V_{OPEN}), the DS2715 determines that the cell pack has been removed and returns to the PRESENCE state.

TOPOFF

In TOPOFF mode, the DS2715 regulates the voltage across the sense resistor to -33mV (V_{TO}) in linear mode or -29mV (V_{TO} + 0.5 x V_{HYS-TO}) in comparator mode. LED1 indicates the cell pack is being charged. The charge timer is reset and restarted with a time-out period of one-half (one-quarter for DS2715B) the fast-charge duration. When the charge timer expires or if the measured temperature exceeds 50°C, the charger enters the DONE state.

DONE/Maintenance

The DS2715 enters the DONE state whenever the charge completes normally or if the measured cell temperature exceeds 50°C during the charge. While in the done state V_{CH} is driven to high impedance to prevent further regulated charging of the cell pack and LED is driven high-impedance to indicate no charging is taking place. A maintenance charge can be applied to the cells by providing a one-way resistive path from the charge source to the cell pack bypassing the regulating transistor. See the example in the circuit of Figure 3. The DS2715 remains in the DONE state until a cell voltage greater than 1.65V (V_{OPEN}) is detected on V_{BATT} indicating cell pack removal, the Rt pin is floated (see SUSPEND function), or DISCHARGE mode is entered.

FAULT

The DS2715 enters FAULT if PRECHARGE is unable to charge the cell above 1.0V (V_{LB}) before the 30 minute PRECHARGE timeout (t_{PC-TO}) or if the cell temperature exceeds 50°C during PRECHARGE. In the fault state, V_{CH} is high impedance and LED1 output pulses to indicate the fault condition. The DS2715 remains in FAULT until a cell voltage greater than 1.65V (V_{OPEN}) is detected on V_{BATT} indicating the cell pack has been removed. The DS2715 then enters the PRESENCE state and waits for the next cell insertion.

SUSPEND

Suspension of charge activity is possible by floating the R_T pin. The state machine and all timers are reset to their presence test conditions when suspending from a charge mode. The DISCHARGE mode is not affected by the SUSPEND function. The Vch output is high-impedance for charging modes, and operates as normal for DISCHARGE mode during SUSPEND. The SUSPEND function is useful for resetting the DS2715 in applications where the batteries are not removed from the circuit and DISCHARGE mode is not utilized. It also allows for a means to stop charging by the application circuit, such as with a microcontroller signal for example.

DISCHARGE Mode

When the DS2715 detects a discharge current voltage drop of $V_{DCHG-SET}$ or greater across the sense resistor, charging is terminated and the DS2715 enters the DISCHARGE state. Initially, the discharge current must flow through the parasitic diode of the PFET regulating transistor until the DS2715 switches to DISCHARGE mode. While in this mode, voltage sensing, thermal sensing, and the LED1 output are disabled. The V_{CH} pin is driven low to fully bias the charge control transistor into a low impedance state and allow the pack to be discharged. Current drain of the DS2715 drops to I_{DDD}. The DS2715 remains in DISCHARGE mode until a charge current across the sense resistor causes a sense voltage of at least $V_{DCHG-RST}$ or the device is power cycled. When either of these events occur, the DS2715 enters the PRESENCE state to begin a new charge cycle.

LED1 Output

Open-drain output LED1 pulls low to indicate charge status. When inactive, the output is high impedance. LED1 displays the state of charge and the charge results. The LED1 pin drives low in a 1Hz, 50% duty cycle “blink” pattern to indicate cells are charging. LED1 blinks at 4Hz, 50% duty cycle to signal a charging fault has occurred. The LED1 pin remains in a high-impedance state when no cells are present or the discharge latch is set. Table 2 summarizes the LED operation for each charge condition.

Table 2. LED DISPLAY PATTERNS BASED ON CHARGE STATE

	CHARGE STATE				
	NO BATTERY	**CHARGING**	**DONE**	**FAULT**	**DISCHARGE MODE**
LED1	High-Z	Blinks at 1HZ, 50% duty cycle	High-Z	Blinks at 4Hz, 50% duty cycle	High-Z

High-Z = High Impedance

CURRENT REGULATION

Three basic modes of charging operation are supported by the DS2715: Offline switching through an optocoupler, linear regulation, and DC input switched mode. The offline switching method requires a voltage clamp on the regulated output. Mode of operation is selected through the Mode pin. Connecting the Mode pin to V_{SS} configures the analog block as a transconductance amplifier for linear mode of operation. Connecting the Mode pin to the Cbias pin configures the DS2715 as a comparator for switched mode of operation.

Current-Sense Amplifier Mode

An error amplifier block provides several options to regulate the charge current. The 20mA open-drain output V_{CH} can drive a PMOS or PNP pass element for linear regulation, or the output can drive an optocoupler for isolated feedback to a primary-side PWM controller. PMOS is the preferred device type when the pass element will also be used as a discharge path to the load. This is because sufficient transconductance with both polarities of drain current is easily realized compared to the difficulty in achieving this with BJT types. The SNS- pin is a remote-sense return and should be connected to the battery ground side of the sense resistor using a separate isolated conductor. During FAST-CHARGE, an error signal between the current-sense signal (across the sense resistor) and the internal reference is produced so the voltage across the sense resistor is maintained at V_{FC} in a closed-loop circuit. During PRECHARGE and TOPOFF, the voltage across the sense resistor is maintained at V_{TO}.

Current-Sense Comparator Mode

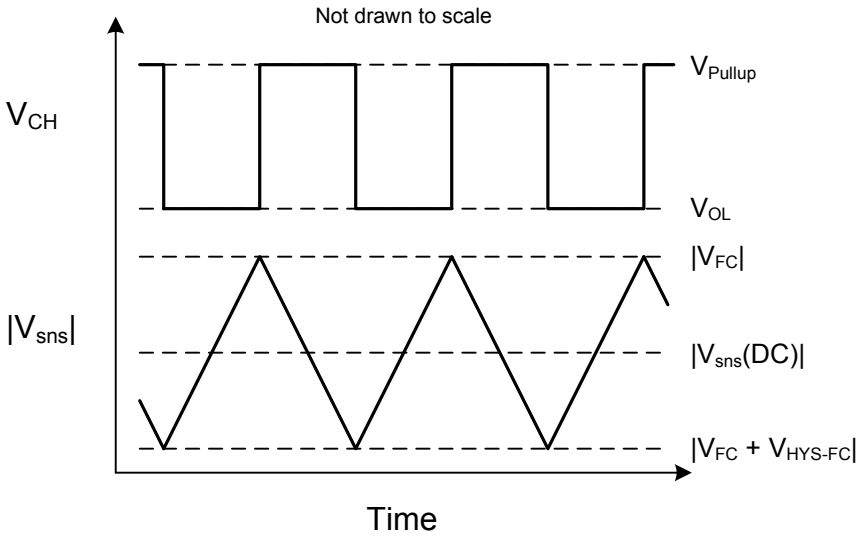
The comparator in the DS2715 switches the open drain V_{CH} pin between ON and OFF when the sense resistor voltage reaches high and low thresholds. The V_{CH} output is capable of driving a PNP bipolar or a PMOS transistor, enabling the use of a switch-mode power stage. PMOS is again preferred when the pass element will also be used

as a discharge path to the load. Hysteresis on the comparator input provides the difference between the ON and OFF state thresholds. In a closed-loop regulation circuit, the comparator regulates voltage across the sense resistor as referenced to the SNS pins to a DC average of:

$$V_{SNS} = V_{FC} + 0.5 \times V_{HYS-FC} = -0.107V \text{ during FAST-CHARGE}$$

$$V_{SNS} = V_{TO} + 0.5 \times V_{HYS-TO} = -0.029V \text{ during TOPOFF}$$

Figure 3. Ideal Comparator Input and Charge Control Output Waveforms



Charge Rate Selection

The charge rate is determined by an external sense resistor connected between the SNS+ and SNS- pins. The DS2715 will regulate the charge current to maintain a voltage drop of V_{FC} (or V_{FC} + 0.5 x V_{HYS-FC} in comparator mode) across the sense resistor during FAST-CHARGE. The sense resistor can therefore be selected by:

Linear Mode: $R = |V_{FC} / \text{Desired FAST-CHARGE Current}|$

Comparator Mode: $R = |(V_{FC} + 0.5 \times V_{HYS-FC}) / \text{Desired FAST-CHARGE Current}|$

Timeout Selection

The various charge modes employ different timers to ensure reliable and safe charging. PRECHARGE has a fixed 30 minute limit generated by an internal oscillator. A fault is generated if this time limit is exceeded. FAST-CHARGE mode normally operates until its dT/dt termination scheme activates. In the event that the dT/dt sensing does not perform correctly, a safety timeout is required. This timeout is set by an external resistor on the Rt pin to V_{SS} and provides secondary protection against significant overcharging. As such, the value of the Rt resistor should be chosen so that the timeout is greater than the FAST-CHARGE time expected in the application, but not so much greater that its protection is compromised. If the timer expires during FAST-CHARGE, the timer count is reset and charging proceeds to the TOPOFF charge phase. The Rt resistor also sets the timed charge duration of TOPOFF mode. The TOPOFF time-out period is fixed at half (a quarter for the DS2715B) of the FAST-CHARGE time-out period. When the timer expires in TOPOFF, the DS2715 enters the DONE state.

Resistors can be selected to support fast-charge time-out periods of 0.5 to 6 hours and TOPOFF charge time-out periods of 0.25 to 3 hours (0.125 to 1.5 hours for the DS2715B). The programmed FAST-CHARGE time approximately follows the equation:

t(minutes) = 1.5 x R(ohms) / 1000

TEMPERATURE SENSE

Accurate temperature sensing is needed to determine end of charge by dT/dt and to detect over temperature fault conditions. Connecting an external 10kΩ NTC thermistor between THM and V_{SS}, and a 10kΩ bias resistor between Div and THM allows the DS2715 to sense temperature. To sense the temperature of the cell pack, locate the thermistor close to the body of a cell, preferably in the middle of the cell pack. Several recommended 10kΩ thermistors are shown in Table 3.

Min, Max Temperature Compare

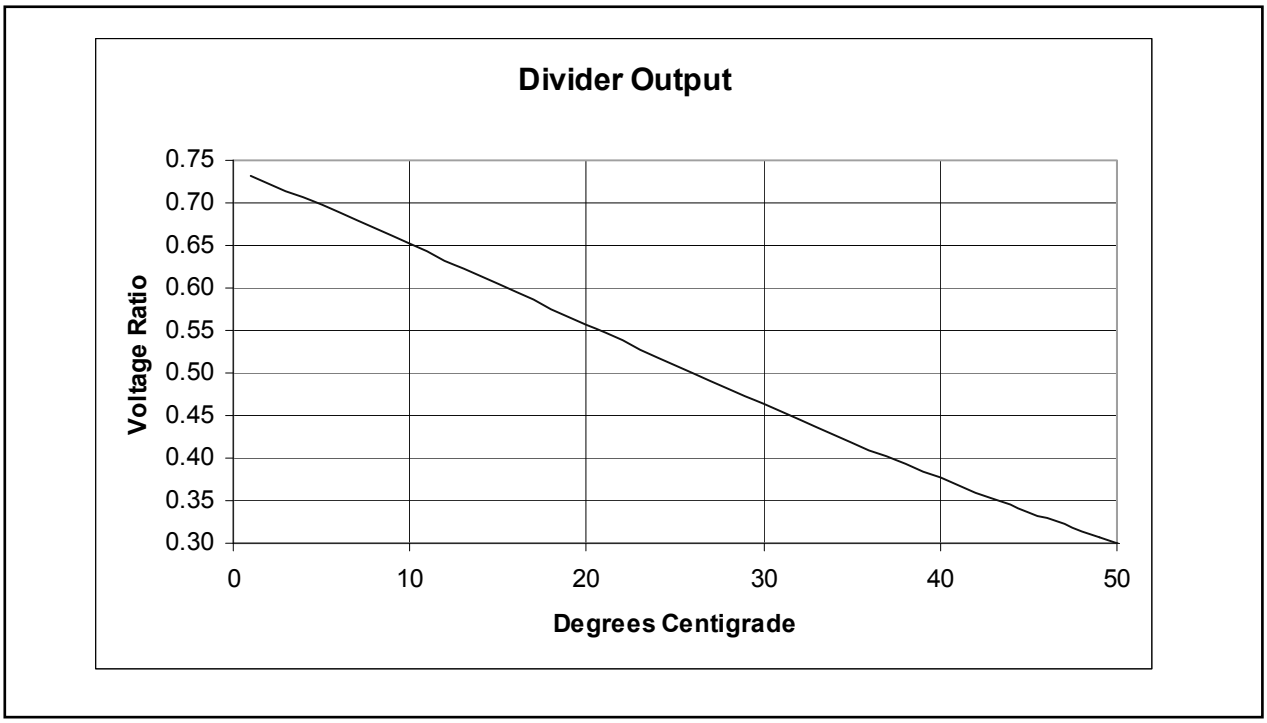
The voltage thresholds of the THM input ($V_{THM-MIN}$, $V_{THM-MAX}$) are set to allow charging to start if the thermistor temperature is between 0°C and 45°C when using the recommended 10kΩ bias resistor and 10kΩ thermistor circuit. If pre-charging is in progress, and the voltage on THM reaches $V_{THM-STOP}$, pre-charging stops and a fault condition is generated. If the voltage on THM reaches $V_{THM-STOP}$ during FAST-CHARGE or TOPOFF, charging stops and the DS2715 enters the DONE state. FAST_CHARGE will complete normally and TOPOFF will begin if the voltage change on THM exceeds the equivalent T_{TERM} ºC per minute (dT/dt Detect specification).

Table 3. THM THRESHOLDS

THM THRESHOLD	RATIO OF V_{CBIAS}	THERMISTOR RESISTANCE (Ω)	TEMPERATURE (°C)	
			Semitec 103AT-2	Fenwal 197-103LAG-A01 173-103LAF-301
MIN	0.73	27.04k	0°C	4°C
MAX	0.33	4.925k	45°C	42°C
STOP	0.29	4.085k	50°C	47°C

Used with a 10k resistor, the Semitec 103AT-2 provides about 0.9% full scale per degree sensitivity. This linearity is shown in the curve in Figure 4. The left axis is the ratio of the sensed voltage to the divider's input voltage (V_{Cbias}).

Figure 4. RATIO OF THM PIN TO CBIAS PIN OVER TEMPERATURE

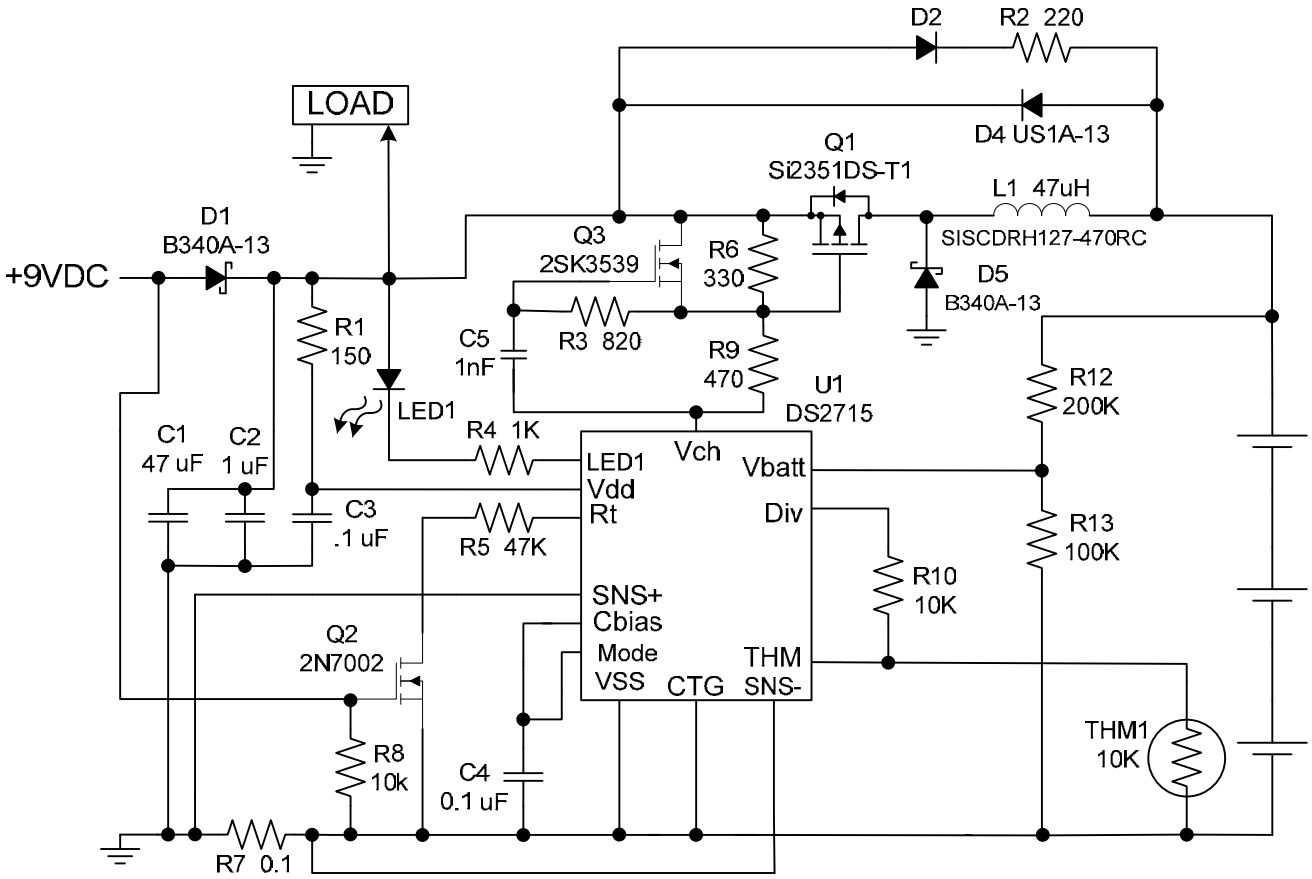


Application Circuits

Switchmode

Figure 5 shows a typical DS2715 switchmode application circuit for charging a 3-cell battery stack. Connecting the MODE pin to CBIAS enables the comparator mode of current regulation. The DS2715 regulates the current through the current sense resistor R7 by switching Q1 on and off as the sense resistor voltage ramps up and down toward the preset sense voltage thresholds. The .1ohm sense resistor along with the DC ground-referenced sense threshold level of $-(V_{FC} + V_{HYS-FC}/2)$ sets the average charge current in the example to 1.07A. The sense resistor should have a proper power rating for the chosen charge current.

Figure 5. TYPICAL Switchmode APPLICATION CIRCUIT FOR A 3-CELL STACK



A bootstrap subcircuit with C5, R3 and Q3 is used to improve the turnoff time of Q1 to minimize switching losses. When V_{CH} is pulled low to turn on Q1, C5 is charged through the R6/R3 path. When V_{CH} is left open-circuit to turn off Q1, the voltage of the V_{CH} node jumps up close to the gate voltage of Q1. This causes the gate of Q3 to be pushed up due to the voltage across C5. Q3 is then turned on, which helps to speed turn-off of Q1 by discharging its internal capacitances. The values of the components in this section of the circuit are tuned to work with the chosen transistors. The values of R6 and R9 should be chosen so that no more than 20mA is sunk by V_{CH}. D4 is used to clamp the inductive spike that could occur if the batteries are removed during charging. This function can also be served by an energy absorbing capacitor placed in parallel with the battery stack.

Q2 is used to float the Rt pin when the supply source is disconnected. This puts the DS2715 into SUSPEND mode and resets the state machine. D1 prevents current from flowing into the charge source. D2 and R2 create the maintenance charge current path. D1, D2 and R2 should be sized appropriately for the wattage they must dissipate based on the application parameters. R1 and C3 create a low pass filter to minimize noise transfer as the DS2715 local ground moves in relation to the system or charge source ground.

The R_T resistor (R5) is set to 47kΩ for a timeout of 70 minutes. This would be appropriate for cells with a capacity of about 1Ah when charged with the 1.07A charge current. The resistor divider with R12 and R13 is configured to present the voltage equivalent to a single cell on the Vbatt pin.

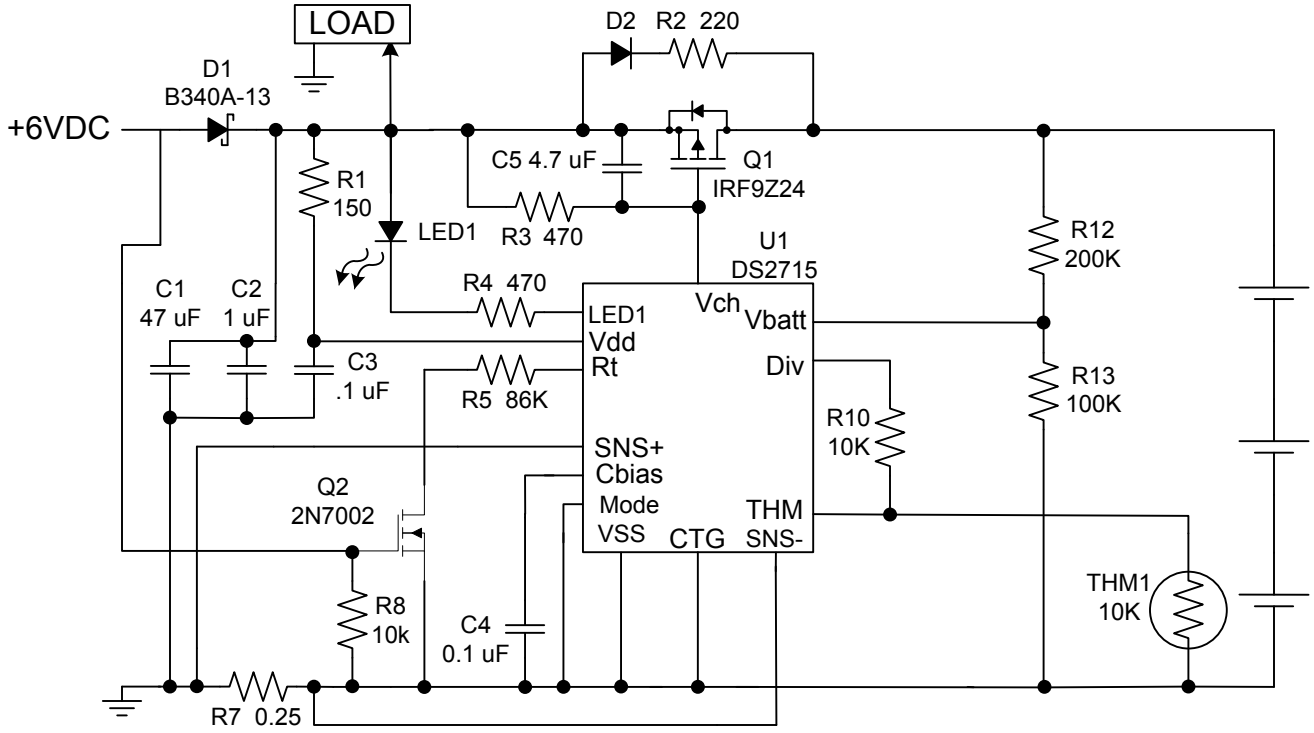
The value of L1 in the example represents a moderate switching speed of 100-150khz for fast-charge mode. L1 may be adjusted to fit specific application goals as long as the associated change in switching speed does not exceed the circuit's ability to maintain proper regulation of the sense resistor voltage. Since TOPOFF and PRECHARGE modes have a faster switching frequency than FAST-CHARGE, the regulation in these modes must be considered.

All capacitors should be ceramic surface mount types of good quality where possible. The 47uF capacitor may be any type that meets the application requirements. A different network for C1 and C2 may be necessary depending on the types of capacitors used, the layout, and the transient requirements of the application load. All resistors not previously mentioned are standard surface mount types.

Linear

Figure 6 shows a typical application circuit for charging a 3-cell stack in linear mode. The Mode pin is tied to V_{SS} for linear operation. A 250mΩ sense resistor (R7) sets the charge current to .484A, which the DS2715 regulates by controlling the V_{GS} of Q1 through the bias resistor R3. The bias resistor should be chosen so that the current that V_{CH} is required to sink does not exceed 20mA when V_{CH} is fully turned on. The preferred design target for FAST-CHARGE conditions is 10mA. The RC network of R3 and C5 set a pole in the control loop to ensure stability.

Figure 6. TYPICAL Linear APPLICATION CIRCUIT FOR A 3-CELL STACK



A lower charge current is used for linear mode, in addition to a lower supply voltage. This reduces the power dissipation of Q1 to a manageable level. This dissipation must be closely considered in the application and proper heatsinking precautions must be taken. Different transistors may be selected for Q1 based on package size and thermal requirements. An 86kΩ resistor on R_T (R5) sets the FAST-CHARGE timeout to about 129 minutes, which for the given charge rate is appropriate for cells of about .9Ah capacity. The other aspects of the circuit are equivalent to those of the switchmode circuit.

Cell Stack Size Adjustment

R12 and R13 of the application circuits form a voltage divider such that the voltage of a single cell is present on the Vbatt pin. This is required for proper operation of the DS2715. Given a 100kΩ resistor for R13, adjust R12 as follows for the number of cells in the battery pack:

R12 = (Number of Cells -1) * R13

To charge 3-cell stacks, a value of 200kΩ is used for R12 for a 100kΩ R13.

It is important that the voltage seen by the Vbatt pin is relatively error free compared to the actual cell voltages in the battery pack. Any parasitic resistances in the connections between the battery cells and the resistor divider will cause errors that will increase with increasing charge current. The error seen by the Vbatt pin is the overall parasitic error divided by the number of cells. So, for a given parasitic resistance, it is more of a concern for circuits with a smaller number of cells. If parasitic resistances of a problematic level cannot be avoided, the connection location of the resistor divider can be manipulated to sense the true battery voltage, or the divider ratio can be adjusted to account for the sensed voltage error.

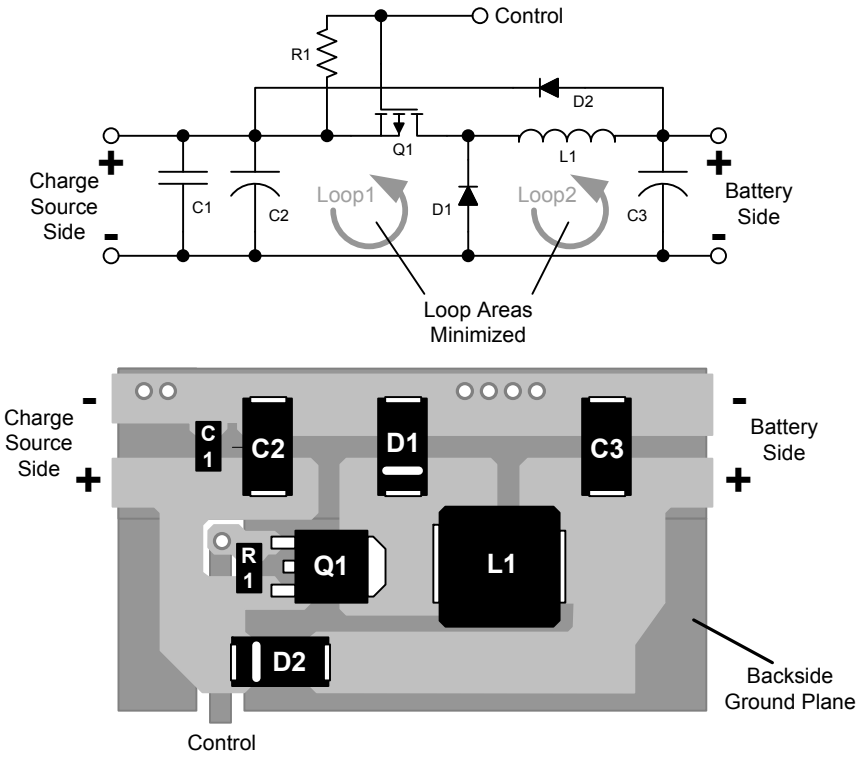
Application PCB Layout

Proper layout rules must be followed to ensure a successful application circuit. For all modes of operation, currents in excess of 1A may flow through the charge and discharge paths. All of these paths should be properly sized to handle the worst case current flow, whether that be from charging or from powering the load with the battery.

The linear mode of operation in some cases must dissipate large amounts of heat. This is typically accomplished with either an external heatsink on the regulating transistor, or through the use of PCB copper to spread the thermal energy that must be removed. Typically, for the TO-220 package transistor used in the application example, a 1 inch square area of 1oz. copper with the transistor firmly attached will have about a 50°C/W temperature rise. Utilizing 2oz. or heavier copper can improve this number by 20% or so. If better heatsinking is needed for the ergonomic or reliability aspects of the application, an add-on heatsink must be used.

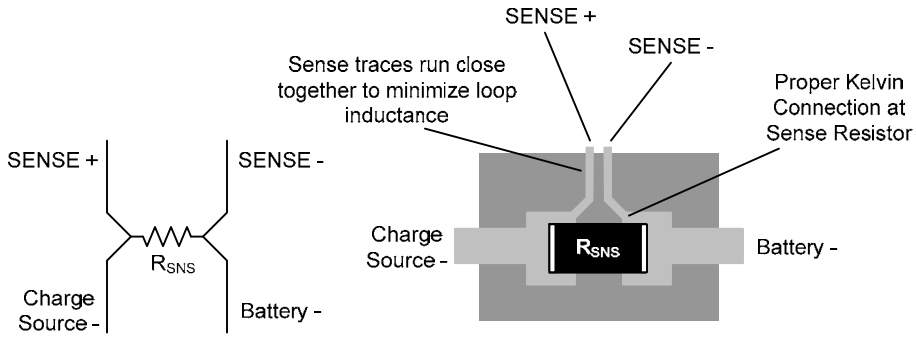
Switchmode operation presents its own unique challenges with fast voltage and current transients. Proper switchmode buck power supply layout should always be observed. Referring to the example circuit and layout of Figure 7, the loop labeled as Loop1 encompassing C1, C2, Q1 and D1 should be kept as small as possible to minimize the change in inductance that occurs when Q1 switches to the on state. Loop2 should also be minimized as much as practical, although it contains DC current components for the most part. The returning ground currents should be allowed to follow a path on a layer directly under the outgoing path since the high frequency components will try to follow the path of least impedance. Low ESR and ESL capacitors should be used when possible and for all capacitors 10uF and smaller. Typical surface mount ceramic types with a X5R or better dielectric are recommended.

Figure 7. Switching Circuit with Example Layout



Another important layout detail is the connection of the sense resistor. Proper Kelvin connection layout should be used to ensure the signal quality viewed by the sensing circuit inside the DS2715 is adequate. Figure 8 shows a recommended connection of the sense lines to the resistor footprint.

Figure 8. Sense Resistor Connection Layout



Package Information

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PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 SO	—	21-0041

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
011408	Various comprehensive changes.	1, 3, 4, 6–15
031609	Added device version DS2715B	1,4,7,8,10
042809	Updated *Ordering Information* table.	1