        - USB 2.0 (Type B)
        - Two HSMC connectors
    - Power and data converters
        - LT1963AES8: 2.5 to 1.5-A, low noise, fast transient response LDO regulators
        - LT1963AES8: 1.5-A, low noise, fast transient response LDO regulators
        - LT3481EDD: 36-V, 2-A, 2.8-MHz step-down switching regulator with 50-µA quiescent current
        - LT1761ES5-SD: 100-mA, low noise, LDO micropower regulators in SOT-23
        - LTC3418EUHF: 8-A, 4-MHz, monolithic synchronous step-down regulator
        - LTM4601EV: 12-A DC/DC µModule
        - LT1931AES5: 1.2/2.2-MHz inverting DC/DC converters in ThinSOT
        - LTC2402CMS: 1/2-Channel, 24-bit µPower no latency delta-sigma ADC in MSOP-10
- Data conversion HSMC
    - Dual 14-bit, 150-MSPS A/D converter
    - Dual 14-bit, 250-MSPS D/A converter
    - Audio in/out/mic
- Cyclone III FPGA Development Kit, CD-ROM
    - Design examples for the Cyclone III FPGA development board
    - Complete documentation
        - User guide
        - Reference manual
        - Board schematic and layout
        - Bill of materials (BOM)
        - Product and partner information
- MATLAB/Simulink evaluation software
- Intel® Complete Design Suite (download from Intel Download Center)
    - Quartus II design software
        - Subscription Edition (optional feature, available for purchase)
        - Web Edition (no charge, Windows only)
    - ModelSim®-Intel software
        - Intel Edition (optional feature, available for purchase)
        - Web Edition (no charge, Windows only)
    - MegaCore® IP Library including Nios® II processor —OpenCore Plus evaluation
    - Nios II Embedded Design Suite, Evaluation Edition (free)
    - Video demos of Quartus II software and the Nios II processor
    - System reference designs and labs
        - DSP Builder filtering design
        - Nios II processor reference designs

HSMC Interface

Intel developed the specification for the HSMC, which is based on the Samtec mechanical connector, to define and standardize the interface between optional daughtercards and host boards. This specification outlines both the electrical and mechanical properties of the interface between daughtercard and host. You can also create your own HSMC interface compatible daughtercards.

- Download High Speed Mezzanine Card (HSMC) Specification (PDF)

Figure 1. Cyclone III FPGA Development Board

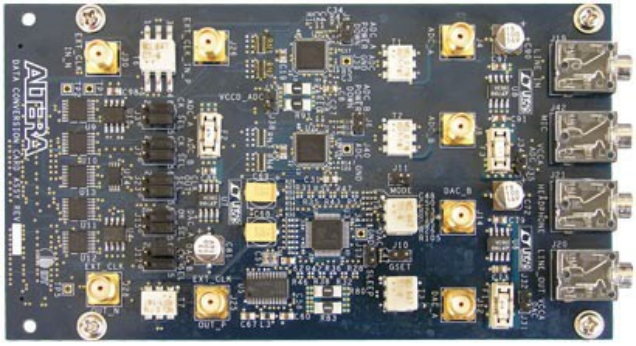

Figure 2. Cyclone III Data Conversion HSMC

Available Documentation

Table 3. Documents Available for the DSP Development Kit, Cyclone III Edition

Document	Description	Version
Kit Installation (via FTP)	**(Updated)** Full installation of all files including reference manual, user guide, quick start guide, demos and tutorials, BOM, layout, PCB, schematics, Board Update Portal example file, Board Test System example file, and others	12.1.0 (1)
Kit Installation (via FTP)	**(Archive)** Full installation of all files including reference manual, user guide, quick start guide, demos and tutorials, BOM, layout, PCB, schematics, Board Update Portal example file, Board Test System example file, and others	12.0.0 (2)
Kit Installation (via FTP)	**(Archive)** Full installation of all files including reference manual, user guide, quick start guide, demos and tutorials, BOM, layout, PCB, schematics, Board Update Portal example file, Board Test System example file, and others	11.1.0 (3)
Kit Installation (via FTP)	**(Archive)** Full installation of all files including reference manual, user guide, quick start guide, demos and tutorials, BOM, layout, PCB, schematics, Board Update Portal example file, Board Test System example file, and others	11.0.0 (4)
Kit Installation (via FTP)	**(Archive)** Full installation of all files including reference manual, user guide, quick start guide, demos and tutorials, BOM, layout,PCB, schematics, Board Update Portal example file, Board Test System example file, and others	7.2.0 (5)

Notes:

1. This kit installation works with Quartus II design software version 12.1.0.
2. This kit installation works with Quartus II design software version 12.0.0.
3. This kit installation works with Quartus II design software version 11.1.0.
4. This kit installation works with Quartus II design software version 11.0.0.
5. This kit installation works with Quartus II design software version 7.2.0

Errata

There are two known errata on this development kit. The problems are with the on-board power monitor circuitry and a reset issue with the embedded USB-Blaster™ circuitry. Both bugs can be fixed by downloading an updated MAX® II CPLD programming file.

To see if your board needs the updated programming file press and hold the CPU_RESET pushbutton. If the Power Display does not show “1337” or higher or it shows nothing at all, then your board should be upgraded to the new programming file. Click here to download a zip file containing the files need to upgrade your board. Follow the instructions in the **max2_upgrade_instructions.txt** text file.

Related Links

- Other Cyclone III FPGA-based development kits
- AN 466: Cyclone III Design Guidelines (PDF)

- Quartus II design software
- Literature for low-cost Cyclone III FPGAs
- Nios II 32-bit embedded processor solutions
- DSP in Cyclone III FPGAs
- Power Management Center for Altera devices