ADM690–ADM695–SPECIFICATIONS

(V_{CC} = Full Operating Range, V_{BATT} = +2.8 V, T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
BATTERY BACKUP SWITCHING					
V_{CC} Operating Voltage Range					
ADM690, ADM691, ADM694, ADM695	4.75		5.5	V	
ADM692, ADM693	4.5		5.5	V	
V_{BATT} Operating Voltage Range					
ADM690, ADM691, ADM694, ADM695	2.0		4.25	V	
ADM692, ADM693	2.0		4.0	V	
V_{OUT} Output Voltage	V_{CC} – 0.05	V_{CC} – 0.025		V	I_{OUT} = 1 mA
	V_{CC} – 0.5	V_{CC} – 0.25		V	I_{OUT} ≤ 100 mA
V_{OUT} in Battery Backup Mode	V_{BATT} – 0.05	V_{BATT} – 0.02		V	I_{OUT} = 250 µA, V_{CC} < V_{BATT} – 0.2 V
Supply Current (Excludes I_{OUT})		1	1.95	mA	I_{OUT} = 100 mA
Supply Current in Battery Backup Mode		0.6	1	µA	V_{CC} = 0 V, V_{BATT} = 2.8 V
Battery Standby Current					5.5 V > V_{CC} > V_{BATT} + 0.2 V
(+ = Discharge, – = Charge)	–0.1		+0.02	µA	T_A = +25°C
	–1.0		+0.02	µA	
Battery Switchover Threshold		70		mV	Power Up
V_{CC} – V_{BATT}		50		mV	Power Down
Battery Switchover Hysteresis		20		mV	
BATT ON Output Voltage			0.3	V	I_{SINK} = 3.2 mA
BATT ON Output Short Circuit Current		35		mA	BATT ON = V_{OUT} = 4.5 V Sink Current
	0.5	1	25	µA	BATT ON = 0 V Source Current
RESET AND WATCHDOG TIMER					
Reset Voltage Threshold					
ADM690, ADM691, ADM694, ADM695	4.5	4.65	4.73	V	
ADM692, ADM693	4.25	4.4	4.48	V	
Reset Threshold Hysteresis		40		mV	
Reset Timeout Delay					
ADM690, ADM691, ADM692, ADM693	35	50	70	ms	OSC SEL = HIGH, V_{CC} = 5 V, T_A = +25°C
ADM694, ADM695	140	200	280	ms	OSC SEL = HIGH, V_{CC} = 5 V, T_A = +25°C
Watchdog Timeout Period, Internal Oscillator	1.0	1.6	2.25	s	Long Period, V_{CC} = 5 V, T_A = +25°C
	70	100	140	ms	Short Period, V_{CC} = 5 V, T_A = +25°C
Watchdog Timeout Period, External Clock	3840		4097	Cycles	Long Period
	768		1025	Cycles	Short Period
Minimum WDI Input Pulse Width	50			ns	V_{IL} = 0.4, V_{IH} = 3.5 V
$\overline{RESET}$ Output Voltage @ V_{CC} = +1 V		4	200	mV	I_{SINK} = 10 µA, V_{CC} = 1 V
$\overline{RESET}$, $\overline{LOW\ LINE}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{CC} = 4.25 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 5 V
$\overline{RESET}$, $\overline{WDO}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{CC} = 5 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 4.25 V
Output Short Circuit Source Current	1	3	25	µA	
Output Short Circuit Sink Current		25		mA	
WDI Input Threshold					V_{CC} = 5 V[1]
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current		20	50	µA	WDI = V_{OUT}, T_A = +25°C
	–50	–15		µA	WDI = 0 V, T_A = +25°C
POWER FAIL DETECTOR					
PFI Input Threshold	1.25	1.3	1.35	V	V_{CC} = +5 V
PFI Input Current	–25	±0.01	+25	nA	
$\overline{PFO}$ Output Voltage			0.4	V	I_{SINK} = 3.2 mA
	3.5			V	I_{SOURCE} = 1 µA
$\overline{PFO}$ Short Circuit Source Current	1	3	25	µA	PFI = Low, $\overline{PFO}$ = 0 V
$\overline{PFO}$ Short Circuit Sink Current		25		mA	PFI = High, $\overline{PFO}$ = V_{OUT}
CHIP ENABLE GATING					
$\overline{CE}_{IN}$ Threshold			0.8	V	V_{IL}
	3.0			V	V_{IH}
$\overline{CE}_{IN}$ Pull-Up Current		3		µA	
$\overline{CE}_{OUT}$ Output Voltage			0.4	V	I_{SINK} = 3.2 mA
	V_{OUT} – 1.5			V	I_{SOURCE} = 3.0 mA
	V_{OUT} – 0.05			V	I_{SOURCE} = 1 µA, V_{CC} = 0 V
$\overline{CE}$ Propagation Delay		5	9	ns	

Downloaded from Arrow.com.

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
OSCILLATOR					
OSC IN Input Current		±2		µA	
OSC SEL Input Pull-Up Current		5		µA	
OSC IN Frequency Range	0		250	kHz	OSC SEL = 0 V
OSC IN Frequency with External Capacitor		4		kHz	OSC SEL = 0 V, C_{OSC} = 47 pF

NOTE
[1]WDI is a three level input which is internally biased to 38% of V_{CC} and has an input impedance of approximately 125 kΩ.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} . . . . . –0.3 V to +6 V
V_{BATT} . . . . . –0.3 V to +6 V
All Other Inputs . . . . . –0.3 V to V_{OUT} + 0.5 V
Input Current
  V_{CC} . . . . . 200 mA
  V_{BATT} . . . . . 50 mA
  GND . . . . . 20 mA
Digital Output Current . . . . . 20 mA
Power Dissipation, N-8 DIP . . . . . 400 mW
  θ_{JA} Thermal Impedance . . . . . 120°C/W
Power Dissipation, Q-8 DIP . . . . . 500 mW
  θ_{JA} Thermal Impedance . . . . . 125°C/W
Power Dissipation, N-16 DIP . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 135°C/W
Power Dissipation, Q-16 DIP . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 100°C/W
Power Dissipation, R-16 SOIC . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 110°C/W
Operating Temperature Range
  Industrial (A Version) . . . . . –40°C to +85°C
  Extended (S Version) . . . . . –55°C to +125°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
  Vapor Phase (60 secs) . . . . . +215°C
  Infrared (15 secs) . . . . . +220°C
Storage Temperature Range . . . . . –65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option
ADM690AN	–40°C to +85°C	N-8
ADM690AQ	–40°C to +85°C	Q-8
ADM690SQ	–55°C to +125°C	Q-8
ADM691AN	–40°C to +85°C	N-16
ADM691AR	–40°C to +85°C	R-16
ADM691AQ	–40°C to +85°C	Q-16
ADM691SQ	–55°C to +125°C	Q-16
ADM692AN	–40°C to +85°C	N-8
ADM692AQ	–40°C to +85°C	Q-8
ADM692SQ	–55°C to +125°C	Q-8
ADM693AN	–40°C to +85°C	N-16
ADM693AR	–40°C to +85°C	R-16
ADM693AQ	–40°C to +85°C	Q-16
ADM693SQ	–55°C to +125°C	Q-16
ADM694AN	–40°C to +85°C	N-8
ADM694AQ	–40°C to +85°C	Q-8
ADM694SQ	–55°C to +125°C	Q-8
ADM695AN	–40°C to +85°C	N-16
ADM695AR	–40°C to +85°C	R-16
ADM695AQ	–40°C to +85°C	Q-16
ADM695SQ	–55°C to +125°C	Q-16

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM690–ADM695 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

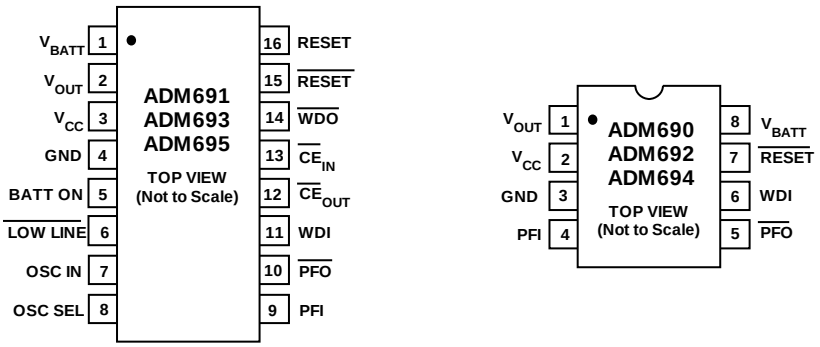
Downloaded from Arrow.com.

PIN FUNCTION DESCRIPTION

Mnemonic	Function
V_{CC}	Power Supply Input: +5 V Nominal.
V_{BATT}	Backup Battery Input. Connect to Ground if a backup battery is not used.
V_{OUT}	Output Voltage, V_{CC} or V_{BATT} is internally switched to V_{OUT} depending on which is at the highest potential. V_{OUT} can supply up to 100 mA to power CMOS RAM. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used.
GND	0 V. Ground reference for all signals.
$\overline{\text{RESET}}$	Logic Output. $\overline{\text{RESET}}$ goes low if 1. V_{CC} falls below the Reset Threshold 2. V_{CC} falls below V_{BATT} 3. The watchdog timer is not serviced within its timeout period. The reset threshold is typically 4.65 V for the ADM690/ADM691/ADM694/ADM695 and 4.4 V for the ADM692 and ADM693. $\overline{\text{RESET}}$ remains low for 50 ms (ADM690/ADM691/ADM692/ADM693) or 200 ms (ADM694/ADM695) after V_{CC} returns above the threshold. $\overline{\text{RESET}}$ also goes low for 50 (200) ms if the watchdog timer is enabled but not serviced within its timeout period. The $\overline{\text{RESET}}$ pulse width can be adjusted on the ADM691/ADM693/ADM695 as shown in Table I. The $\overline{\text{RESET}}$ output has an internal 3 μA pull up, and can either connect to an open collector Reset bus or directly drive a CMOS gate without an external pull-up resistor.
WDI	Watchdog Input. WDI is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{\text{RESET}}$ pulses low and WDO goes low. The timer resets with each transition on the WDI line. The watchdog timer may be disabled if WDI is left floating or is driven to midsupply.
PFI	Power Fail Input. PFI is the noninverting input to the Power Fail Comparator when PFI is less than 1.3 V, $\overline{\text{PFO}}$ goes low. Connect PFI to GND or V_{OUT} when not used.
$\overline{\text{PFO}}$	Power Fail Output. $\overline{\text{PFO}}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.3 V. The comparator is turned off and $\overline{\text{PFO}}$ goes low when V_{CC} is below V_{BATT}.
$\overline{\text{CE}}_{IN}$	Logic Input. The input to the $\overline{\text{CE}}$ gating circuit. Connect to GND or V_{OUT} if not used.
$\overline{\text{CE}}_{OUT}$	Logic Output. $\overline{\text{CE}}_{OUT}$ is a gated version of the $\overline{\text{CE}}_{IN}$ signal. $\overline{\text{CE}}_{OUT}$ tracks $\overline{\text{CE}}_{IN}$ when V_{CC} is above the reset threshold. If V_{CC} is below the reset threshold, $\overline{\text{CE}}_{OUT}$ is forced high. See Figures 5 and 6.
BATT ON	Logic Output. BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 35 mA and can directly drive the base of an external PNP transistor to increase the output current above the 100 mA rating of V_{OUT}.
$\overline{\text{LOW LINE}}$	Logic Output. $\overline{\text{LOW LINE}}$ goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold.
RESET	Logic Output. RESET is an active high output. It is the inverse of $\overline{\text{RESET}}$.
OSC SEL	Logic Oscillator Select Input. When OSC SEL is unconnected (floating) or driven high, the internal oscillator sets the reset active time and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3 μA internal pull up, (see Table I).
OSC IN	Oscillator Logic Input. With OSC SEL low, OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND. This sets both the reset active pulse timing and the watchdog timeout period (see Table I and Figure 4). With OSC SEL high or floating, the internal oscillator is enabled and the reset active time is fixed at 50 ms typ. (ADM691/ADM693) or 200 ms typ (ADM695). In this mode the OSC IN pin selects between fast (100 ms) and slow (1.6 s) watchdog timeout periods. In both modes, the timeout period immediately after a reset is 1.6 s typical.
$\overline{\text{WDO}}$	Logic Output. The Watchdog Output, $\overline{\text{WDO}}$, goes low if WDI remains either high or low for longer than the watchdog timeout period. $\overline{\text{WDO}}$ is set high by the next transition at WDI. If WDI is unconnected or at midsupply, the watchdog timer is disabled and $\overline{\text{WDO}}$ remains high. $\overline{\text{WDO}}$ also goes high when $\overline{\text{LOW LINE}}$ goes low.

Downloaded from Arrow.com.

PIN CONFIGURATIONS



PRODUCT SELECTION GUIDE

Part Number	Nominal Reset Time	Nominal V_{CC} Reset Threshold	Nominal Watchdog Timeout Period	Battery Backup Switching	Base Drive Ext PNP	Chip Enable Signals
ADM690	50 ms	4.65 V	1.6 s	Yes	No	No
ADM691	50 ms or ADJ	4.65 V	100 ms, 1.6 s, ADJ	Yes	Yes	Yes
ADM692	50 ms	4.4 V	1.6 s	Yes	No	No
ADM693	50 ms or ADJ	4.4 V	100 ms, 1.6 s, ADJ	Yes	Yes	Yes
ADM694	200 ms	4.65 V	1.6 s	Yes	No	No
ADM695	200 ms or ADJ	4.65 V	100 ms, 1.6 s, ADJ	Yes	Yes	Yes

CIRCUIT INFORMATION

Battery Switchover Section

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50 mV higher than V_{BATT} as V_{CC} falls, and when V_{CC} is 70 mV greater than V_{BATT} as V_{CC} rises. This 20 mV of hysteresis prevents repeated rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

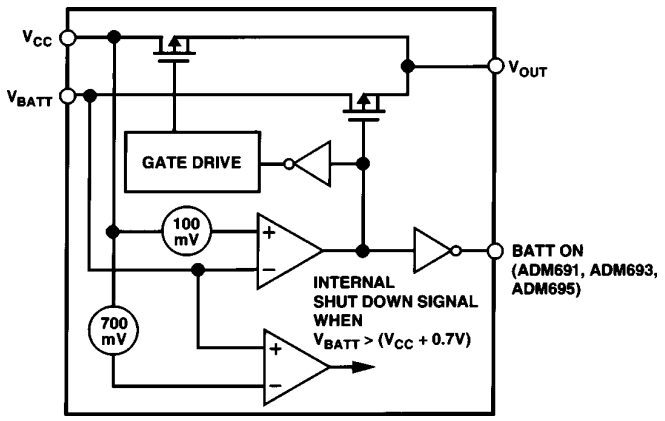


Figure 1. Battery Switchover Schematic

During normal operation with V_{CC} higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via an internal PMOS transistor switch. This switch has a typical on-resistance of 1.5 Ω and can supply up to 100 mA at the V_{OUT} terminal. V_{OUT} is normally used to drive a RAM memory bank which may require instantaneous currents of greater than 100 mA. If this is the case then a bypass capacitor should be connected to V_{OUT}. The capacitor will provide the peak current transients to the RAM. A capacitance value of 0.1 µF or greater may be used.

If the continuous output current requirement at V_{OUT} exceeds 100 mA or if a lower V_{CC}–V_{OUT} voltage differential is desired, an external PNP pass transistor may be connected in parallel with the internal transistor. The BATT ON output (ADM691/ADM693/ADM695) can directly drive the base of the external transistor.

A 20 Ω MOSFET switch connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery back up of CMOS RAM or other low power CMOS circuitry. The supply current in battery back up is typically 0.6 µA.

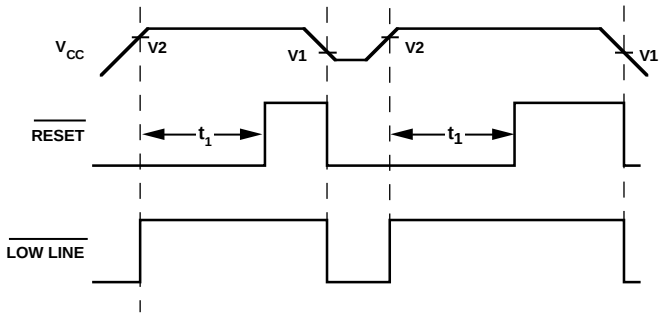
The ADM690/ADM691/ADM694/ADM695 operates with battery voltages from 2.0 V to 4.25 V and the ADM692/ADM693 operates with battery voltages from 2.0 V to 4.0 V. High value capacitors, either standard electrolytic or the farad size double layer capacitors, can also be used for short-term memory back up. A small charging current of typically 10 nA (0.1 µA max) flows out of the V_{BATT} terminal. This current is useful for maintaining rechargeable batteries in a fully charged condition. This extends the life of the back up battery by compensating for its self discharge current. Also note that this current poses no problem when lithium batteries are used for back up since the maximum charging current (0.1 µA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, V_{BATT} should be connected to GND and V_{OUT} should be connected to V_{CC}.

Downloaded from Arrow.com.

POWER FAIL $\overline{\text{RESET}}$ OUTPUT

$\overline{\text{RESET}}$ is an active low output which provides a $\overline{\text{RESET}}$ signal to the Microprocessor whenever V_{CC} is at an invalid level. When V_{CC} falls below the reset threshold, the $\overline{\text{RESET}}$ output is forced low. The nominal reset voltage threshold is 4.65 V (ADM690/ ADM691/ADM694/ADM695) or 4.4 V (ADM692/ADM693).



t_1 = RESET TIME.
V1 = RESET VOLTAGE THRESHOLD LOW
V2 = RESET VOLTAGE THRESHOLD HIGH
HYSTERESIS = V2–V1

Figure 2. Power Fail Reset Timing

On power-up $\overline{\text{RESET}}$ will remain low for 50 ms (200 ms for ADM694 and ADM695) after V_{CC} rises above the appropriate reset threshold. This allows time for the power supply and microprocessor to stabilize. On power-down, the $\overline{\text{RESET}}$ output remains low with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition.

This $\overline{\text{RESET}}$ active time is adjustable on the ADM691/ADM693/ ADM695 by using an external oscillator or by connecting an external capacitor to the OSC IN pin. Refer to Table I and Figure 4.

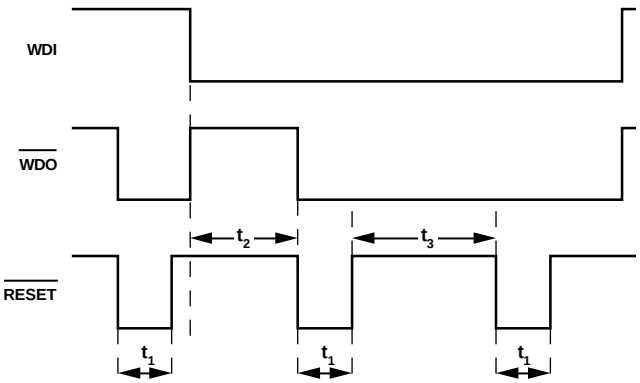
The guaranteed minimum and maximum thresholds of the ADM690/ADM691/ADM694/ADM695 are 4.5 V and 4.73 V, while the guaranteed thresholds of the ADM692/ADM693 are 4.25 V and 4.48 V. The ADM690/ADM691/ADM694/ADM695 is, therefore, compatible with 5 V supplies with a +10%, –5% tolerance while the ADM692/ADM693 is compatible with 5 V ± 10% supplies. The reset threshold comparator has approximately 50 mV of hysteresis. The response time of the reset voltage comparator is less than 1 µs. If glitches are present on the V_{CC} line which could cause spurious reset pulses, then V_{CC} should be decoupled close to the device.

In addition to $\overline{\text{RESET}}$ the ADM691/ADM693/ADM695 contain an active high $\overline{\text{RESET}}$ output. This is the complement of $\overline{\text{RESET}}$ and is intended for processors requiring an active high RESET signal.

Watchdog Timer $\overline{\text{RESET}}$

The watchdog timer circuit monitors the activity of the microprocessor in order to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the Watchdog Input (WDI) line. If this line is not toggled within the selected timeout period, a $\overline{\text{RESET}}$ pulse is generated. The nominal watchdog timeout period is preset at 1.6 seconds on the ADM690/ADM692/ADM694. The ADM691/ADM693/ADM695 may be configured for either a fixed “short” 100 ms or a “long” 1.6 second timeout period or for an adjustable timeout period. If the “short” period is selected, some systems may be unable to service the watchdog timer immediately after a reset, so the ADM691/ADM693/ADM695 automatically selects the “long” timeout period directly after a reset is issued. The watchdog timer is restarted at the end of reset, whether the reset was caused by lack of activity on WDI or by V_{CC} falling below the reset threshold.

The normal (short) timeout period becomes effective following the first transition of WDI after $\overline{\text{RESET}}$ has gone inactive. The watchdog timeout period restarts with each transition on the WDI pin. To ensure that the watchdog timer does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur at or less than the minimum timeout period. If WDI remains permanently either high or low, reset pulses will be issued after each “long” timeout period (1.6 s). The watchdog monitor can be deactivated by floating the Watchdog Input (WDI) or by connecting it to midsupply.



t_1 = RESET TIME.
t_2 = NORMAL (SHORT) WATCHDOG TIMEOUT PERIOD.
t_3 = WATCHDOG TIMEOUT PERIOD IMMEDIATELY FOLLOWING A RESET.

Figure 3. Watchdog Timeout Period and Reset Active Time

Downloaded from Arrow.com.

Table I. ADM691, ADM693, ADM695 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Active Period	
		Normal	Immediately After Reset	ADM691/ADM693	ADM695
Low	External Clock Input	1024 CLKS	4096 CLKS	512 CLKS	2048 CLKS
Low	External Capacitor	260 ms × C/47 pF	1.04 s × C/47 pF	130 ms × C/47 pF	520 ms × C/47 pF
Floating or High	Low	100 ms	1.6 s	50 ms	200 ms
Floating or High	Floating or High	1.6 s	1.6 s	50 ms	200 ms

NOTE
With the OSC SEL pin low, OSC IN can be driven by an external clock signal, or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24 kHz. The nominal oscillator frequency with external capacitor is: F_{OSC} (Hz) = 184,000/C (pF).

The watchdog timeout period is fixed at 1.6 seconds, and the reset pulse width is fixed at 50 ms on the ADM690/ADM692. On the ADM694 the watchdog timeout period is also 1.6 seconds but the reset pulse width is fixed at 200 ms. The ADM691/ADM693/ADM695 allow these times to be adjusted as shown in Table I. Figure 4 shows the various oscillator configurations which can be used to adjust the reset pulse width and watchdog timeout period.

The internal oscillator is enabled when OSC SEL is high or floating. In this mode, OSC IN selects between the 1.6 second and 100 ms watchdog timeout periods. With OSC IN connected high or floating, the 1.6 second timeout period is selected; while with it connected low, the 100 ms timeout period is selected. In either case, immediately after a reset, the timeout period is 1.6 seconds. This gives the microprocessor time to reinitialize the system. If OSC IN is low, then the 100 ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70 ms.

Watchdog Output (WDO)
The Watchdog Output $\overline{WDO}$ (ADM691/ADM693/ADM695) provides a status output which goes low if the watchdog timer "times out" and remains low until set high by the next transition on the Watchdog Input. $\overline{WDO}$ is also set high when V_{CC} goes below the reset threshold.

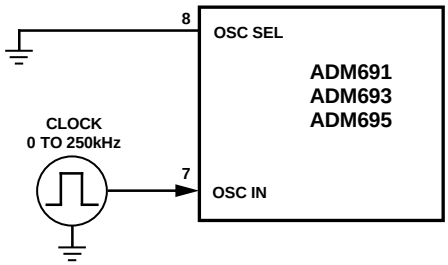


Figure 4a. External Clock Source

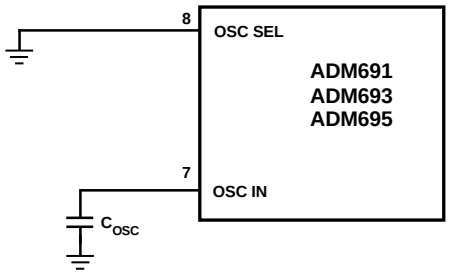


Figure 4b. External Capacitor

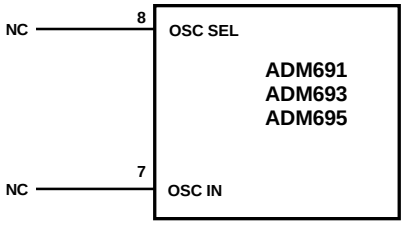


Figure 4c. Internal Oscillator (1.6 Second Watchdog)

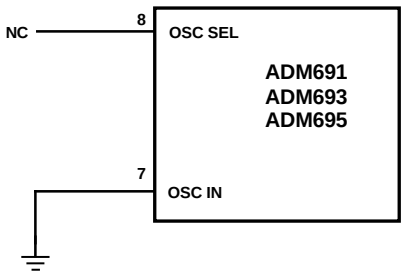


Figure 4d. Internal Oscillator (100 ms Watchdog)

Downloaded from Arrow.com.

$\overline{CE}$ Gating and RAM Write Protection (ADM691/ADM693/ADM695)

The ADM691/ADM693/ADM695 products include memory protection circuitry which ensures the integrity of data in memory by preventing write operations when V_{CC} is at an invalid level. There are two additional pins, $\overline{CE}_{IN}$ and $\overline{CE}_{OUT}$, which may be used to control the Chip Enable or Write inputs of CMOS RAM. When V_{CC} is present, $\overline{CE}_{OUT}$ is a buffered replica of $\overline{CE}_{IN}$, with a 5 ns propagation delay. When V_{CC} falls below the reset voltage threshold or V_{BATT}, an internal gate forces $\overline{CE}_{OUT}$ high, independent of $\overline{CE}_{IN}$.

$\overline{CE}_{OUT}$ typically drives the $\overline{CE}$, $\overline{CS}$, or write input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{CE}_{OUT}$ to drive the store or write inputs.

If the 5 ns typical propagation delay of $\overline{CE}_{OUT}$ is excessive, connect $\overline{CE}_{IN}$ to GND and use the resulting $\overline{CE}_{OUT}$ to control a high speed external logic gate.

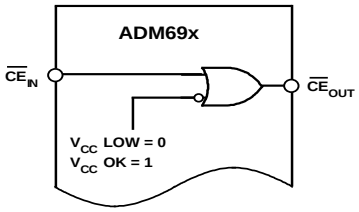


Figure 5. Chip Enable Gating

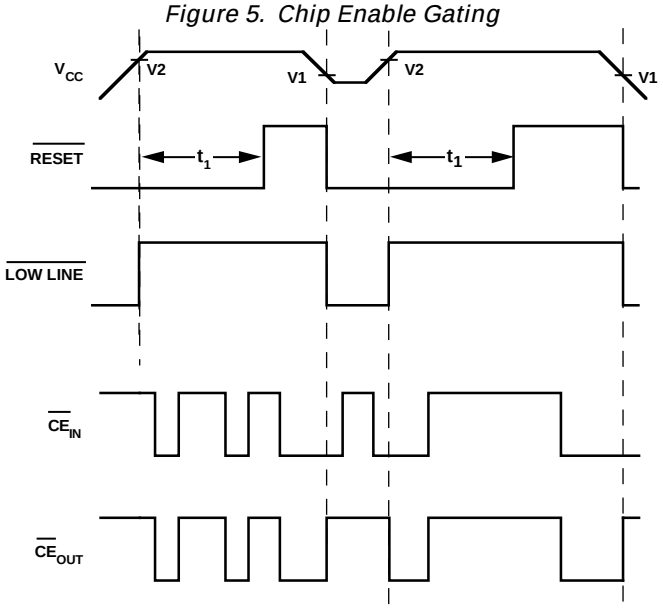


Figure 6. Chip Enable Timing

Power Fail Warning Comparator

An additional comparator is provided for early warning of failure in the microprocessor's power supply. The Power Fail Input (PFI) is compared to an internal +1.3 V reference. The Power Fail Output ($\overline{PFO}$) goes low when the voltage at PFI is less than 1.3 V. Typically PFI is driven by an external voltage divider which senses either the unregulated dc input to the system's 5 V regulator or the regulated 5 V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3 V several milliseconds before the +5 V power supply falls below the reset threshold. $\overline{PFO}$ is normally used to interrupt the microprocessor so that data can be stored in RAM and the shut down procedure executed before power is lost

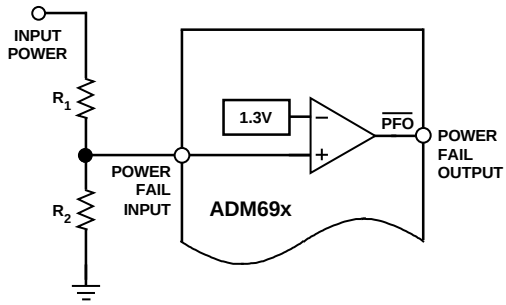


Figure 7. Power Fail Comparator

Table II. Input and Output Status In Battery Backup Mode

Signal	Status
V_{OUT}	V_{OUT} is connected to V_{BATT} via an internal PMOS switch.
$\overline{RESET}$	Logic low.
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low.
BATT ON	Logic high. The open circuit voltage is equal to V_{OUT}.
WDI	WDI is ignored. It is internally disconnected from the internal pull-up resistor and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{WDO}$	Logic high. The open circuit voltage is equal to V_{OUT}.
PFI	The Power Fail Comparator is turned off and has no effect on the Power Fail Output.
$\overline{PFO}$	Logic low.
$\overline{CE}_{IN}$	$\overline{CE}_{IN}$ is ignored. It is internally disconnected from its internal pull-up and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{CE}_{OUT}$	Logic high. The open circuit voltage is equal to V_{OUT}.
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.

Downloaded from Arrow.com.

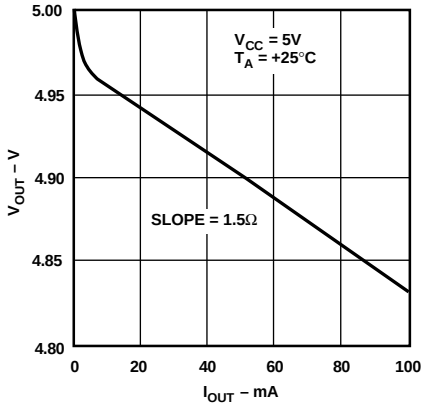


Figure 8. V_{OUT} vs. I_{OUT} Normal Operation

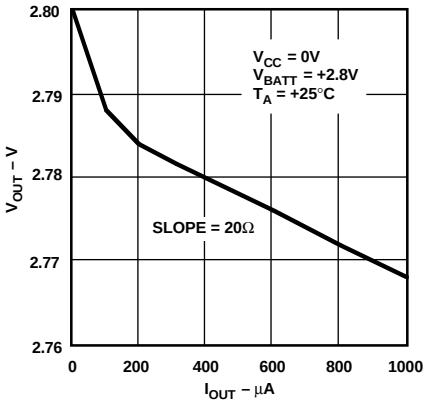


Figure 9. V_{OUT} vs. I_{OUT} Battery Backup

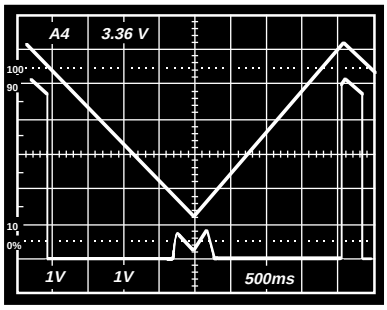


Figure 10. Reset Output Voltage vs. Supply Voltage

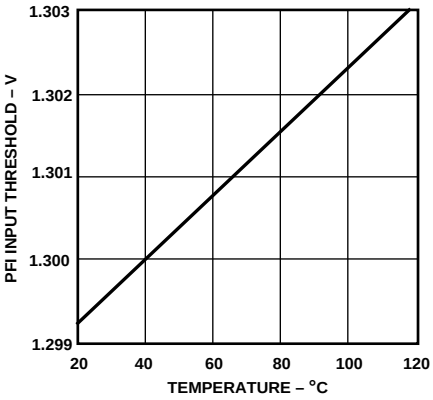


Figure 11. PFI Input Threshold vs. Temperature

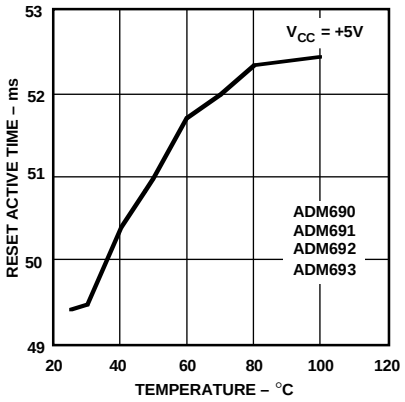


Figure 12. Reset Active Time vs. Temperature

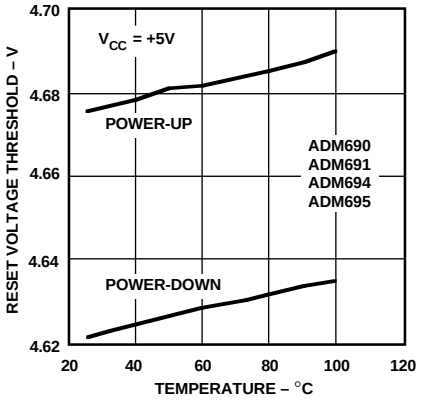


Figure 13. Reset Voltage Threshold vs. Temperature

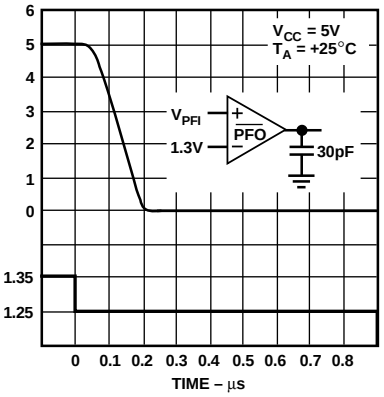


Figure 14. Power Fail Comparator Response Time

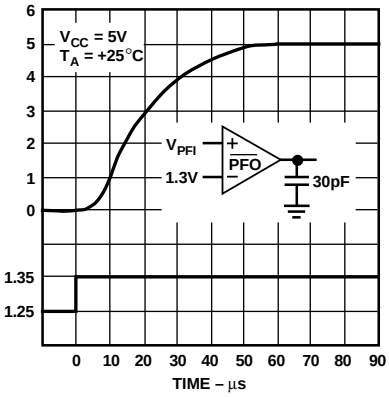


Figure 15. Power Fail Comparator Response Time

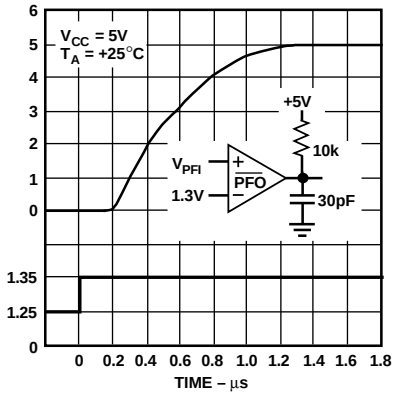


Figure 16. Power Fail Comparator Response Time with Pull-Up Resistor

Downloaded from Arrow.com.

+APPLICATION INFORMATION

Increasing the Drive Current

If the continuous output current requirements at V_{OUT} exceed 100 mA or if a lower V_{CC}–V_{OUT} voltage differential is desired, an external PNP pass transistor may be connected in parallel with the internal transistor. The BATT ON output (ADM691/ ADM693/ADM695) can directly drive the base of the external transistor.

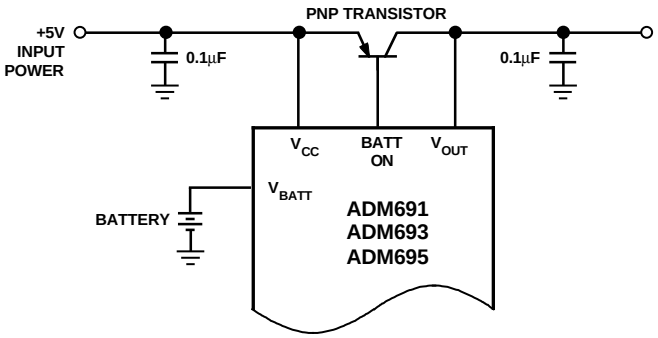


Figure 17. Increasing the Drive Current

Using a Rechargeable Battery for Back Up

If a capacitor or a rechargeable battery is used for back up then the charging resistor should be connected to V_{OUT} since this eliminates the discharge path that would exist during power down if the resistor is connected to V_{CC}.

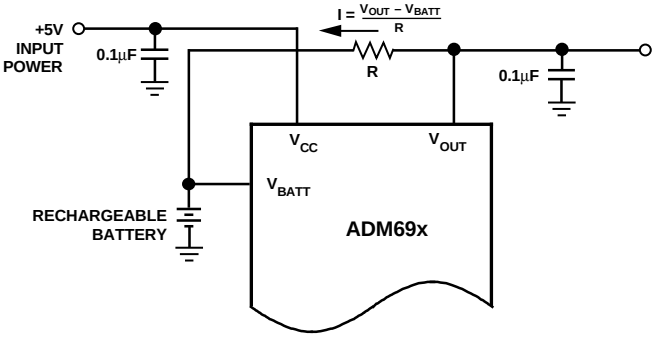


Figure 18. Rechargeable Battery

Adding Hysteresis to the Power Fail Comparator

For increased noise immunity, hysteresis may be added to the power fail comparator. Since the comparator circuit is noninverting, hysteresis can be added simply by connecting a resistor between the $\overline{PFO}$ output and the PFI input as shown in Figure 19.

When $\overline{PFO}$ is low, resistor R_3 sinks current from the summing junction at the PFI pin. When $\overline{PFO}$ is high, the series combination of R_3 and R_4 source current into the PFI summing junction. This results in differing trip levels for the comparator.

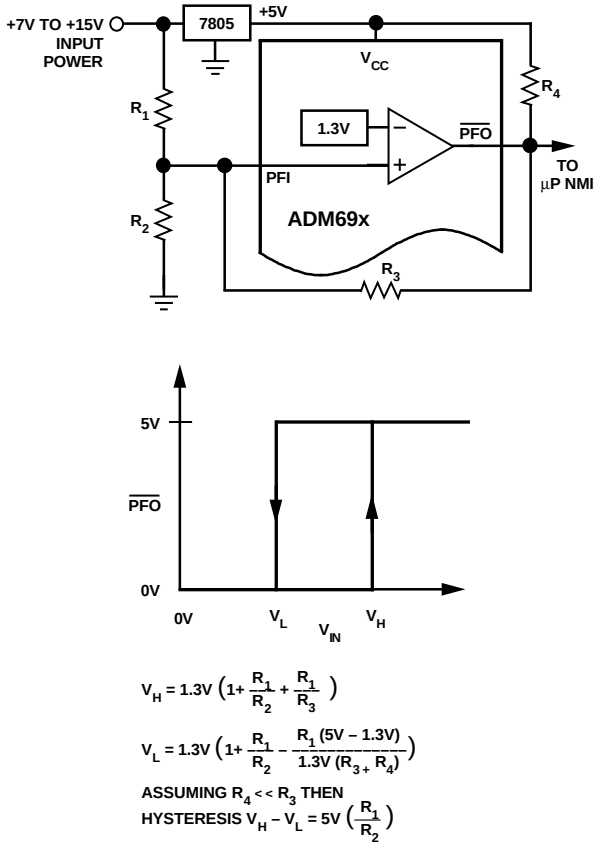


Figure 19. Adding Hysteresis to the Power Fail Comparator

Monitoring the Status of the Battery

The power fail comparator can be used to monitor the status of the backup battery instead of the power supply if desired. This is shown in Figure 20. The PFI input samples the battery voltage and generates an active low $\overline{PFO}$ signal when the battery voltage drops below a chosen threshold. It may be necessary to apply a test load in order to determine the loaded battery voltage. This can be done under processor control using $\overline{CE}_{OUT}$. Since $\overline{CE}_{OUT}$ is forced high during the battery backup mode, the test load will not be applied to the battery while it is in use, even if the microprocessor is not powered.

Downloaded from Arrow.com.

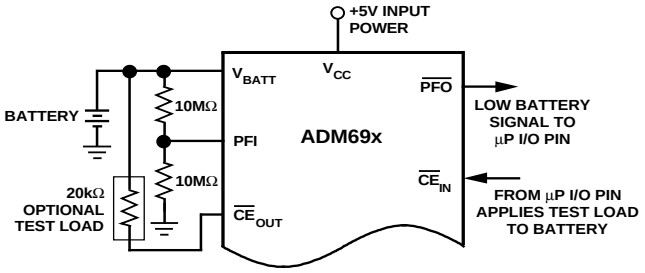


Figure 20. Monitoring the Battery Status

Alternate Watchdog Input Drive Circuits

The watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer (Figure 21a). When three-stated, the WDI input will float thereby disabling the watchdog timer.

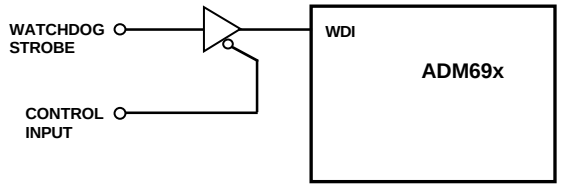


Figure 21a. Programming the Watchdog Input

This circuit is not entirely foolproof, and it is possible that a software fault could erroneously 3-state the buffer. This would then prevent the ADM69x from detecting that the microprocessor is no longer operating correctly. In most cases a better method is to extend the watchdog period rather than disabling the watchdog. This may be done under program control using the circuit shown in Figure 21b. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01 µF capacitor sets a watchdog timeout delay of 100 seconds. When the control input is low, the OSC SEL pin is driven high, selecting the internal oscillator. The 100 ms or the 1.6 s period is chosen, depending on which diode in Figure 21b is used. With D1 inserted the internal timeout is set at 100 ms, while with D2 inserted the timeout is set at 1.6 s.

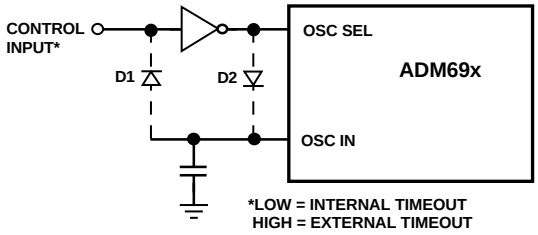


Figure 21b. Programming the Watchdog Input

Replacing the Backup Battery

When changing the backup battery with system power on, spurious resets can occur when the battery is removed. This occurs because the leakage current flowing out of the V_{BATT} pin will charge up the stray capacitance. If the voltage on V_{BATT} reaches within 50 mV of V_{CC}, a reset pulse is generated.

If spurious resets during battery replacement are acceptable, then no action is required. If not, then one of the following solutions should be considered:

1. A capacitor from V_{BATT} to GND. This gives time while the capacitor is charging up to replace the battery. The leakage current will charge up the external capacitor towards the V_{CC} level. The time taken is related to the charging current, the size of external capacitor and the voltage differential between the capacitor and the charging voltage supply.

$$t = C_{EXT} \times V_{DIFF}/I$$

The maximum leakage (charging) current is 1 µA over temperature and $V_{DIFF} = V_{CC}–V_{BATT}$. Therefore, the capacitor size should be chosen such that sufficient time is available to make the battery replacement.

$$C_{EXT} = T_{REQD}\ (1\ \mu A/(V_{CC}–V_{BATT}))$$

If a replacement time of 5 seconds is allowed and assuming a V_{CC} of 4.5 V and a V_{BATT} of 3 V

$$C_{EXT} = 3.33\ \mu F$$

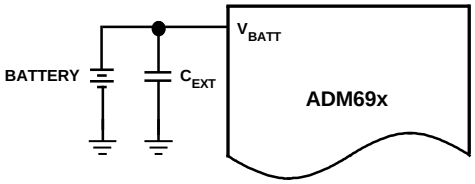


Figure 22a. Preventing Spurious RESETS During Battery Replacement

2. A resistor from V_{BATT} to GND. This will prevent the voltage on V_{BATT} from rising to within 50 mV of V_{CC} during battery replacement.

Downloaded from Arrow.com.

$$R = (V_{CC} - 50\ mV)/1\ \mu A$$

Note that the resistor will discharge the battery slightly. With a V_{CC} supply of 4.5 V, a suitable resistor is 4.3 MΩ. With a 3 V battery this will draw around 700 nA. This will be negligible in most cases.

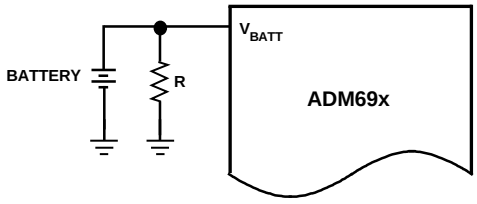


Figure 22b. Preventing Spurious RESETS During Battery Replacement

TYPICAL APPLICATIONS

ADM690, ADM692 AND ADM694

Figure 23 shows the ADM690/ADM692/ADM694 in a typical power monitoring, battery backup application. V_{OUT} powers the CMOS RAM. Under normal operating conditions with V_{CC} present, V_{OUT} is internally connected to V_{CC}. If a power failure occurs, V_{CC} will decay and V_{OUT} will be switched to V_{BATT} thereby maintaining power for the CMOS RAM. A $\overline{\text{RESET}}$ pulse is also generated when V_{CC} falls below 4.65 V for the ADM690/ADM694 or 4.4 V for the ADM692. $\overline{\text{RESET}}$ will remain low for 50 ms (200 ms for ADM694) after V_{CC} returns to 5 V.

The watchdog timer input (WDI) monitors an I/O line from the µP system. This line must be toggled once every 1.6 seconds to verify correct software execution. Failure to toggle the line indicates that the µP system is not correctly executing its program and may be tied up in an endless loop. If this happens, a reset pulse is generated to initialize the processor.

If the watchdog timer is not needed, the WDI input should be left floating.

The Power Fail Input, PFI, monitors the input power supply via a resistive divider network. The voltage on the PFI input is compared with a precision 1.3 V internal reference. If the input voltage drops below 1.3 V, a power fail output ($\overline{\text{PFO}}$) signal is generated. This warns of an impending power failure and may be used to interrupt the processor so that the system may be shut down in an orderly fashion. The resistors in the sensing network are ratioed to give the desired power fail threshold voltage V_T.

$$V_T = (1.3\ R_1/R_2) + 1.3\ V$$

$$R_1/R_2 = (V_T/1.3) - 1$$

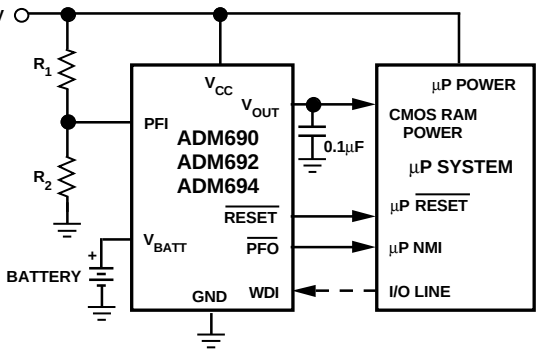


Figure 23a. ADM690/ADM692/ADM694 Typical Application Circuit A

Figure 23b shows a similar application but in this case the PFI input monitors the unregulated input to the 7805 voltage regulator. This gives an earlier warning of an impending power failure. It is useful with processors operating at low speeds or where there are a significant number of housekeeping tasks to be completed before the power is lost.

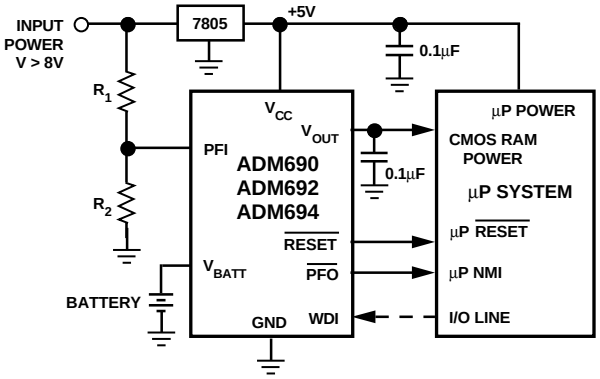


Figure 23b. ADM690/ADM692/ADM694 Typical Application Circuit B

ADM691, ADM693, ADM695

A typical connection for the ADM691/ADM693/ADM695 is shown in Figure 24. CMOS RAM is powered from V_{OUT}. When 5 V power is present this is routed to V_{OUT}. If V_{CC} fails then V_{BATT} is routed to V_{OUT}. V_{OUT} can supply up to 100 mA from V_{CC}, but if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT}, the BATT ON output goes low, providing up to 25 mA of base drive for the external transistor. A 0.1 µF capacitor is connected to V_{OUT} to supply the transient currents for CMOS RAM. When V_{CC} is lower than V_{BATT}, an internal 20 Ω MOSFET connects the backup battery to V_{OUT}.

Downloaded from Arrow.com.

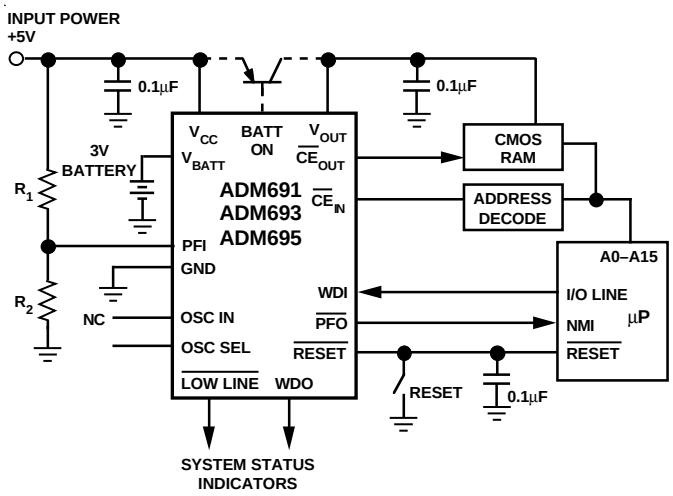


Figure 24. ADM691/ADM693/ADM695 Typical Application

Reset Output

The internal voltage detector monitors V_{CC} and generates a $\overline{\text{RESET}}$ output to hold the microprocessor's Reset line low when V_{CC} is below 4.65 V (4.4 V for ADM693). An internal timer holds $\overline{\text{RESET}}$ low for 50 ms (200 ms for the ADM695) after V_{CC} rises above 4.65 V (4.4 V for ADM693). This prevents repeated toggling of $\overline{\text{RESET}}$ even if the 5 V power drops out and recovers with each power line cycle.

The crystal oscillator normally used to generate the clock for microprocessors can take several milliseconds to stabilize. Since most microprocessors need several clock cycles to reset, $\overline{\text{RESET}}$ must be held low until the microprocessor clock oscillator has started. The power-up $\overline{\text{RESET}}$ pulse lasts 50 ms (200 ms for the ADM695) to allow for this oscillator start-up time. If a different reset pulse width is required, then a capacitor should be connected to OSC IN or an external clock may be used. Please refer to Table I and Figure 4. The manual reset switch and the 0.1 µF capacitor connected to the reset line can be omitted if a manual reset is not needed. An inverted, active high, RESET output is also available.

Power Fail Detector

The +5 V V_{CC} power line is monitored via a resistive potential divider connected to the Power Fail Input (PFI). When the voltage at PFI falls below 1.3 V, the Power Fail Output ($\overline{\text{PFO}}$) drives the processor's NMI input low. If for example a Power Fail threshold of 4.8 V is set with resistors R_1 and R_2, the microprocessor will have the time when V_{CC} falls from 4.8 V to 4.65 V to save data into RAM. An earlier power fail warning can be generated if the unregulated dc input to the 5 V regulator is available for monitoring. This will allow more time for microprocessor housekeeping tasks to be completed before power is lost.

RAM Write Protection

The ADM691/ADM693/ADM695 $\overline{\text{CE}}_{\text{OUT}}$ line drives the Chip Select inputs of the CMOS RAM. $\overline{\text{CE}}_{\text{OUT}}$ follows $\overline{\text{CE}}_{\text{IN}}$ as long as V_{CC} is above the 4.65 V (4.4 V for ADM693) reset threshold.

If V_{CC} falls below the reset threshold, $\overline{\text{CE}}_{\text{OUT}}$ goes high, independent of the logic level at $\overline{\text{CE}}_{\text{IN}}$. This prevents the microprocessor from writing erroneous data into RAM during power-up, power-down, brownouts and momentary power interruptions.

Watchdog Timer

The microprocessor drives the Watchdog Input (WDI) with an I/O line. When OSC IN and OSC SEL are unconnected, the microprocessor must toggle the WDI pin once every 1.6 seconds to verify proper software execution. If a hardware or software failure occurs such that WDI not toggled, the ADM691/ADM693 will issue a 50 ms (200 ms for ADM695) $\overline{\text{RESET}}$ pulse after 1.6 seconds. This typically restarts the microprocessor's power-up routine. A new $\overline{\text{RESET}}$ pulse is issued every 1.6 seconds until WDI is again strobed. If a different watchdog timeout period is required, then a capacitor should be connected to OSC IN or an external clock may be used. Please refer to Table I and Figure 4.

The WATCHDOG OUTPUT ($\overline{\text{WDO}}$) goes low if the watchdog timer is not serviced within its timeout period. Once $\overline{\text{WDO}}$ goes low, it remains low until a transition occurs at WDI. The watchdog timer feature can be disabled by leaving WDI unconnected.

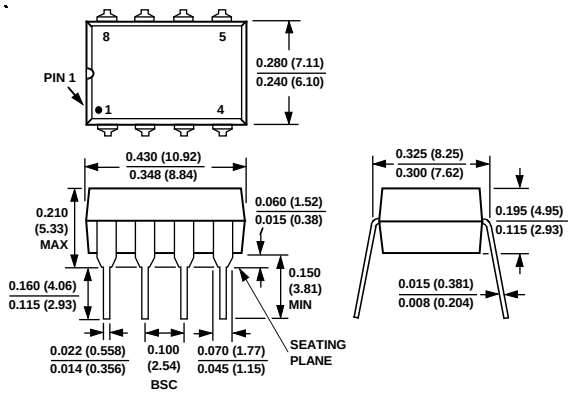
The $\overline{\text{RESET}}$ output has an internal 3 µA pull-up, and can either connect to an open collector reset bus or directly drive a CMOS gate without an external pull-up resistor.

Downloaded from Arrow.com.

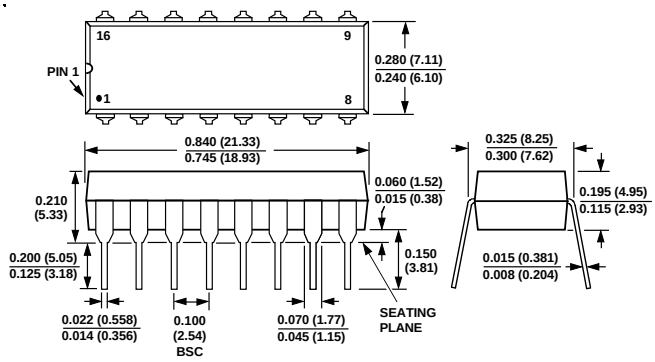
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

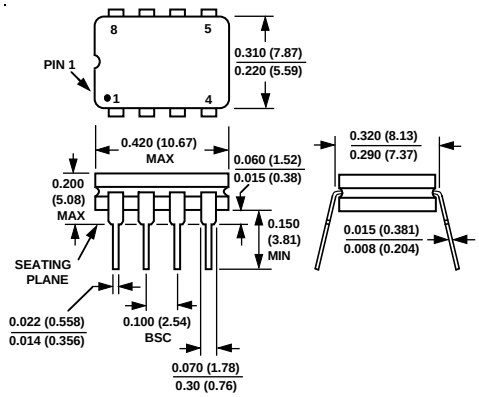
8-Pin Plastic DIP (N-8)



16-Lead Plastic DIP (N-16)

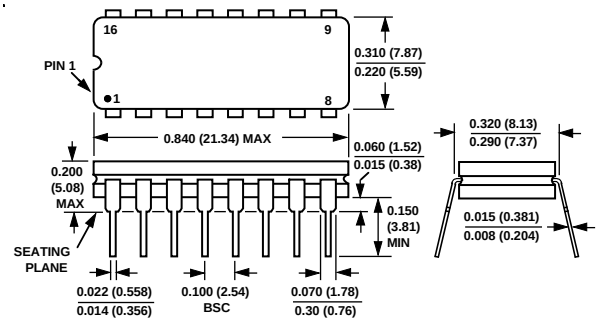


8-Pin Cerdip (Q-8)

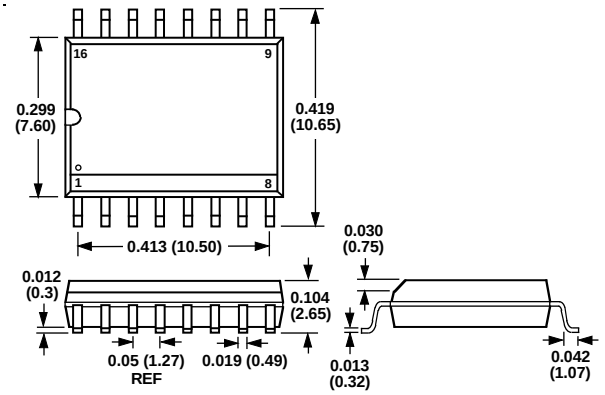


Downloaded from Arrow.com.

16-Lead Cerdip (Q-16)



16-Lead SOIC (R-16)



Downloaded from Arrow.com.

C1782a–2–6/96

PRINTED IN U.S.A.

Downloaded from Arrow.com.