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REVISION HISTORY

3/2019—Rev. B to Rev. C

Added Endnote 2 to Inclinometer, Relative Accuracy Parameter, Table 1; Renumbered Sequentially ... 2
Added X-Ray Sensitivity Section ... 25
Changes to Ordering Guide ... 26

7/2018—Rev. A to Rev. B

Changed Applications Section to Applications Information Section ... 24
Deleted Power-On Reset Operation Section, Figure 33, Second-Level Assembly Section, Figure 34, and Table 24; Renumbered Sequentially ... 25
Added Power Supply Considerations Section, Power-On-Reset Function Section, Transient Current from VDD Ramp Rate Section, and Assembly Section ... 25

1/2010—Rev. 0 to Rev. A

Changes to Figure 25 ... 11
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Updated Outline Dimensions ... 26

8/2006—Revision 0: Initial Version

SPECIFICATIONS

T_A = −40°C to +125°C, VDD = 3.3 V, tilt = 0°, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
INCLINOMETER[1]					
Input Range			360		Degrees
Relative Accuracy[2]	25°C, maximum filter setting		±0.6		Degrees
Sensitivity	25°C		0.025		Degrees/LSB
Accuracy Temperature Coefficient			±0.0167		Degrees/°C
NOISE PERFORMANCE					
Output Noise	At 25°C, no averaging		1.0		Degrees rms
	At 25°C, maximum averaging		0.1		Degrees rms
Noise Density	At 25°C, no averaging		0.037		Degrees/√Hz rms
FREQUENCY RESPONSE					
Sensor Bandwidth			2250		Hz
Sensor Resonant Frequency			5.5		kHz
SELF-TEST STATE					
Output Change When Active	At 25°C		34		Degrees
TEMPERATURE SENSOR					
Output at 25°C			1278		LSB
Scale Factor			−2.13		LSB/°C
ADC INPUT					
Resolution			12		Bits
Integral Nonlinearity			±2		LSB
Differential Nonlinearity			±1		LSB
Offset Error			±4		LSB
Gain Error			±2		LSB
Input Range		0		2.5	V
Input Capacitance	During acquisition		20		pF
ON-CHIP VOLTAGE REFERENCE			2.5		V
Accuracy	At 25°C	−10		+10	mV
Reference Temperature Coefficient			±40		ppm/°C
Output Impedance			70		Ω
DAC OUTPUT	5 kΩ/100 pF to GND				
Resolution			12		Bits
Relative Accuracy	For Code 101 to Code 4095		4		LSB
Differential Nonlinearity			1		LSB
Offset Error			±5		mV
Gain Error			±0.5		%
Output Range			0 to 2.5		V
Output Impedance			2		Ω
Output Settling Time			10		µs
LOGIC INPUTS					
Input High Voltage, V_{INH}		2.0			V
Input Low Voltage, V_{INL}				0.8	V
Logic 1 Input Current, I_{INH}	V_{IH} = VDD		±0.2	±1	µA
Logic 0 Input Current, I_{INL}	V_{IL} = 0 V		−40	−60	µA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 1.6 mA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 1.6 mA			0.4	V

Parameter	Conditions	Min	Typ	Max	Unit
SLEEP TIMER					
Timeout Period[3]		0.5		128	Seconds
FLASH MEMORY					
Endurance[4]		20,000			Cycles
Data Retention[5]	T_J = 85°C	20			Years
CONVERSION RATE					
Minimum Conversion Time			244		µs
Maximum Conversion Time			484		ms
Maximum Throughput Rate			4096		SPS
Minimum Throughput Rate			2.066		SPS
POWER SUPPLY					
Operating Voltage Range VDD		3.0	3.3	3.6	V
Power Supply Current	Normal mode, SMPL_TIME ≥ 0x08 (f_S ≤ 910 Hz) at 25°C		11	14	mA
	Fast mode, SMPL_TIME ≤ 0x07 (f_S ≥ 1024 Hz) at 25°C		36	42	mA
	Sleep mode at 25°C		500	750	µA
Turn-On Time			130		ms

[1] This sensor relies on the earth's gravity to provide accurate incline angle measurements. The axis of rotation must be perpendicular to the earth's gravity to maintain the factory-calibrated accuracy of the sensor.
[2] X-ray exposure may degrade this performance metric.
[3] Guaranteed by design.
[4] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[5] Retention lifetime equivalent at junction temperature (TJ) 55°C as per JEDEC Standard 22 Method A117. Retention lifetime decreases with junction temperature.

TIMING SPECIFICATIONS

T_A = +25°C, VDD = 3.3 V, tilt = 0°, unless otherwise noted.

Table 2.

Parameter	Description	Min[1]	Typ	Max	Unit
f_{SCLK}	Fast mode, SMPL_TIME ≤ 0x07 (f_S ≥ 1024 Hz)	0.01		2.5	MHz
	Normal mode, SMPL_TIME ≥ 0x08 (f_S ≤ 910 Hz)	0.01		1.0	MHz
$t_{DATARATE}$	Chip select period, fast mode, SMPL_TIME ≤ 0x07 (f_S ≥ 1024 Hz)	40			µs
	Chip select period, normal mode, SMPL_TIME ≥ 0x08 (f_S ≤ 910 Hz)	100			µs
t_{CS}	Chip select to clock edge	48.8			ns
t_{DAV}	Data output valid after SCLK falling edge[2]			100	ns
t_{DSU}	Data input setup time before SCLK rising edge	24.4			ns
t_{DHD}	Data input hold time after SCLK rising edge	48.8			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge[3]	5			ns

[1] Guaranteed by design, not production tested.
[2] The MSB presents an exception to this parameter. The MSB clocks out on the falling edge of $\overline{CS}$. The rest of the DOUT bits are clocked after the falling edge of SCLK and are governed by this specification.
[3] This parameter may need to be expanded to allow for proper capture of the LSB. After $\overline{CS}$ goes high, the DOUT line goes into a high impedance state.

TIMING DIAGRAMS

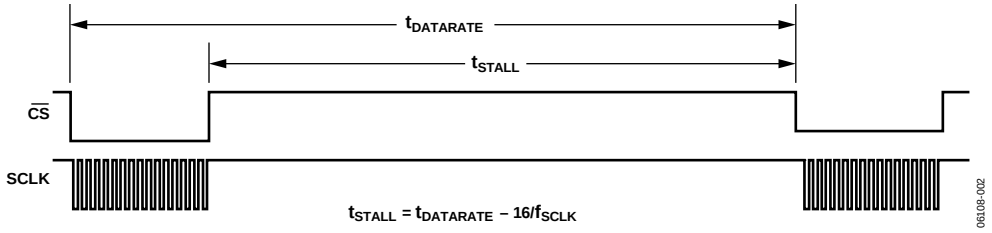

Figure 2. SPI Chip Select Timing

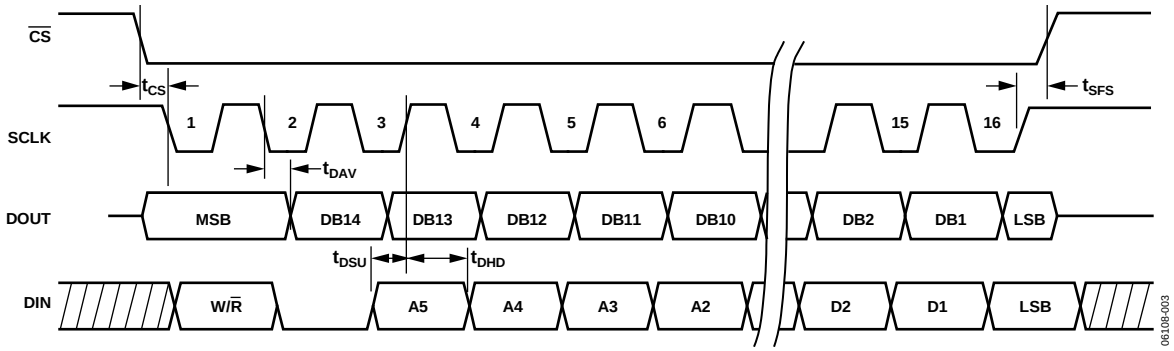

Figure 3. SPI Timing, Utilizing SPI Settings Typically Identified as Phase = 1, Polarity = 1

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration (Any Axis, Unpowered)	3500 *g*
Acceleration (Any Axis, Powered)	3500 *g*
VDD to COM	−0.3 V to +7.0 V
Digital Input/Output Voltage to COM	−0.3 V to +5.5 V
Analog Inputs to COM	−0.3 V to VDD + 0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 4. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
16-Terminal LGA	250°C/W	25°C/W	0.6 g

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

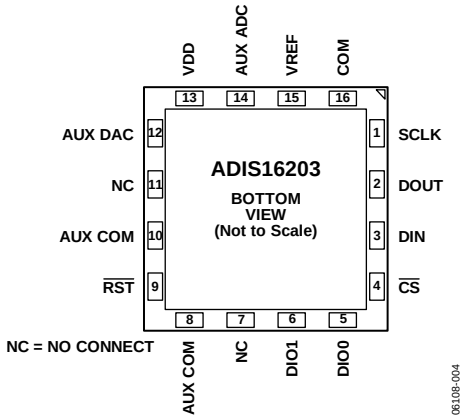

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	SCLK	I	SPI Serial Clock.
2	DOUT	O	SPI Data Out.
3	DIN	I	SPI Data In.
4	$\overline{CS}$	I	SPI Chip Select, Active Low. This input frames the serial data transfer.
5, 6	DIO0, DIO1	I/O	Multifunction Digital I/O Pin.
7, 11	NC	–	No Connect.
8, 10	AUX COM	S	Auxiliary Grounds. Connect to GND for proper operation.
9	$\overline{RST}$	I	Reset, Active Low. This input resets the embedded microcontroller to a known state.
12	AUX DAC	O	Auxiliary DAC Analog Voltage Output.
13	VDD	S	+3.3 V Power Supply.
14	AUX ADC	I	Auxiliary ADC Analog Input Voltage.
15	VREF	O	Precision Reference Output.
16	COM	S	Common. Reference point for all circuitry in the ADIS16203.

[1] S = supply, O = output, I = input.

TYPICAL PERFORMACE CHARACTERISTICS

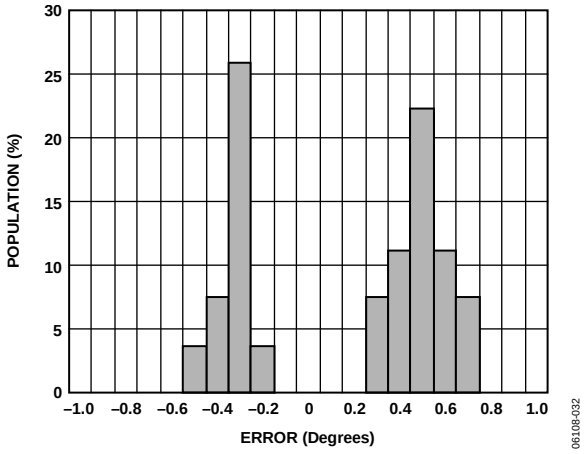

Figure 5. Inclination Error Distribution at 25°C/3.3 V, Incline = 0°

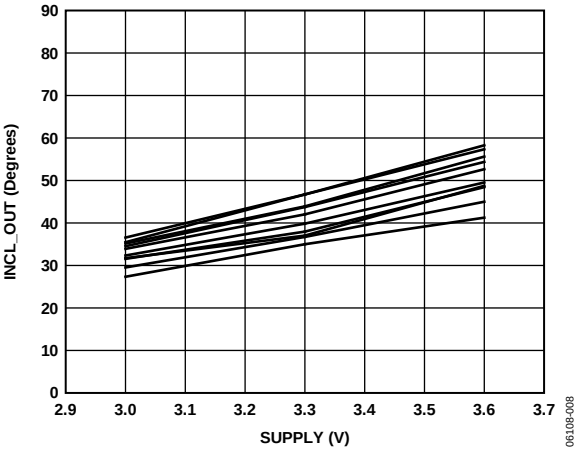

Figure 8. Self-Test Shift vs. Supply at 25°C

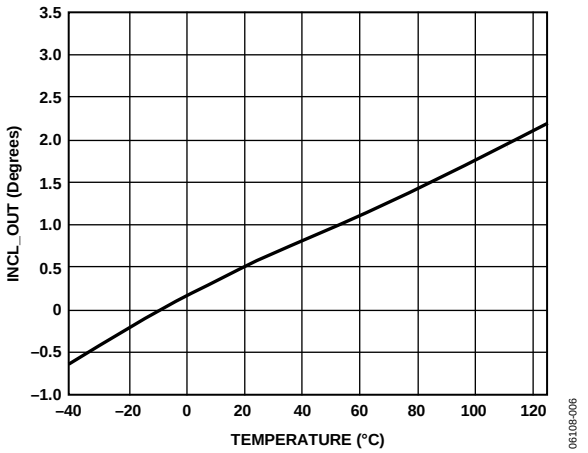

Figure 6. Inclination Error vs. Temperature

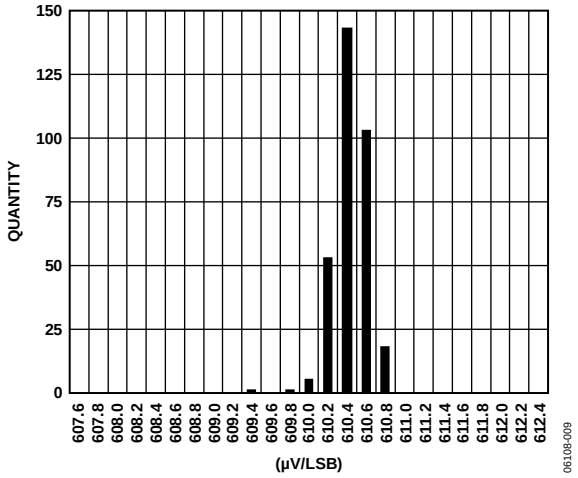

Figure 9. ADC Gain Distribution at 25°C/3.3 V

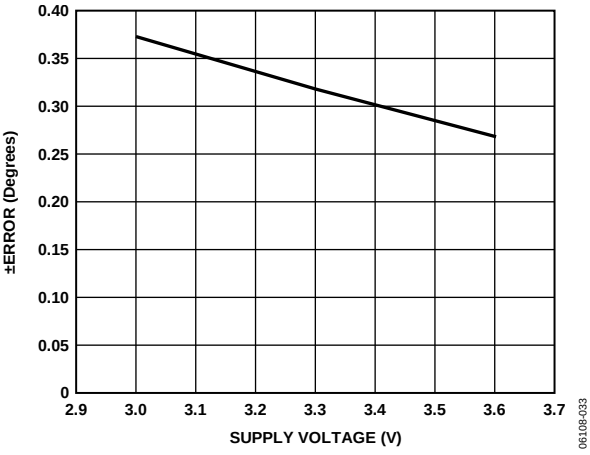

Figure 7. Inclination Error vs. Supply

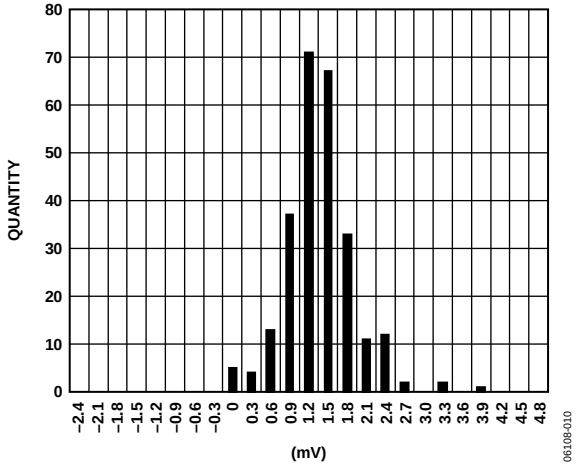

Figure 10. ADC Offset Distribution at 25°C/3.3 V

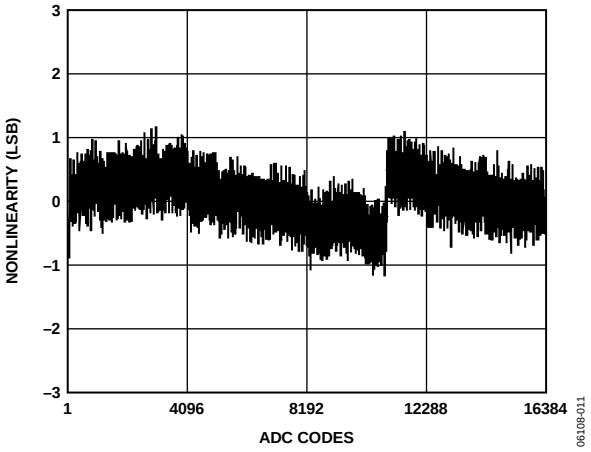

Figure 11. Typical ADC Integral Nonlinearity at 25°C/3.3 V

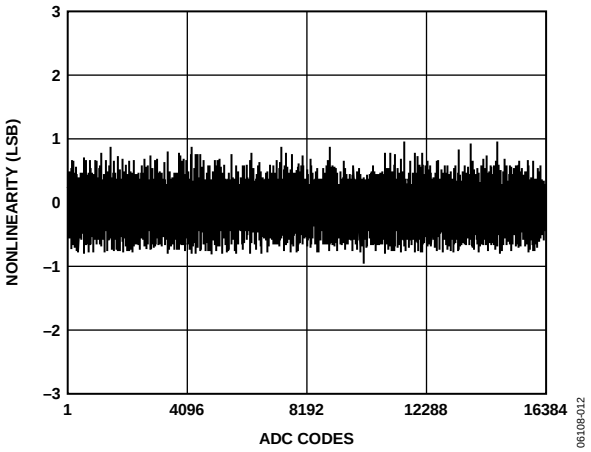

Figure 12. Typical ADC Differential Nonlinearity

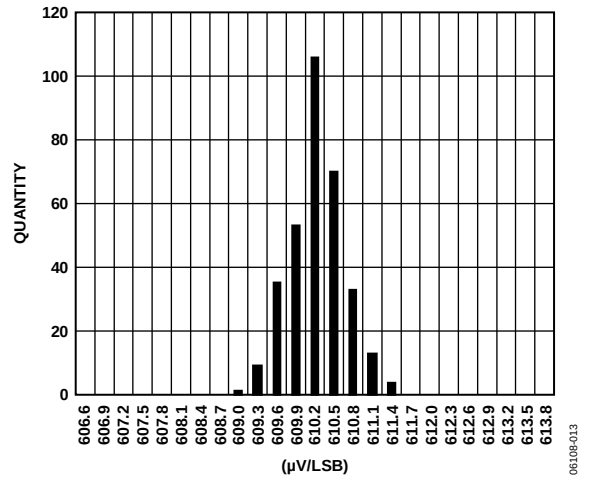

Figure 13. DAC Gain Distribution at 25°C/3.3 V

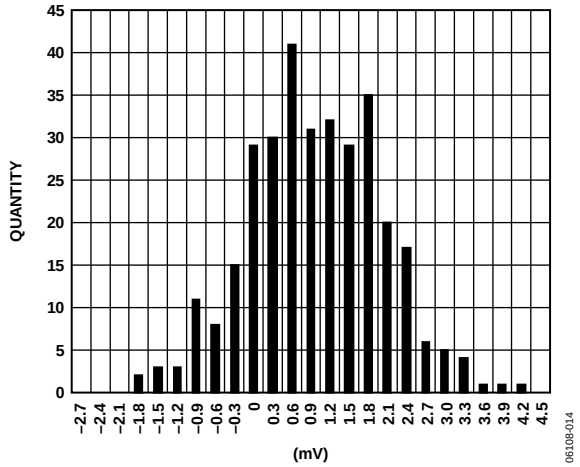

Figure 14. DAC Offset Distribution at 25°C/3.3 V

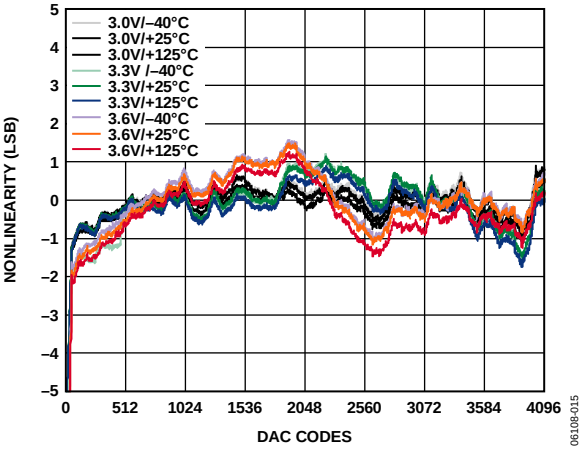

Figure 15. Typical DAC Integral Nonlinearity

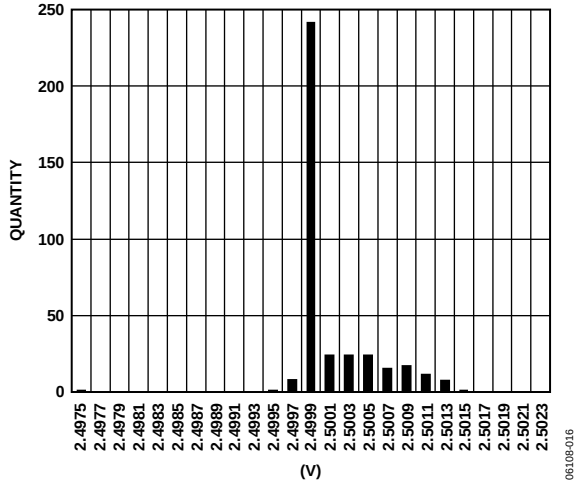

Figure 16. VREF Distribution at 25°C/3.3 V

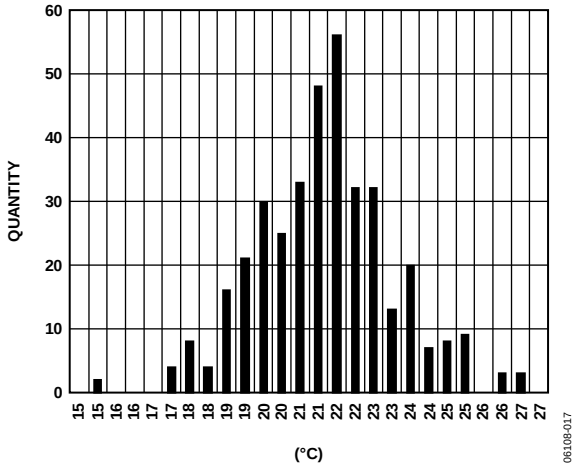

Figure 17. Temperature Distribution at 25°C/3.3 V

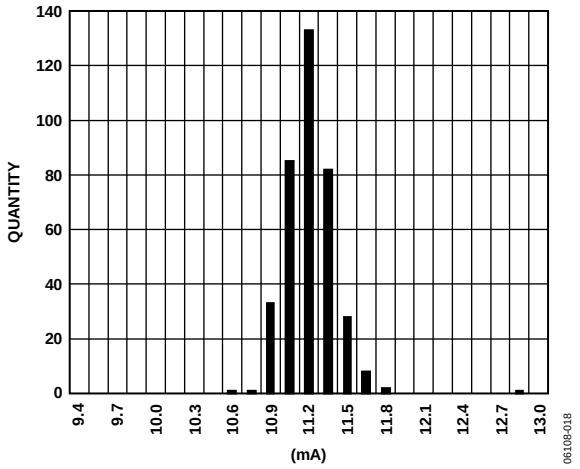

Figure 18. Normal Mode Power Supply Current Distribution at 25°C/3.3 V

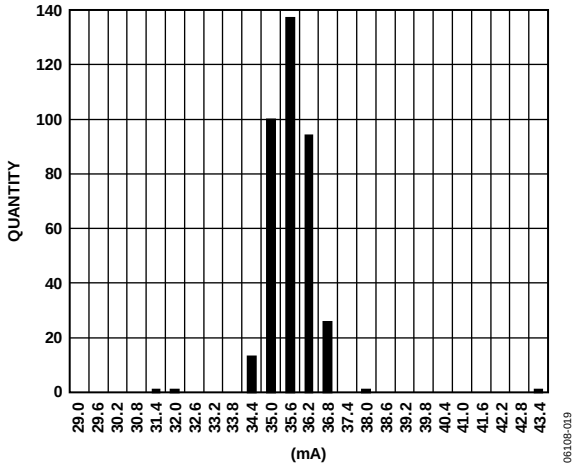

Figure 19. Fast Mode Power Supply Current Distribution at 25°C/3.3 V

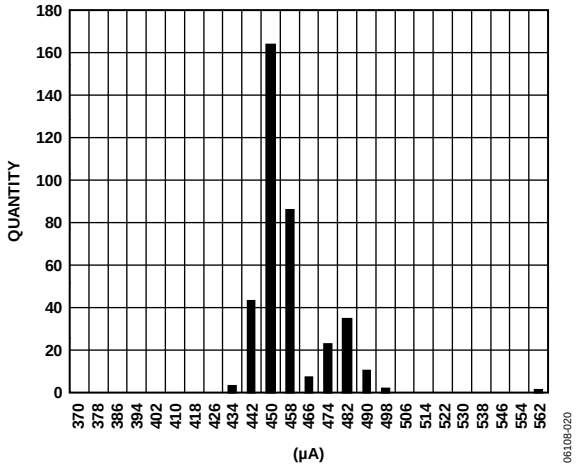

Figure 20. Sleep Mode Power Supply Current Distribution at 25°C/3.3 V

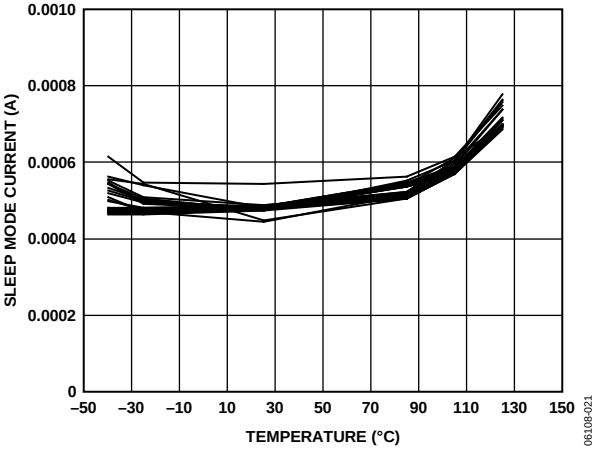

Figure 21. Sleep Mode Current vs. Temperature at 3.3 V

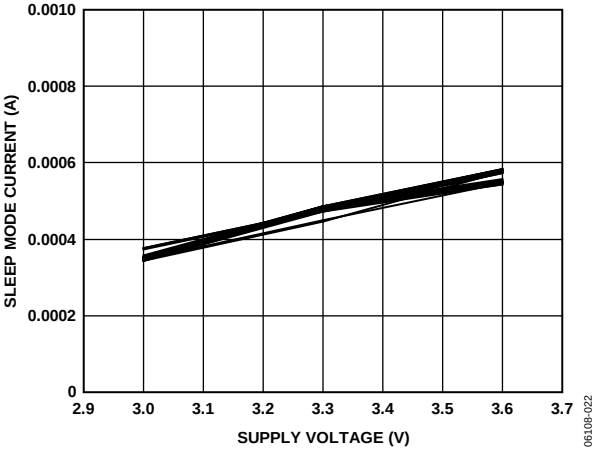

Figure 22. Sleep Mode Current vs. Supply Voltage at 25°C

THEORY OF OPERATION

The ADIS16203 is a calibrated digital inclinometer that provides a full 360° of measurement range in any rotational plane that is parallel to the earth's gravity. A dual-axis accelerometer provides the base-sensing function, which resolves the earth's gravity into two orthogonal vectors, as displayed in Figure 23. A power-efficient approach to a common trigonometric identity converts these orthogonal vectors into an incline-angle measurement.

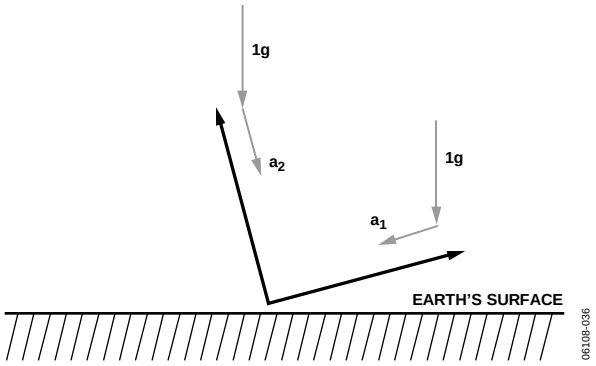

Figure 23. Sensor Measurement Diagram

The digital postprocessing circuit digitizes the sensor outputs and applies sensitivity/offset calibration coefficients prior to angle calculations. A factory calibration produces these coefficients using a full 360° mechanical rotational apparatus. This eliminates the need for system-level calibration in many cases. In addition to calibrating the sensor elements, the ADIS16203 corrects for power-supply-dependent parameters, providing a more robust calibration.

The accuracy of the incline-angle measurements relies on three important factors: the absence of external (aside from gravity) acceleration, managing offset errors introduced during system-level configuration, and maintaining a proper axis of rotation (rotation plane parallel with earth's gravity). All of these factors can influence the acceleration measurements and introduce error. The ADIS16203 provides a simple method for calibrating configuration errors by providing the INCL_NULL register function. See the Calibration section for more details. In addition, a 10° tilt plane error can introduce as much as ±1° of error in the incline-angle outputs.

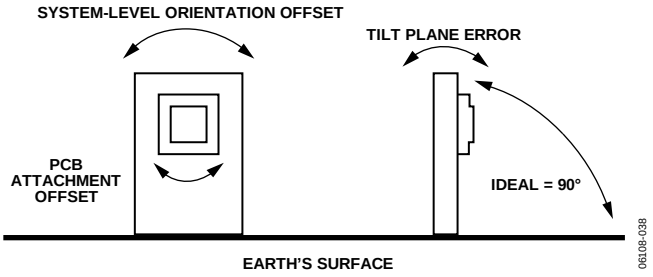

Figure 24. ADIS16203 System-Level Orientation

OUTPUT RESPONSE

The incline-angle measurements are linear with respect to degrees, and the sensor's orientation produces the output response displayed in Figure 25. This figure is helpful in understanding the basic orientation of the inertial sensor measurement axes.

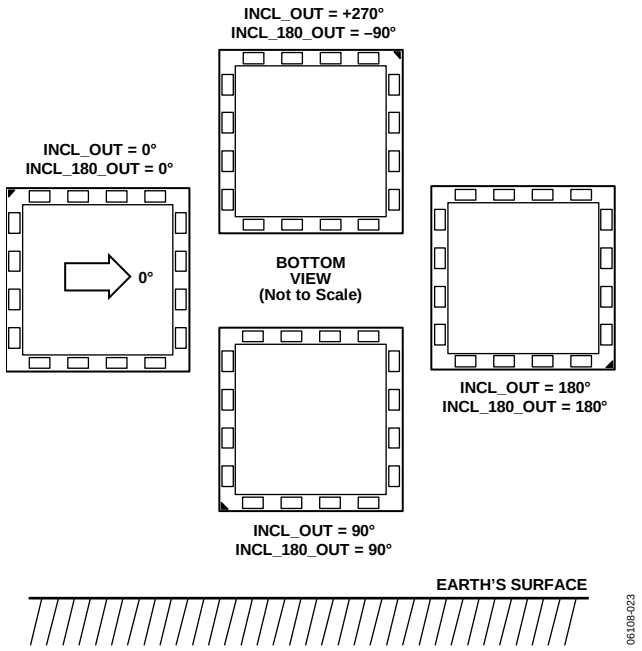

Figure 25. Output Response vs. Orientation

TEMPERATURE SENSOR

An internal temperature sensor monitors the accelerometer's junction temperature. The TEMP_OUT data register provides a digital representation of this measurement. This sensor provides a convenient temperature measurement for system-level characterization and calibration feedback.

BASIC OPERATION

The ADIS16203 is designed for simple integration into industrial system designs, requiring only a 3.3 V power supply and a 4-wire, industry standard SPI. The SPI port facilitates all data transfers with the ADIS16203's registers. Each ADIS16203 function (output data and programming control) has its own register that contains two bytes of data, and each byte of data has its own unique bit map. These two bytes are referred to as *upper* and *lower* bytes, and each has its own 6-bit address.

SERIAL PERIPHERAL INTERFACE (SPI)

The ADIS16203's SPI port provides a common interface that is supported by a wide variety of digital platforms, including MCUs, DSPs, and FPGAs. Even when a dedicated port is not available, the SPI can be implemented using manual bit manipulation, which is more commonly known as *bit banging*. The purpose of this section is to provide a basic description of SPI operation in the ADIS16203. Please refer to Table 2, Figure 2, and Figure 3 for detailed timing and operation of this port.

The ADIS16203's SPI port includes four signals: chip select ($\overline{CS}$), serial clock (SCLK), data input (DIN), and data output (DOUT). The $\overline{CS}$ line enables the ADIS16203's SPI port and, in effect, frames each SPI event. When this signal is high, the DOUT lines are in a high impedance state and the signals on DIN and SCLK have no impact on operation. A complete data frame contains 16 clock cycles. Because the SPI port operates in full duplex mode, it supports simultaneous, 16-bit receive (DIN) and transmit (DOUT) functions during the same data frame.

Figure 26 displays a typical data frame for writing a command to a control register. In this case, the first bit of the DIN sequence is a 1, followed by a 0, then the 6-bit address and 8-bit data command. Because each write command covers a single byte of data, two data frames are required when writing the entire 16-bit space of a register.

Reading the contents of a register requires a modification to the sequence in Figure 26. In this case, the first two bits in the DIN sequence are 0, followed by the address of the register. Each register has two addresses, but either one can be used to access its entire 16 bits of data. The final eight bits of the DIN sequence are irrelevant and can be counted as *don't cares* during a read command. Then, during the next data frame, the DOUT sequence will contain the register's 16-bit data, as shown in Figure 27. Even though a single read command requires two separate data frames, the full duplex mode minimizes this overhead, requiring only one extra data frame when continuously sampling.

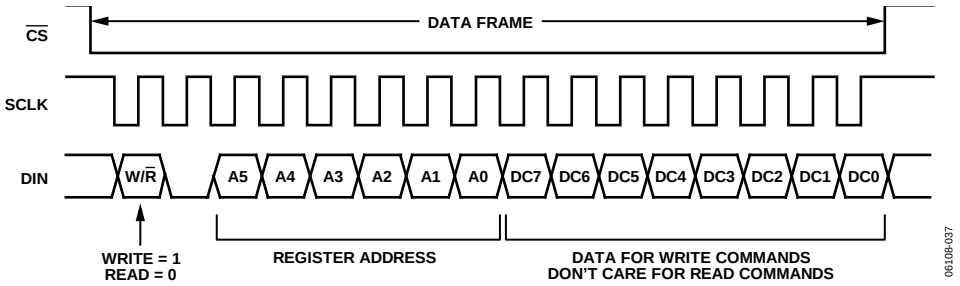

Figure 26. DIN Bit Sequence

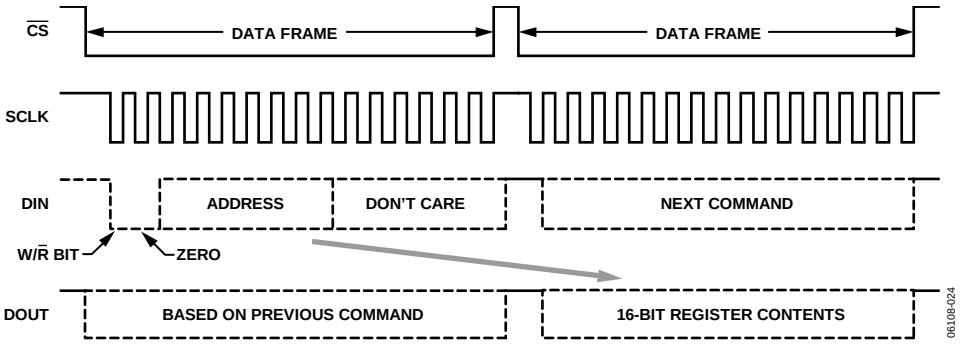

Figure 27. SPI Sequence for Read Commands

DATA OUTPUT REGISTER ACCESS

The ADIS16203 provides access to two calibrated incline-angle measurements (+360° and ±180° output formats), power supply measurements, temperature measurements, and an auxiliary 12-bit ADC channel. This output data is continuously updating internally, regardless of user read rates. The follow bit map describes the structure of all output data registers in the ADIS16203.

MSB **LSB**

ND	EA	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

The MSB holds the new data (ND) indicator. When the output registers are updated with new data, the ND bit goes to a 1 state. After the output data is read, it returns to a 0 state. The EA bit is used to indicate an alarm condition, which could result from a number of conditions, such as a power supply that is out of the specified operating range. See the Alarms section for more details.

The output data is either 12 or 14 bits in length. For all of the 12-bit output data, the D13 and D12 bits are assigned don't care status.

The output data register map is located in Table 6 and provides all of the necessary details for accessing each register's data. Table 7 displays the output coding for the ±180° output data register, INCL_180_OUT, and Figure 28 displays a timing diagram example for reading this register.

Table 6. Data Output Register Information

Name	Function	Address	Resolution (Bits)	Data Format	Scale Factor (per LSB)
SUPPLY_OUT	Power supply data	0x03, 0x02	12	Binary	1.22 mV
AUX_ADC	Auxiliary analog input data	0x09, 0x08	12	Binary	0.61 mV
TEMP_OUT	Sensor temperature data	0x0B, 0x0A	12	Binary	−0.47°C
INCL_OUT	Inclination data	0x0D, 0x0C	14	Binary	0.025°
INCL_180_OUT	±180° inclination data	0x0F, 0x0E	14	Twos complement	0.025°

Table 7. Output Coding Example, INCL_180_OUT[1, 2]

Acceleration Level	Binary Output	Hex Output	Decimal
+170.10°	01 1010 1001 0100	0x1A94	+6804
+93.05°	00 1110 1000 1010	0x0E8A	+3722
+0.625°	00 0000 0001 1001	0x0019	+25
0.00°	00 0000 0000 0000	0x0000	0
−0.625	11 1111 1110 0111	0x3FE7	−25
−93.05°	11 0001 0111 0110	0x3176	−3722
−170.10°	11 1100 0001 1000	0x256C	−6804

[1] Two MSBs have been masked off and are not considered in the coding.
[2] Nominal sensitivity (0.025°/LSB) and zero offset null performance are assumed.

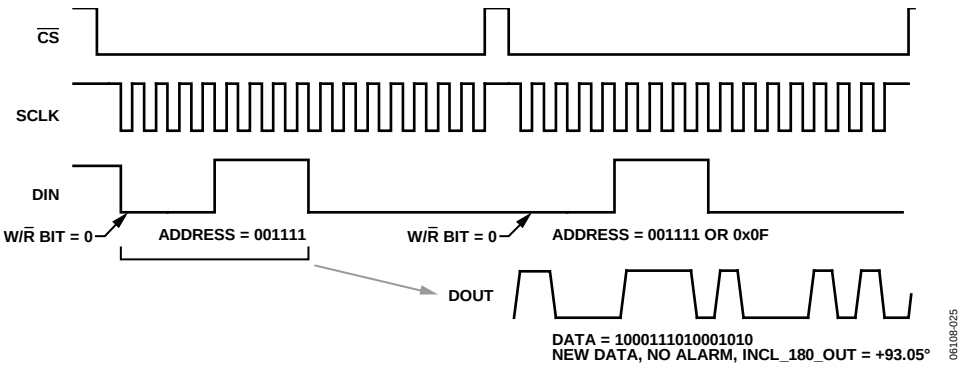

Figure 28. SPI Sequence Reading INCL_OUT When Incline Angle = 93.05°

PROGRAMMING AND CONTROL

CONTROL REGISTER OVERVIEW

The ADIS16203 offers many programmable features that are controlled by writing commands to the appropriate control registers using the SPI. For added system flexibility and programmability, the following sections describe these controls and specify each register's configuration. A list of features that are available for configuration in this register space follows:

- Calibration: Automatic offset null, manual offset adjustment, factory reset
- Rotational direction: clockwise or counter-clockwise
- Sample rate adjustment
- Filter response optimization
- Alarm settings: threshold or rate of change, and comparison with filtered or unfiltered data
- I/O configuration: data ready, etc.
- Power management: sleep mode, normal and high performance modes
- Auxiliary DAC level setting
- Status checks: verify power supply, SPI communication, package orientation
- Flash™ updates to store configuration

CONTROL REGISTER ACCESS

Table 8 displays the control register map for the ADIS16203, including address, volatile status, basic function, and accessibility (read/write). The following sections contain detailed descriptions and configurations for each of these registers.

The ADIS16203 is a Flash-based device with the nonvolatile functional registers implemented as Flash registers. Take note of the endurance limitation of 20,000 writes when considering the system-level integration of these devices. The nonvolatile column in Table 8 indicates the registers that are recovered on power-up. The user must use a manual Flash update command (using the command register) to store the nonvolatile data registers once they are configured properly. When performing a manual Flash update command, the user needs to ensure that the power supply remains within limits for a minimum of 50 ms after the start of the update. This ensures a successful write of the nonvolatile data.

Table 8. Control Register Mapping

Register Name	Type	Nonvolatile	Address	Bytes	Function
			0x00 to 0x01	2	Reserved
INCL_NULL	R/W	X	0x18	2	Incline null calibration
ALM_MAG1	R/W	X	0x20	2	Alarm 1 amplitude threshold
ALM_MAG2	R/W	X	0x22	2	Alarm 2 amplitude threshold
ALM_SMPL1	R/W	X	0x24	2	Alarm 1 sample period
ALM_SMPL2	R/W	X	0x26	2	Alarm 2 sample period
ALM_CTRL	R/W	X	0x28	2	Alarm source control register
			0x2A to 0x2F	6	Reserved
AUX_DAC	R/W		0x30	2	Auxiliary DAC data
GPIO_CTRL	R/W		0x32	2	Auxiliary digital I/O control register
MSC_CTRL	R/W	X	0x34	2	Miscellaneous control register
SMPL_TIME	R/W	X	0x36	2	ADC sample period control
AVG_CNT	R/W	X	0x38	2	Defines number of samples used by moving average filter
SLP_CNT	R/W		0x3A	2	Counter used to determine length of power-down mode
STATUS	R		0x3C	2	System status register
COMMAND	W		0x3E	2	System command register

CONTROL REGISTER DETAILS

All ADIS16203 control registers are organized into 2-byte segments, and both upper (Bit 8 to Bit 15) and lower (Bit 0 to Bit 7) bytes have unique addresses and can be accessed individually.

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

This section provides a description of each register, including its purpose, relevant scaling information, bit maps, addresses, and default values.

CALIBRATION

In addition to the factory calibration, the ADIS16203 provides two user calibration options. Both options utilize the INCL_NULL control register, which provides an *add* function to the two incline-angle output registers: INCL_OUT and INCL_180_OUT. Because the default contents of INCL_NULL are 0, adding it to these two outputs has no effect on the output data.

The first calibration option is an automatic null function. This function measures the contents of INCL_OUT and then writes the inverse of this value into the INCL_NULL control register. The accuracy of this calibration is dependent on the stability of the INCL_OUT measurement; therefore, maximizing the filtering will minimize the errors associated with noise. Table 9 displays a sequence that executes the automatic null.

Table 9. Automatic Null Sequence

Step	Description
Write 0x08 to Address 0x38	Sets averaging count to 256 using the AVG_CNT register
Wait for 512 samples	Waits for the lowest noise data
Write 0x01 to Address 0x3E	Executes the global autonull function using the COMMAND register
Restore previous average count	

Increasing the sample rate using the SMPL_TIME control register will minimize the waiting time if this parameter is critical.

The second option for system-level calibration is manual adjustment. The INCL_NULL control register can be updated using write commands. Refer to its definition in the INCL_NULL Register Definition section for details.

The factory calibration can be restored by writing 0x02 to Register Address 0x3E. This restores INCL_NULL to 0.

CALIBRATION REGISTER DEFINITION

INCL_NULL Register Definition

Address	Scale[1]	Default	Format	Access
0x19, 0x18	0.025°	0x0000	Binary	R/W

[1] Scale is the weight of each LSB.

The INCL_NULL register is the user controlled register for calibrating system-level inclination offset errors. The maximum calibration range is +0° to +359.975° or 0 to +14,399 decimal codes. The contents of this register are nonvolatile.

Table 10. INCL_NULL Bit Designations

Bit	Description
15:14	Not necessary, force to 0
13:0	Data bits

ALARMS

The ADIS16203 contains two independent alarm functions that are referred to as Alarm 1 and Alarm 2. The Alarm 1 function is managed by the ALM_MAG1 and ALM_SMPL1 control registers. The Alarm 2 function is managed by the ALM_MAG2 and ALM_SMPL2 control registers. Both the Alarm 1 and Alarm 2 functions share the ALM_CTRL register. For simplicity, this section refers to the Alarm 1 functionality only.

The 16-bit ALM_CTRL register serves several roles in controlling the Alarm 1 function. First, it is used to enable the overall Alarm 1 function and to select the output data variable that is to be monitored for the alarm condition. Second, it is used to select whether the Alarm 1 function is based upon a predefined threshold (THR) level or a predefined rate-of-change (ROC) slope. Third, the ALM_CTRL register can be used in setting up one of the two general-purpose input/output lines (GPIOs) to serve as a hardware output that indicates when an alarm condition has occurred. Enabling the I/O alarm function as well as setting its polarity and controlling its operation are accomplished using this register. Fourth, this register provides the controls for setting the comparison data as filtered or unfiltered.

Note that when enabled, the hardware output indicator serves both the Alarm 1 and Alarm 2 functions and cannot be used to differentiate between one alarm condition and the other. It is simply used to indicate that an alarm is active and that the user should poll the device via the SPI to determine the source of the alarm condition (see the STATUS Register Definition section).

Because the ALM_CTRL, MSC_CTRL, and GPIO_CTRL control registers can influence the same GPIO pins, a priority level has been established to avoid conflicting assignments of the two GPIO pins. This priority level is defined as MSC_CTRL, which has precedence over ALM_CTRL, which has precedence over GPIO_CTRL.

The ALM_MAG1 control register used in controlling the Alarm 1 function has two roles. The first role is to store the value with which the output data variable is compared against to discern if an alarm condition exists. The second role is to identify whether the alarm should be active for excursions above or below the alarm limit. If 1 is written to Bit 15 of the ALM_MAG1 control register, the alarm is active for excursions extending above a given limit. If 0 is written to Bit 15, the alarm is active for excursions dropping below the given limit. The comparison value contained within the ALM_MAG1 control register is located within the lower 14 bits.

The monitored output register establishes the format of the 14-bit data space in the ALM_MAG1 and ALM_MAG2 registers. For example, setting the alarm to monitor INCL_OUT sets the data format to a 14-bit, twos complement number, which carries a bit weight of 0.025°.

Use caution when monitoring the temperature output register for the alarm conditions. Here, the negative temperature scale factor results in the greater than and less than selections requiring reverse logic.

Setting Bit 11 in the ALM_CTRL register establishes the mode of operation: threshold or rate of change (ROC). When the ROC function is enabled, the comparison of the output data variable is against the ALM_MAG1 level averaged over the number of samples as identified in the ALM_SMPL1 control register. This acts to create a comparison of (Δ units/Δ time) or the derivative of the output data variable against a predefined slope.

The versatility built into the alarm function allows the user to adapt to several applications. For example, in the case of monitoring twos complement variables, Bit 15 within the ALM_MAG1 control register can allow for the detection of negative excursions below a fixed level. In addition, the Alarm 1 and Alarm 2 functions can be set to monitor the same variable that allows the user to discern if an output variable remains within a predefined window.

Another potential ROC application is to monitor slowly changing outputs in the inclination level. With the addition of the alarm hardware functionality, the ADIS16203 can be left to run independently of the main processor and interrupt the system only when an alarm condition occurs. Conversely, the alarm condition can be monitored through the routine polling of any one of the seven data output registers.

Bits 4 and 5 in the ALM_CTRL register establishes whether ALM_MAG1 and ALM_MAG2 are compared with filtered or unfiltered data.

ALM_MAG1 Register Definition

Address	Default[1]	Format[2]	Access
0x21, 0x20	0x0000	N/A	R/W

[1] Default is valid only until the first register write cycle.
[2] Format is established by source of monitored data

The ALM_MAG1 register contains the threshold level for Alarm 1. The contents of this register are nonvolatile.

Table 11. ALM_MAG1 Bit Designations

Bit	Description
15	Greater than Active Alarm Bit. 1: Alarm is active for an output greater than ALM_MAG1 register setting. 0: Alarm is active for an output less than ALM_MAG1 register setting.
14	Not used.
13:0	Data Bits. This number can be either twos complement or straight binary. The format is set by the value being monitored by this function.

ALM_SMPL1 Register Definition

Address	Default[1]	Format	Access
0x25, 0x24	0x0000	Binary	R/W

[1] Default is valid only until the first register write cycle.

The ALM_SMPL1 register contains the sample period information for Alarm 1, when it is set for ROC alarm monitoring. The ROC alarm function averages the change in the output variable over the specified number of samples and compares this change directly to the values specified in the ALM_MAG1 register. The contents of this register are nonvolatile.

Table 12. ALM_SMPL1 Bit Designations

Bit	Description
15:8	Not used
7:0	Data bits

ALM_MAG2 Register Definition

Address	Default[1]	Format[2]	Access
0x23, 0x22	0x0000	N/A	R/W

[1] Default is valid only until the first register write cycle.
[2] Format is established by source of monitored data.

The ALM_MAG2 register contains the threshold level for Alarm 2. The contents of this register are nonvolatile.

Table 13. ALM_MAG2 Bit Designations

Bit	Description
15	Greater than Active Alarm Bit. 1: Alarm is active for an output greater than ALM_MAG2 register setting. 0: Alarm is active for an output less than ALM_MAG2 register setting.
14	Not used.
13:0	Data Bits. This number can be either twos complement or straight binary. The format is set by the value being monitored by this function.

ALM_SMPL2 Register Definition

Address	Default[1]	Format	Access
0x27, 0x26	0x0000	Binary	R/W

[1] Default is valid only until the first register write cycle.

The ALM_SMPL2 register contains the sample period information for Alarm 2, when it is set for ROC alarm monitoring. The ROC alarm function averages the change in the output variable over the specified number of samples and compares this change directly to the values specified in the ALM_MAG2 register. The contents of this register are nonvolatile.

Table 14. ALM_SMPL2 Bit Designations

Bit	Description
15:8	Not used
7:0	Data bits

ALM_CTRL Register Definition

Address	Default[1]	Format	Access
0x29, 0x28	0x0000	N/A	R/W

[1] Default is valid only until the first register write cycle.

The ALM_CTRL register contains the alarm control variables.

Table 15. ALM_CTRL Bit Designations

Bit	Value	Description
15		Rate of Change (ROC) Enable for Alarm 2 1: ROC is active 0: ROC is inactive
14:12		Alarm 2 Source Selection
	000	Alarm disable
	001	Alarm source: power supply output
	010	Not used
	011	Not used
	100	Alarm source: auxiliary ADC output
	101	Alarm source: temperature sensor output
	110	Alarm source: INCL_OUT output
	111	Alarm source: INCL_180_OUT output
11		Rate of Change (ROC) Enable for Alarm 1 1: ROC is active 0: ROC is inactive
10:8		Alarm 1 Source Selection
	000	Alarm disable
	001	Alarm source: power supply output
	010	Not used
	011	Not used
	100	Alarm source: auxiliary ADC output
	101	Alarm source: temperature sensor output
	110	Alarm source: INCL_OUT output
	111	Alarm source: INCL_180_OUT output
7:6		Not used
5		ADF2—Alarm Data Filter 1: Use filtered data for comparison 0: Use instantaneous data for comparison
4		ADF1—Alarm Data Filter 1: Use filtered data for comparison 0: Use instantaneous data for comparison
3		Not used
2		Alarm Output Enable 1: Alarm output enabled 0: Alarm output disabled
1		Alarm Output Polarity 1: Active high 0: Active low
0		Alarm Output Line Select 1: DIO1 0: DIO0

SAMPLE PERIOD CONTROL

The output data variables within the ADIS16203 are sampled and updated at a rate based upon the SMPL_TIME control register. The sample period can be precisely controlled over more than a three-decade range using a time base with two settings and a 7-bit binary count. The use of a time base that varies with a ratio of 1:31 allows for a more optimum resolution in the sample period than a straight binary counter. This is reflected in Figure 29, where the frequency is presented on a logarithmic scale.

Note that the sample period given is defined as the cumulative time required to sample, process, and update all data output variables. The data output variables are sampled as a group and in unison with one another. Whatever update rate is selected for one signal, all output data variables are updated at the same rate whether they are monitored via the SPI or not.

For a sample period setting of less than 1098.9 µs (SMPL_TIME ≤ 0x07), the overall power dissipation in the part rises by approximately 300%.

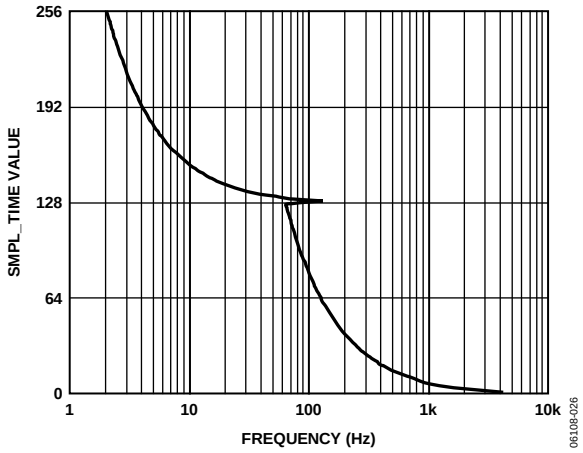

Figure 29. SMPL_TIME Values vs. Sample Frequency

SMPL_TIME Register Definition

Address	Default[1]	Format	Access
0x37, 0x36	0x0008	N/A	R/W

[1] Default is valid only until the first register write cycle.

The data within this register is nonvolatile, allowing for data recovery upon reset.

Table 16. SMPL_TIME Bit Descriptions

Bit	Description
15:8	Not used.
7	ADC Time Base Control. The MSB and TMBS set the time base of the acquisition system to 122.1 µs when SR7 = 0 vs. 3.784 ms when SR7 = 1.
6:0	ADC Sample Period Count. The lower seven bits, SP6 to SP0, represent a binary count that results in the combined sample period of the ADC when added to one and then multiplied by the time base. (The combined sample period is the period required to sample and update all seven data outputs.) The minimum setting for the lower seven bits, SP6 to SP0, is 0x01. The overall acquisition time can be varied from 244.2 µs to 15.51 ms in 122.1 µs increments for TMBS = 0 and from 7.57 ms to 481 ms in 3.784 ms increments for TMBS = 1. This equates to the sample rate varying from 4096 SPS to 64.5 SPS for TMBS = 0 and from 132 SPS to 2.08 SPS for TMBS = 1.

FILTERING CONTROL

The ADIS16203 uses two types of filters for the output data. The INCL_OUT and INCL_180_OUT data outputs use a Bartlett Window function, and the SUPPLY_OUT, AUX_ADC, and TEMP_OUT data outputs use a standard moving-averaging filter. The number of taps set by the AVG_CNT control register establishes the frequency response. The number of taps can be derived from the contents of AVG_CNT using the following equation:

$$N = 2^{AVG\_CNT}$$

The following equations characterize the expected behavior of each filtering approach. Figure 30 and Figure 31 shows the frequency responses of each filter approach.

Averaging:

$$H_A(f) = \frac{\sin(\pi \times N \times f \times t_s)}{N \times \sin(\pi \times f \times t_s)}$$

Bartlett Window:

$$H_B(f) = H_A^2(f)$$

The primary difference in the frequency responses offered by each approach lies in their side lobes, which are 13 dB better in the Bartlett Windowing approach. The Bartlett Window filtering has two times the latency of the moving average filter.

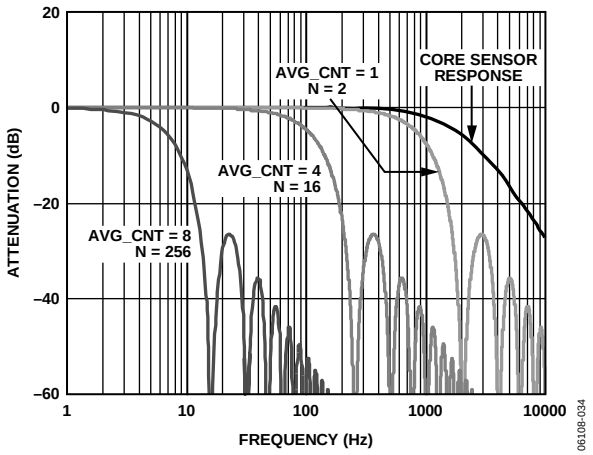

Figure 30. INCL_OUT, INCL_180_OUT Filter Response

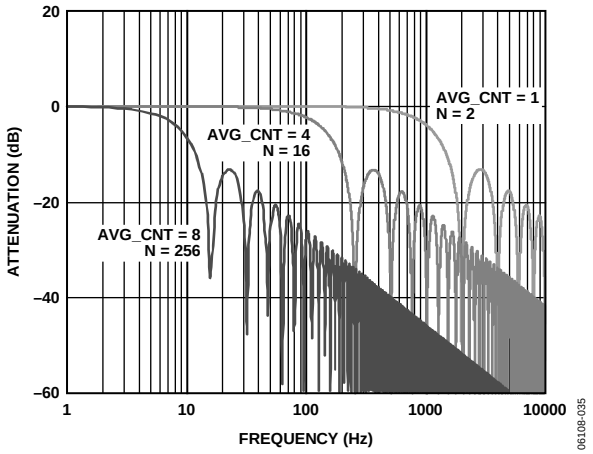

Figure 31. SUPPLY_OUT, AUX_ADC, and TEMP_OUT Filter Response, f_S = 4096 SPS

AVG_CNT Register Definition

Address	Default[1]	Format	Access
0x39, 0x38	0x0007	Binary	R/W

[1] Default is valid only until the first register write cycle.

The AVG_CNT register contains information that represents the number of averages to be applied to the output data. The number of averages can be calculated by powers of 2. The number of averages can be set to 1, 2, 4, 8, 16, 32, 64, 128, or 256.

Table 17. AVG_CNT Bit Description

Bit	Description
15:4	Not used
3:0	Data bits (maximum = 1000, or a decimal value of 8)

POWER-DOWN CONTROL

The ADIS16203 has the ability to power down for user-defined amounts of time, using the SLP_CNT control register. The amount of time specified by the SLP_CNT control register is equal to the binary count of the 8-bit control word multiplied by 0.5 sec. Therefore, the 255 codes cover an overall shutdown period of 127.5 seconds. The SLP_CNT register is volatile and is set to 0 upon both power-up and subsequent wake-ups from the power-down period. By setting the SLP_CNT control register to a nonzero state, the ADIS16203 automatically powers down once the next sample period is completed and the data output registers are updated.

Once the ADIS16203 is placed into power-down mode, it can only return to normal operation by timing out, by a reset command (using the $\overline{\text{RST}}$ hardware control line), or by cycling the power applied to the part. Once awake, the data output registers can be scanned to determine what the state of the output registers were prior to powering down. Once the data is recovered, the device can be powered down again by simply writing a nonzero value to the SLP_CNT control register and starting the process over.

Once the power-down time is complete, the recovery time for the ADIS16203 is approximately 2 ms. This recovery time is implemented within the device to allow for recovery of the ADC prior to performing the next data conversion. Note that the ND data bit within the data output control registers is cleared when the ADIS16203 is powered down. Likewise, the new data hardware I/O line is placed into an inactive state prior to being powered down. The DAC is placed into a power-down mode as well, resulting in the DAC output dropping to 0 V during the power-down period. All control register settings are retained while powered down with the exception of the SLP_CNT control register.

SLP_CNT Register Definition

Address	Default[1]	Format	Access
0x3B, 0x3A	0x0000	Binary	R/W

[1] Default is valid only until the first register write cycle.

Table 18. SLP_CNT Bit Descriptions

Bit	Description
15:8	Not used
7:0	Data bits

STATUS FEEDBACK

The status control register within the ADIS16203 is utilized in determining the present state of the device. The ability to monitor the device becomes necessary when and if the ADIS16203 has registered an alarm and/or error condition as indicated by the alarm enable (Bit 14) within the output data registers.

STATUS Register Definition

Address	Default[1]	Format	Access
0x3D, 0x3C	0x0000	N/A	Read only

[1] Default is valid only until the first register write cycle.

The STATUS control register contains the alarm/error flags that indicate abnormal operating conditions. See Table 19 for the definition of each bit. Bit 0 and Bit 1 will automatically clear when the power supply is in the specified range of operation. Setting Bit 4 in the COMMAND register clears all flags. The flags are set on a continuing basis as long as the error or alarm conditions persist.

Table 19. STATUS Bit Descriptions

Bit	Description
15:10	Not used
9	Alarm 2 Status 1: Active 0: Normal mode
8	Alarm 1 status 1: Active 0: Normal mode
7:6	Not used
5	Self Test Fail 1: Self-test failure 0: Self-test pass
3	SPI Communications Failure 1: Error condition 0: Normal mode
2	Control Register Update Failed 1: Error condition 0: Normal mode.
1	Power Supply Above 3.625 V 1: Error condition 0: Normal mode
0	Power Supply Below 2.975 V 1: Error condition 0: Normal mode

COMMAND CONTROL

The COMMAND control register is utilized in sending global commands to the ADIS16203 device. Any one of the global commands can be implemented by simply writing 1 to its corresponding bit location. The command control register has write-only capability and is volatile. Table 20 describes each of these global commands.

COMMAND Register Definition

Address	Default[1]	Format	Access
0x3F, 0x3E	0x0000	N/A	Write only

[1] Default is valid only until the first register write cycle.

Table 20. COMMAND Bit Descriptions

Bit	Description
15:8	Not used.
7	Software Reset Command.
6:5	Not used.
4	Clear Status Register, once per activation
3	Manual Flash Update Command. This command is utilized in updating all of the nonvolatile registers to Flash. Once the command is initiated, the supply voltage, VDD, must remain within specified limits for 50 ms to ensure proper update of the nonvolatile registers to Flash.
2	Auxiliary DAC Latch Command. This command acts to latch the AUX_DAC control register data into the auxiliary DAC upon receipt of the command. This allows for sequential loading of the upper and lower AUX_DAC data bytes via the SPI without having the auxiliary DAC transition into unwanted, intermediate states based upon the individual AUX_DAC data bytes. Once the two bytes of AUX_DAC are loaded, the DAC latch command is initiated to move the data into the auxiliary DAC itself.
1	Factory Reset Command. This command allows the user to reset the INCL_NULL register to its nominal setting (0x0000) upon receipt of the command. Data within the moving average filters is reset. As the manual Flash command (COMMAND register, Bit 3), this command stores all of the nonvolatile registers to Flash. Once the command is initiated, the supply voltage, VDD, must remain within specified limits for 50 ms to ensure proper update of the nonvolatile registers to Flash.
0	Null Command. This command loads the inclination offset register with a value that zeros out the inclination and outputs. Useful as a single command to simultaneously zero the inclination outputs. As the manual Flash command (COMMAND register, Bit 3), this command stores all of the nonvolatile registers to Flash. Once the command is initiated, the supply voltage, VDD, must remain within specified limits for 50 ms to ensure proper update of the nonvolatile registers to Flash.

MISCELLANEOUS CONTROL REGISTER

The MSC_CTRL control register governs the operation of several miscellaneous features: using the general purpose I/O for data-ready (DR) hardware I/O function, reversing the polarity of rotation (clockwise vs. counter clockwise), and self-test. The control bits for each of these functions are described in Table 21.

The operation of the data-ready hardware I/O function is very similar to the alarm hardware I/O function (controlled through the ALM_CTRL control register). In this case, the MSC_CTRL register can be used in setting up one of the GPIO pins to serve as the hardware output pin that indicates when the sampling, conversion, and processing of the data output variables have been completed. This register provides the ability to enable the data-ready hardware function and establish its polarity.

The data-ready hardware I/O pin is reset automatically to an inactive state part way through the next conversion cycle, resulting in a pulse train with a duty cycle varying from ~15% to 35%, depending upon the sample period setting. Upon completion of the next data processing cycle, the data ready hardware I/O line is set to 1.

The MSC_CTRL, ALM_CTRL, and GPIO_CTRL control registers can influence the same GPIO pins. A priority level has been established to avoid conflicting assignments of the two GPIO pins. This priority level is defined as MSC_CTRL and has precedence over ALM_CTRL, which has precedence over GPIO_CTRL.

The self-test operation exercises the base accelerometer's mechanical structure and establishes a mechanical diagnostic test. The self-test offers the ability to have the ADIS16203 run an internal diagnostic test, which returns a pass/fail condition (see the STATUS register definition of Bit 5 in Table 19). This feature also provides the ability to observe the incline angle outputs during the self-test function, which is nominally 37°, regardless of the incline angle of the device. Note that a self-test changes the contents of SMPL_TIME to improve the speed of this test. Upon completion, the ADIS16203 restores the original contents to SMPL_TIME.

MSC_CTRL Register Definition

Address	Default[1]	Format	Access
0x35, 0x34	0x0000	N/A	R/W

[1] Default is valid only until the first register write cycle.

The 16-bit miscellaneous control register is used in the controlling of the self-test and data-ready hardware functions. This includes turning on and off the self-test function, as well as configuring the data-ready function. For the data-ready function, the written values are nonvolatile, allowing for data recovery upon reset. The self-test data is volatile and is set to 0s upon reset. This register has read/write capability.

Table 21. MSC_CTRL Bit Descriptions

Bit	Description
15:11	Not used
10	No Self-Test on Power-Up 1: No self-test on power-up or reset 0: Self-test on power-up enabled (typically requires approximately 13 ms in high performance mode and approximately 35 ms in low power mode with every power-up or reset)
9	Reverse Rotation 1: Reverses rotation of both inclination outputs 0: Normal operation
8	Self-Test Enable 1: ST enabled (continuous self-test) 0: ST disabled
7:3	Not used
2	Data-Ready Enable 1: DR enabled 0: DR disabled
1	Data-Ready Polarity 1: Active high 0: Active low
0	Data-Ready Line Select 1: DIO1 0: DIO0

PERIPHERALS

AUXILIARY ADC FUNCTION

The auxiliary ADC function integrates a standard 12-bit ADC into the ADIS16203 to digitize other system-level analog signals. The output of the ADC can be monitored through the AUX_ADC control register, as defined in Table 6. The ADC consists of a 12-bit successive approximation converter. The output data is presented in straight binary format with the full-scale range extending from 0 V to VREF. A high precision, low drift, factory-calibrated 2.5 V reference is also provided.

Figure 32 shows the equivalent circuit of the analog input structure of the ADC. The input capacitor, C1, is typically 4 pF and can be attributed to parasitic package capacitance. The two diodes provide ESD protection for the analog input. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. This would cause these diodes to become forward-biased and to start conducting. These diodes can handle 10 mA without causing irreversible damage to the part. The resistor is a lumped component that represents the on resistance of the switches. The value of this resistance is typically 100 Ω. Capacitor C2 represents the ADC sampling capacitor and is typically 16 pF.

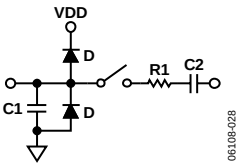

Figure 32. Equivalent Analog Input Circuit
Conversion Phase: Switch Open
Track Phase: Switch Closed

For ac applications, removing high frequency components from the analog input signal is recommended by using an RC low-pass filter on the relevant analog input pins.

In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This can necessitate the use of an input buffer amplifier. When no input amplifier is used to drive the analog input, the source impedance should be limited to values less than 1 kΩ. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated.

AUXILIARY DAC FUNCTION

The auxiliary DAC function integrates a standard 12-bit DAC into the ADIS16203. The DAC output is buffered and fed off-chip to allow for the control of miscellaneous system-level functions. Data downloads through the writing of two adjacent data bytes as defined in its register definition. To prevent the DAC from transitioning through inadvertent states during data downloads, a single command is used to simultaneously latch both data bytes into the DAC after they have been written into the AUX_DAC control register. This command is implemented by writing 1 to Bit 2 of the command control register and, once received, results in the DAC output transitioning to the desired state.

The DAC output provides an output range of 0 V to 2.5 V. The DAC output buffer features a true rail-to-rail output stage. This means that, unloaded, the output is capable of reaching within 5 mV of ground. Moreover, the DAC's linearity performance (when driving a 5 kΩ resistive load to ground) is good through the full transfer function, except for Code 0 to Code 100. Linearity degradation near ground is caused by saturation of the output amplifier. As the output is forced to sink more current, the non-linear region at the bottom of the transfer function becomes larger. Larger current demands can significantly limit output voltage swing.

AUX_DAC Register Definition

Address	Default[1]	Format	Access
0x31, 0x30	0x0000	Binary	R/W

[1] Default is valid only until the first register write cycle.

The AUX_DAC register controls the DAC function of the ADIS16203. The data bits provide a 12-bit binary format number, with 0 representing 0 V and 0x0FFFh representing 2.5 V. The data within this register is volatile and is set to 0s upon reset. This register has read/write capability.

Table 22. AUX_DAC Bit Descriptions

Bit	Description
15:12	Not used
11:0	Data bits

GENERAL-PURPOSE I/O CONTROL

As previously noted, the ADIS16203 provides two general-purpose, bidirectional I/O pins (GPIOs) that are available to the user for control of auxiliary circuits within the target application. All I/O pins are 5 V tolerant, meaning that the GPIOs support an input voltage of 5 V. Each GPIO pin has an internal pull-up resistor of approximately 100 kΩ and a drive capability of 1.6 mA. The direction, as well as the logic level, can be controlled for these GPIO pins through the GPIO_CTRL control register, as defined in Table 23.

These same GPIO pins are also controllable through the ALM_CTRL and MSC_CTRL control registers. The priority for these three control registers in controlling the two GPIO pins is MSC_CTRL has precedence over ALM_CTRL, which has precedence over GPIO_CTRL.

GPIO_CTRL Register Definition

Address	Default[1]	Format	Access
0x33, 0x32	0x0000	N/A	R/W

[1] Default is valid only until the first register write cycle.

The data within the general-purpose digital I/O control register is volatile and is set to 0s upon reset.

Table 23. GPIO_CTRL Bit Descriptions

Bit	Description
15:10	Not used
9	General-Purpose I/O Line 1 Polarity 0: Low 1: High
8	General-Purpose I/O Line 0 Polarity 0: Low 1: High
7:2	Not used
1	General-Purpose I/O Line 1, Data Direction Control 0: Input 1: Output
0	General-Purpose I/O Line 0, Data Direction Control 0: Input 1: Output

APPLICATIONS INFORMATION

HARDWARE CONSIDERATIONS

The ADIS16203 can be operated from a single 3.3 V (3.0 V to 3.6 V) power supply. The ADIS16203 integrates two decoupling capacitors that are 1 µF and 0.1 µF in value. For the local operation of the ADIS16203, no additional power supply decoupling capacitance is required.

However, if the system power supply presents a substantial amount of noise, additional filtering may be required. If additional capacitors are required, connect the ground terminal of each capacitor directly to the underlying ground plane. Finally, note that all analog and digital grounds should be referenced to the same system ground reference point.

GROUNDING AND BOARD LAYOUT RECOMMENDATIONS

Maintaining low impedance signal return paths can be very critical in managing system-level noise effects. For best results, use a single, continuous ground plane that is tied to each ADIS16203 ground pin via short trace lengths. In addition to maintaining a low impedance ground structure, routing the SPI signals away from sensitive analog circuits, such as the ADC and DACs (if they are in use), can help mitigate system-level noise risks.

SELF-TEST TIPS

When using the ADIS16203's self-test function to monitor incline angles around 0°, using the INCL_180_OUT register is more convenient than using the INCL_OUT register. Because the measurements in the INCL_OUT register jump from 0 to 359.975, they may trigger false alarms. The same philosophy can be applied to monitoring conditions around 180°. Because the INCL_OUT provides continuous measurements through 180° and the INCL_180_OUT abruptly changes from −180° to +180°, the INCL_OUT register is a more convenient choice.

BAND GAP REFERENCE

The ADIS16203 provides an on-chip band gap reference of 2.5 V that is utilized by the on-board ADC and DAC. This internal reference also appears on the VREF pin. This reference can be connected to external circuits in the system. An external buffer would be required because of the low drive capability of the VREF output.

POWER SUPPLY CONSIDERATIONS

The ADIS16203 is a precision sensing system that uses an embedded processor for critical interface and signal processing functions. Supporting this processor requires a low impedance power supply, which can manage transient current demands that happen during normal operation, as well as during the start-up process. Transient current demands start when the voltage on the VDD pin reaches ~2.1 V. Therefore, it is important for the voltage on the VDD pin to reach 3 V as quickly as possible. Linear VDD ramp profiles that reach 3 V in 100 µs provide reliable results when used in conjunction with design practices that support a low dynamic source impedance. The ADP1712 is a linear regulator that can support the recommended ramp profile. See the ADIS1620x/21x/22x Power Regulator Suggestion page for a reference design suggestion for using this regulator with the ADIS16203.

Power-On-Reset Function

The ADIS16203 has a power-on-reset (POR) function that triggers a reset if the voltage on the VDD pin fails to transition between 2.35 V and 2.7 V within 128 ms.

Transient Current from VDD Ramp Rate

Because the ADIS16203 contains 2 µF of decoupling capacitance on VDD and some systems may use additional filtering capacitance, the VDD ramp rate has a direct impact on the initial transient current requirements. Use the following formula to estimate the transient current associated with the capacitance (C) and VDD ramp rate (dV/dt):

$$i(t) = C\,dV/dt$$

For example, if VDD transitions from 0 V to 3.3 V in 33 µs, dV/dt is equal to 100000 V/S (3.3 V/33 µs). When charging the internal 2 µF capacitor (no external capacitance), the charging current for this ramp rate is 200 mA during the 33 µs ramp time. This relationship provides a tool for evaluating the initial charging currents against the current-limit thresholds of system power supplies, which can cause power supply interruptions and the appearance of failed startups. This relationship can also be important for maintaining surge current ratings of series elements.

ASSEMBLY

When developing a process flow for installing ADIS16203 devices on printed circuit boards (PCBs), see the JEDEC J-STD-020C standard for reflow temperature profile and processing information. The ADIS16203 can use the tin (Sn), lead (Pb) eutectic process and the Pb-free eutectic process from this standard. One exception to the standard is that the peak temperature exposure is 240°C. For a complete list of assembly process suggestions, see the ADIS162xx LGA Assembly Guidelines page. See Figure 33 for an example pattern of the location of the ADIS16203 on a PCB.

EXAMPLE PAD LAYOUT

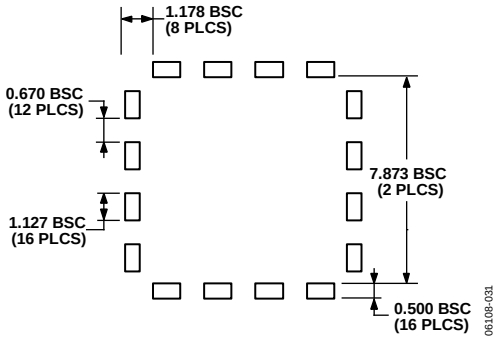

Figure 33. Example Pad Layout

X-RAY SENSITIVITY

Exposure to high dose rate X-rays, such as those in production systems that inspect solder joints in electronic assemblies, may affect accelerometer bias errors. For optimal performance, avoid exposing the ADIS16203 to this type of inspection.

OUTLINE DIMENSIONS

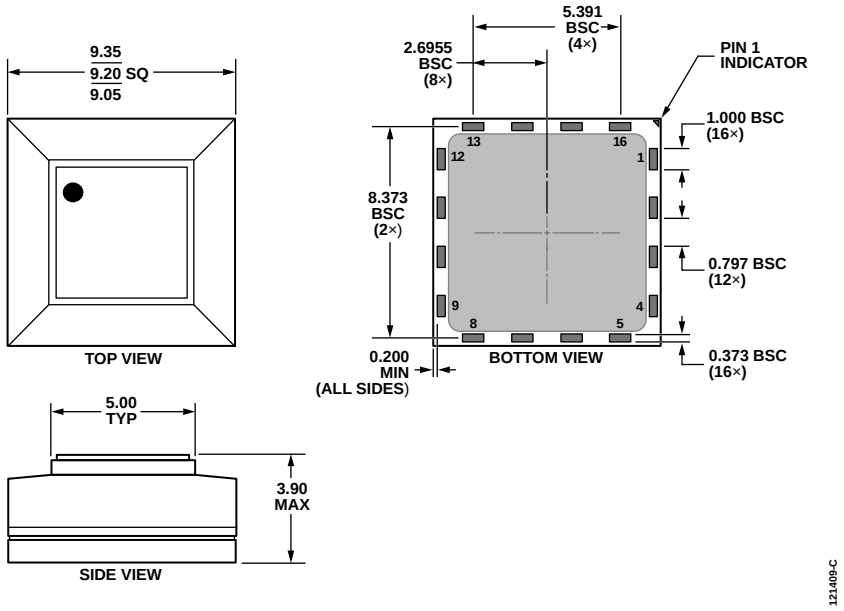

Figure 34. 16-Terminal Land Grid Array [LGA]
(CC-16-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16203CCCZ	−40°C to +125°C	16-Terminal Land Grid Array [LGA]	CC-16-2
ADIS16203/PCBZ		Evaluation Board	
EVAL-ADIS2Z		Evaluation System	

[1] Z = RoHS Compliant Part.