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REVISION HISTORY

9/2017—Rev. E to Rev. F

Changed CP-8-2 to CP-8-13	Throughout
Updated Outline Dimensions	17
Changes to Ordering Guide	17

10/2013—Rev. D to Rev. E

Change to Figure 15 Caption	7
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Changes to Figure 46 through Figure 50	13
Changes to Figure 53 and Figure 54	14

2/2013—Rev. C to Rev. D

Changes to Figure 44	12
Changes to Figure 46 and Figure 49	13

12/2009—Rev. B to Rev. C

Changes to Table 1	1
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10/2008—Rev. A to Rev. B

Added AD8597	Universal
Added LFCSP_VD	Universal
Added Table 1	1

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Changes to Specifications Section	3
Changes to Absolute Maximum Ratings Section	5
Changes to Typical Performance Characteristics Section	6
Added Figure 12 and Figure 15	7
Added Figure 18 and Figure 19	8
Added Figure 30 and Figure 33	10
Added Figure 34 to Figure 38	11
Added Figure 42 and Figure 45	12
Added Figure 52, Figure 55, Figure 57	14
Added Functional Operation Section	15
Added Figure 58	15
Updated Outline Dimensions	17
Changes to Ordering Guide	17

4/2007—Rev. 0 to Rev. A

Updated Layout	5
Changes to Figure 45 Caption	12
Added Figure 48	12
Changes to Figure 51 Caption	13

2/2007—Revision 0: Initial Version

SPECIFICATIONS

$V_{SY} = \pm 5\text{ V}$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		15	120	μV
					180	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.8	2.2	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	210	nA
					340	nA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		65	250	nA
					340	nA
Input Voltage Range	IVR		-2.0		+2.0	V
Common-Mode Rejection Ratio	CMRR	$-2.0\text{ V} \leq V_{CM} \leq +2.0\text{ V}$	120	135		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	105			dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 600\ \Omega$, $V_O = -11\text{ V to } +11\text{ V}$	105	110		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100			dB
Input Capacitance						
Differential Capacitance	C_{DIFF}			15.4		pF
Common-Mode Capacitance	C_{CM}			5.5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 600\ \Omega$	3.5	3.7		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	3.3			V
		$R_L = 2\text{ k}\Omega$	3.7	3.8		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	3.5			V
Output Voltage Low	V_{OL}	$R_L = 600\ \Omega$		-3.6	-3.4	V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			-3.3	V
		$R_L = 2\text{ k}\Omega$		-3.7	-3.5	V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			-3.4	V
Output Short-Circuit Current	I_{SC}			± 52		mA
Closed-Loop Output Impedance	Z_{OUT}	At 1 MHz, $A_V = 1$		5		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 18\text{ V to } \pm 4.5\text{ V}$	120	140		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	118			dB
Supply Current per Amplifier	I_{SY}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		4.8	5.5	mA
					6.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$A_V = -1$, $R_L = 2\text{ k}\Omega$		14		V/ μs
		$A_V = 1$, $R_L = 2\text{ k}\Omega$		14		V/ μs
Settling Time	t_S	To 0.01%, step = 10 V		2		μs
Gain Bandwidth Product	GBP			10		MHz
Phase Margin	Φ_M			60		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	0.1 Hz to 10 Hz		76		nV p-p
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		1.07	1.15	nV/ $\sqrt{\text{Hz}}$
		$f = 10\text{ Hz}$			1.5	nV/ $\sqrt{\text{Hz}}$
Correlated Current Noise		$f = 1\text{ kHz}$		2.0		pA/ $\sqrt{\text{Hz}}$
		$f = 10\text{ Hz}$		4.2		pA/ $\sqrt{\text{Hz}}$
Uncorrelated Current Noise		$f = 1\text{ kHz}$		2.4		pA/ $\sqrt{\text{Hz}}$
		$f = 10\text{ Hz}$		5.2		pA/ $\sqrt{\text{Hz}}$
Total Harmonic Distortion + Noise	THD + N	$G = 1$, $R_L \geq 1\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{RMS} = 1\text{ V}$		-120		dB
Channel Separation	CS	$f = 10\text{ kHz}$		-120		dB

$V_S = \pm 15\text{ V}$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise specified.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V _{OS}	−40°C ≤ T _A ≤ +125°C		10	120 180	μV μV
Offset Voltage Drift	ΔV _{OS} /ΔT	−40°C ≤ T _A ≤ +125°C		0.8	2.2	μV/°C
Input Bias Current	I _B	−40°C ≤ T _A ≤ +125°C		25	200 300	nA nA
Input Offset Current	I _{OS}	−40°C ≤ T _A ≤ +125°C		50	200 300	nA nA
Input Voltage Range	IVR		−12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	−12.5 V ≤ V _{CM} ≤ +12.5 V −40°C ≤ T _A ≤ +125°C	120 115	135		dB dB
Large Signal Voltage Gain	A _{VO}	R _L ≥ 600 Ω, V _O = −11 V to +11 V −40°C ≤ T _A ≤ +125°C	110 106	116		dB dB
Input Capacitance						
Differential Capacitance	C _{DIFF}			12.1		pF
Common-Mode Capacitance	C _{CM}			5.1		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V _{OH}	R _L = 600 Ω −40°C ≤ T _A ≤ +125°C	13.1 12.8	13.4		V V
		R _L = 2 kΩ −40°C ≤ T _A ≤ +125°C	13.5 13.2	13.7		V V
Output Voltage Low	V _{OL}	R _L = 600 Ω −40°C ≤ T _A ≤ +125°C		−13.2	−12.9	V V
		R _L = 2 kΩ −40°C ≤ T _A ≤ +125°C		−13.5	−12.8	V V
					−13.3	V
Output Short-Circuit Current	I _{SC}			±52		mA
Closed-Loop Output Impedance	Z _{OUT}	At 1 MHz, A _V = 1		5		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V _{SY} = ±18 V to ±4.5 V −40°C ≤ T _A ≤ +125°C	120 118	140		dB dB
Supply Current per Amplifier	I _{SY}	−40°C ≤ T _A ≤ +125°C		5.0	5.7 6.75	mA mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	A _V = −1, R _L = 2 kΩ A _V = 1, R _L = 2 kΩ		16 15		V/μs V/μs
Settling Time	t _s	To 0.01%, step = 10 V		2		μs
Gain Bandwidth Product	GBP			10		MHz
Phase Margin	Φ _M			65		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e _n p-p	0.1 Hz to 10 Hz		76		nV p-p
Voltage Noise Density	e _n	f = 1 kHz		1.07	1.15	nV/√Hz
		f = 10 Hz			1.5	nV/√Hz
Correlated Current Noise		f = 1 kHz		1.9		pA/√Hz
		f = 10 Hz		4.3		pA/√Hz
Uncorrelated Current Noise		f = 1 kHz		2.3		pA/√Hz
		f = 10 Hz		5.3		pA/√Hz
Total Harmonic Distortion + Noise	THD + N	G = 1, R _L ≥ 1 kΩ, f = 1 kHz, V _{RMS} = 3 V		−120		dB
Channel Separation	CS	f = 10 kHz		−120		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	$\pm 18\text{ V}$
Input Voltage	$-V \leq V_{\text{IN}} \leq +V$
Differential Input Voltage ¹	$\pm 1\text{ V}$
Output Short-Circuit to GND	Indefinite
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-40°C to $+125^{\circ}\text{C}$
Lead Temperature Range (Soldering 60 sec)	300°C
Junction Temperature	150°C

¹ If the differential input voltage exceeds 1 V, limit the current to 5 mA.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified with the device soldered on a circuit board with its exposed paddle soldered to a pad (if applicable) on a 4-layer JEDEC standard PCB with zero air flow.

Table 5.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead LFCSP (CP-8-13)	78	20	$^{\circ}\text{C/W}$
8-Lead SOIC (R-8) (AD8597)	140	39	$^{\circ}\text{C/W}$
8-Lead SOIC (R-8) (AD8599)	120	36	$^{\circ}\text{C/W}$

POWER SEQUENCING

Apply the op amp supplies simultaneously. The op amp supplies must be stable before any input signals are applied. In any case, the input current must be limited to 5 mA.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

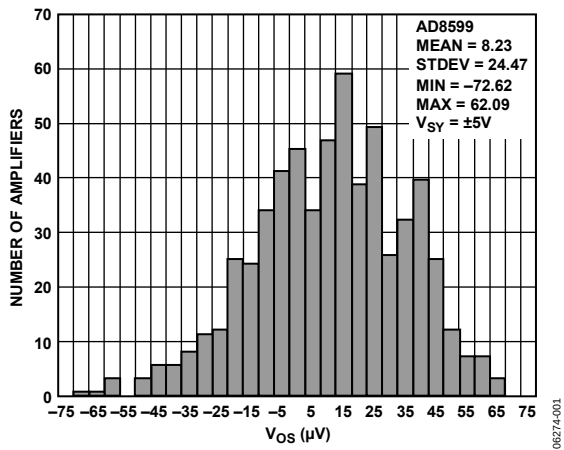


Figure 4. Input Offset Voltage Distribution

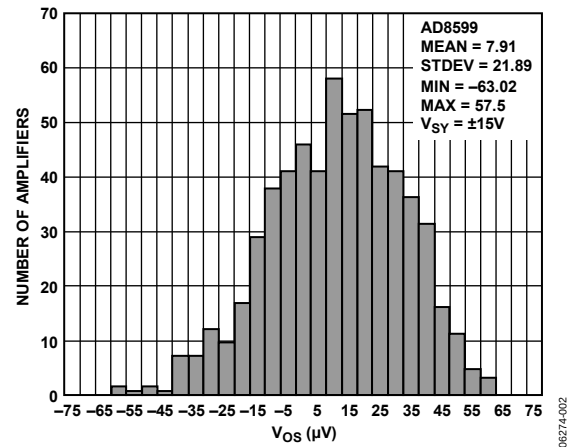
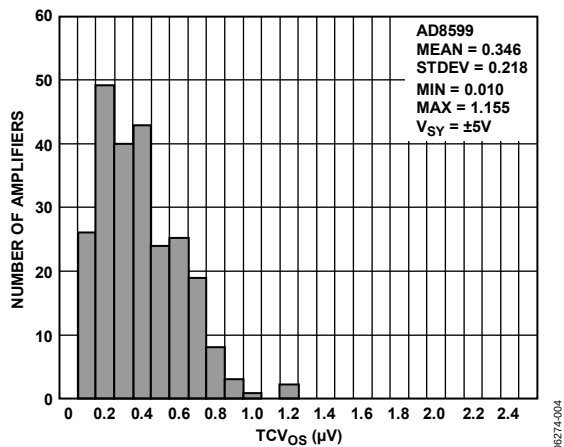
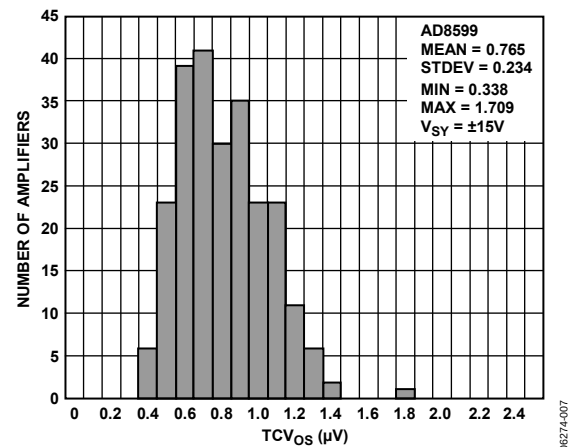
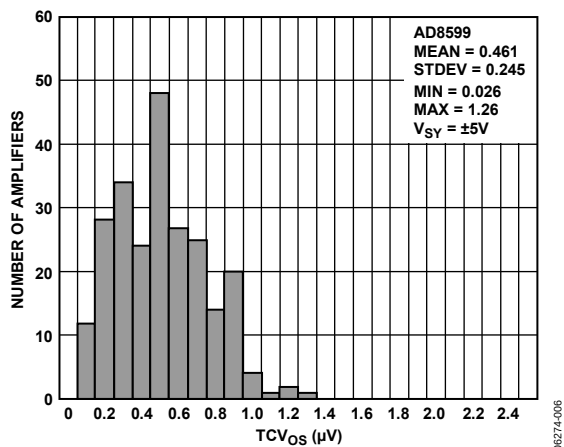
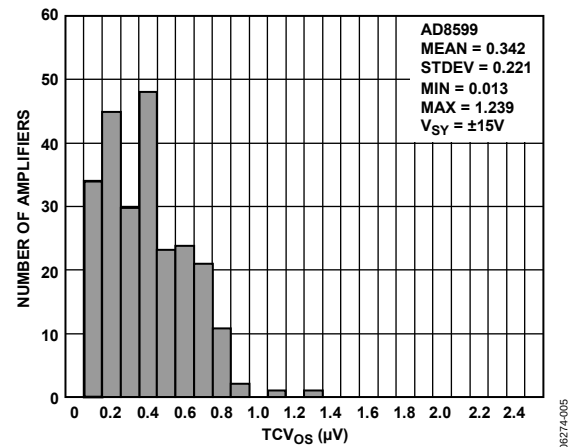


Figure 7. Input Offset Voltage Distribution

Figure 5. TCV_{OS} Distribution, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ Figure 8. TCV_{OS} Distribution, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ Figure 6. TCV_{OS} Distribution, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ Figure 9. TCV_{OS} Distribution, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$

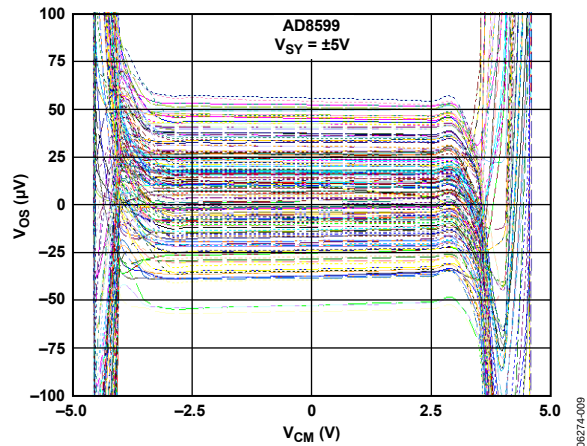
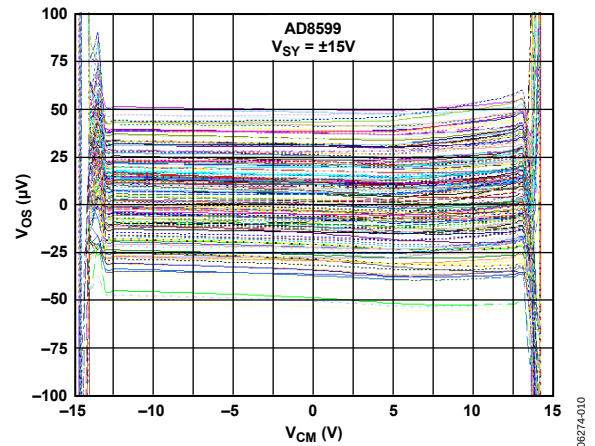
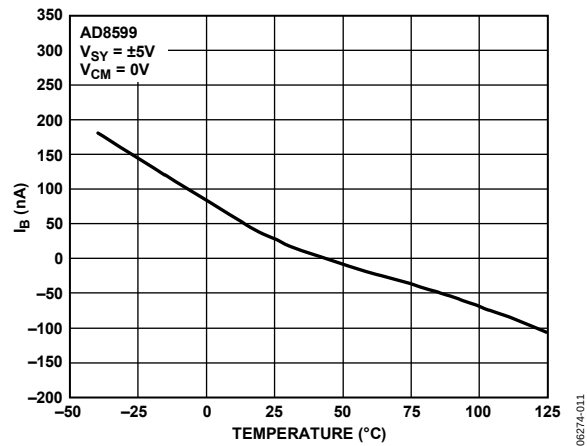
Figure 10. Offset Voltage vs. V_{CM} Figure 13. Offset Voltage vs. V_{CM} 

Figure 11. Input Bias Current vs. Temperature

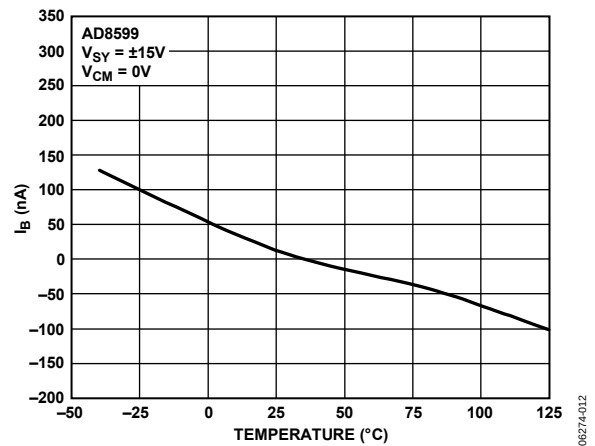


Figure 14. Input Bias Current vs. Temperature

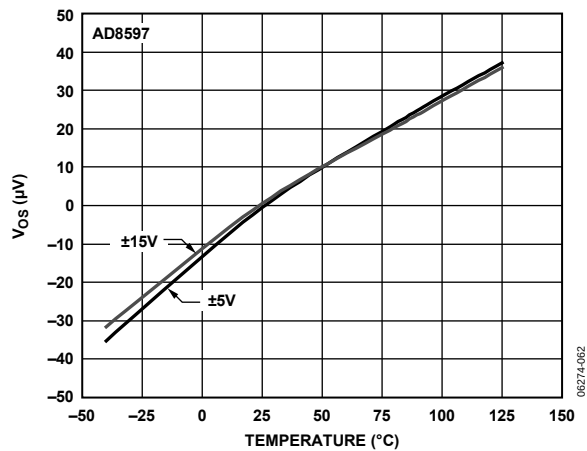
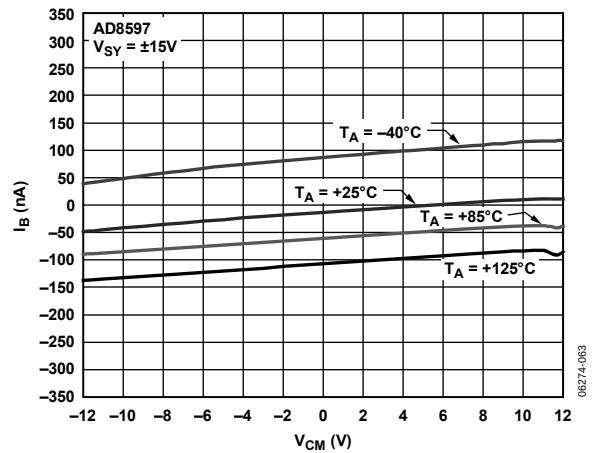


Figure 12. Input Offset Voltage vs. Temperature

Figure 15. Input Bias Current vs. Common-Mode Voltage (V_{CM}) Over Temperature

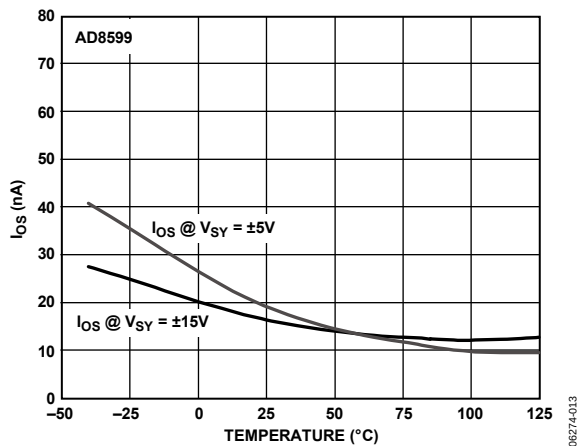


Figure 16. Input Offset Current vs. Temperature

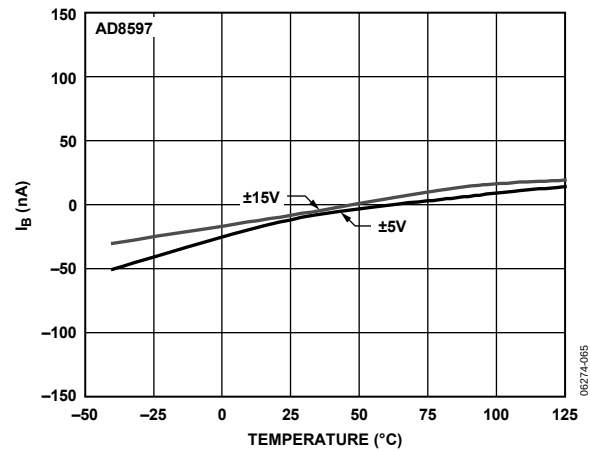


Figure 19. Input Offset Current vs. Temperature

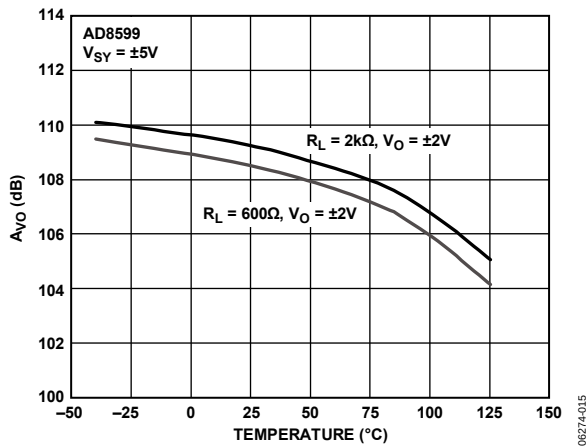


Figure 17. Large Signal Voltage Gain vs. Temperature

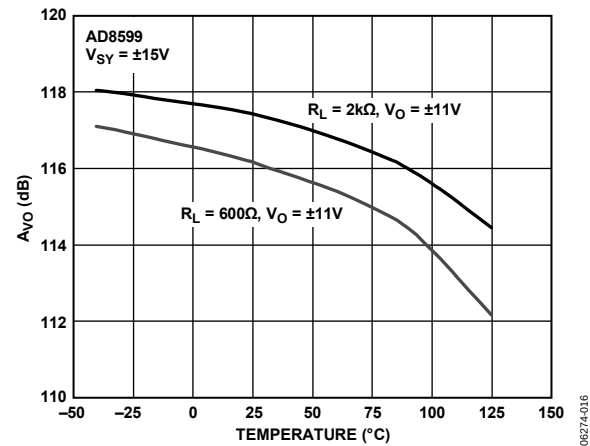


Figure 20. Large Signal Voltage Gain vs. Temperature

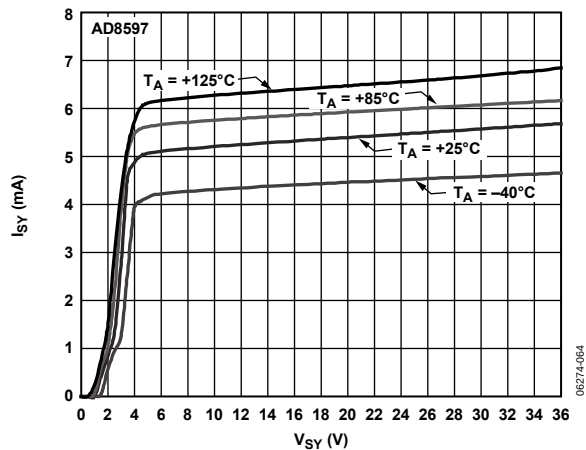
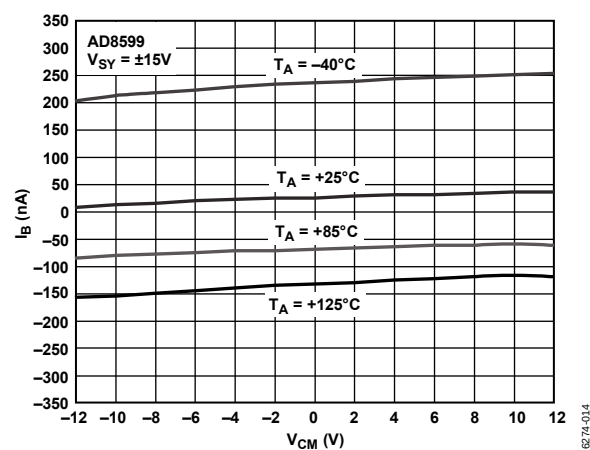
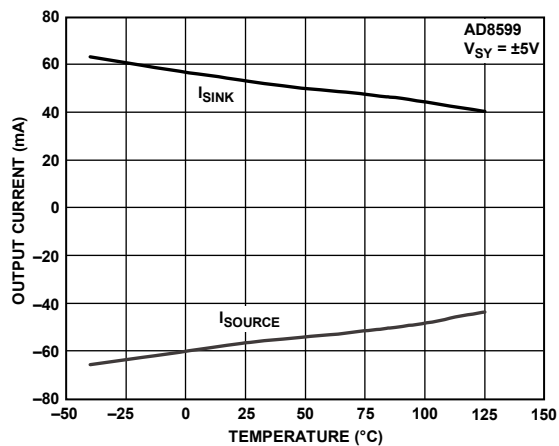
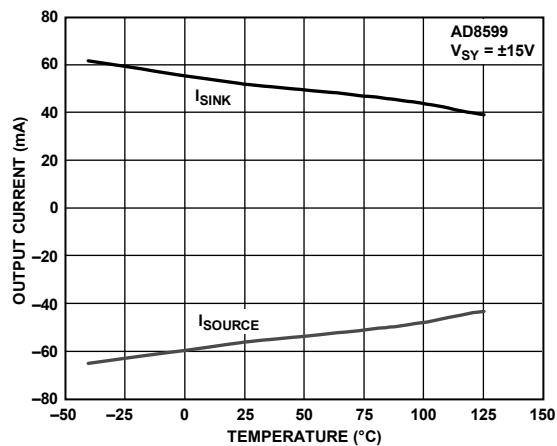


Figure 18. Supply Current vs. Supply Voltage

Figure 21. Input Bias Current vs. V_{CM}

Figure 22. I_{SC} vs. Temperature

06274-017

Figure 25. I_{SC} vs. Temperature

06274-018

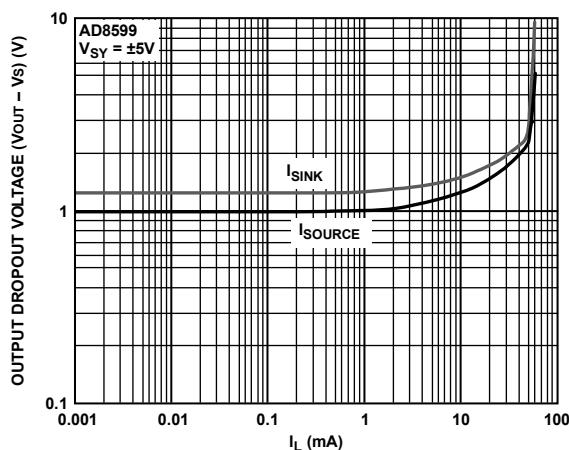


Figure 23. Output Dropout Voltage vs. Current Load

06274-021

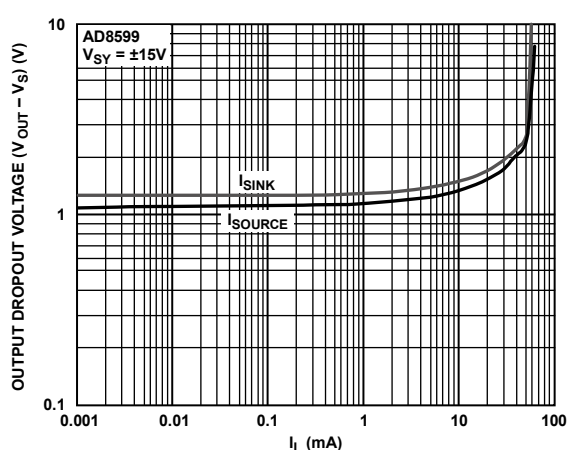


Figure 26. Output Dropout Voltage vs. Current Load

06274-022

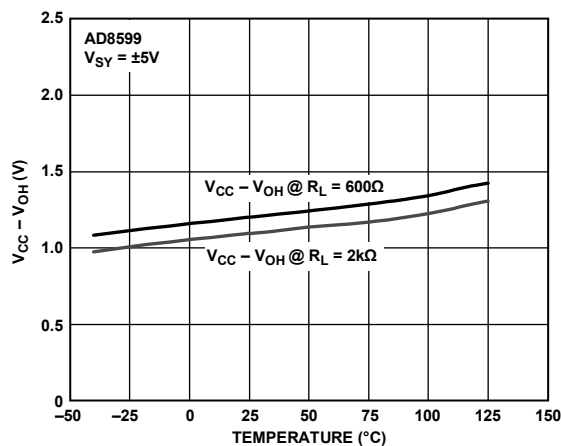


Figure 24. Output Saturation Voltage vs. Temperature

06274-027

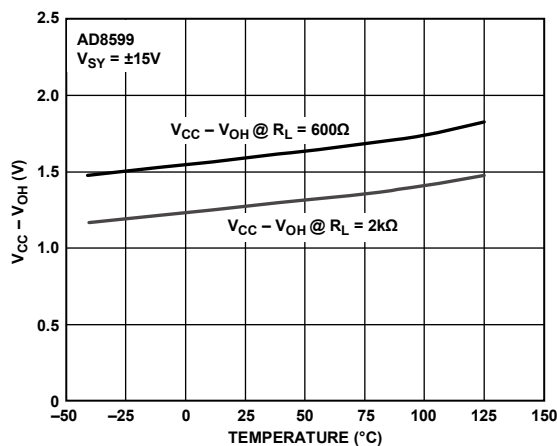


Figure 27. Output Saturation Voltage vs. Temperature

06274-029

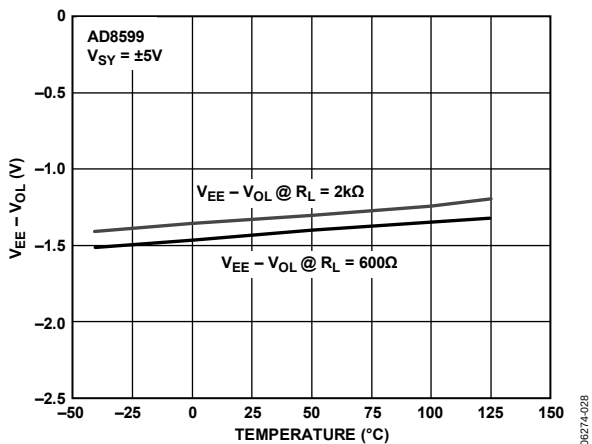


Figure 28. Output Saturation Voltage vs. Temperature

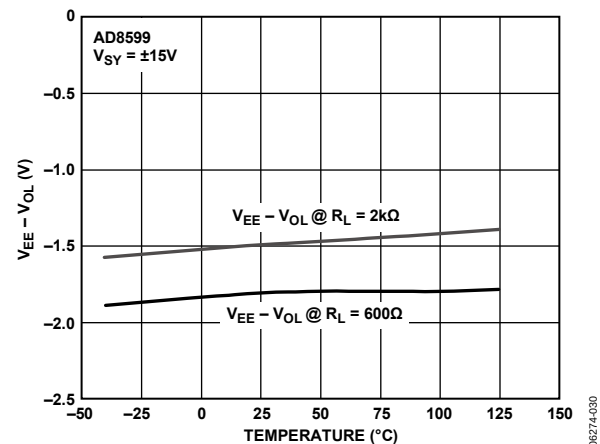


Figure 31. Output Saturation Voltage vs. Temperature

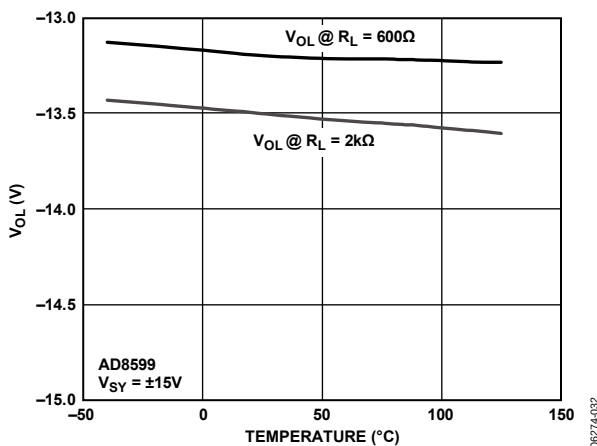


Figure 29. Output Voltage Low vs. Temperature

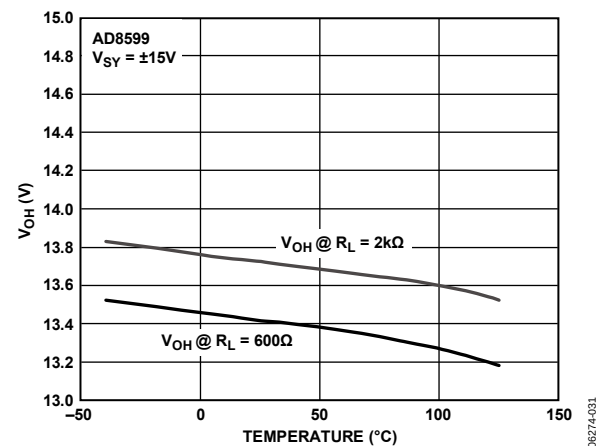


Figure 32. Output Voltage High vs. Temperature

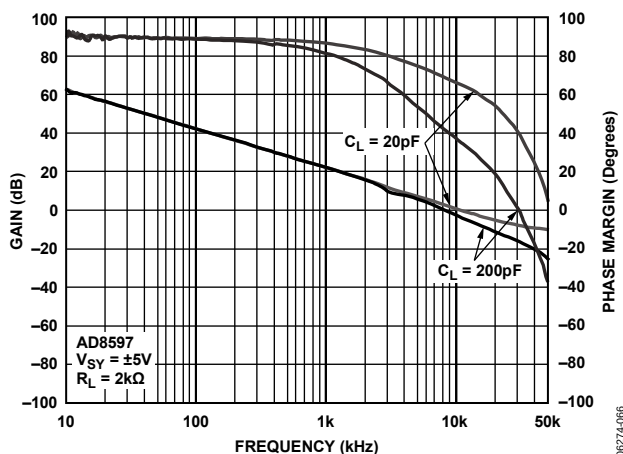


Figure 30. Gain and Phase vs. Frequency

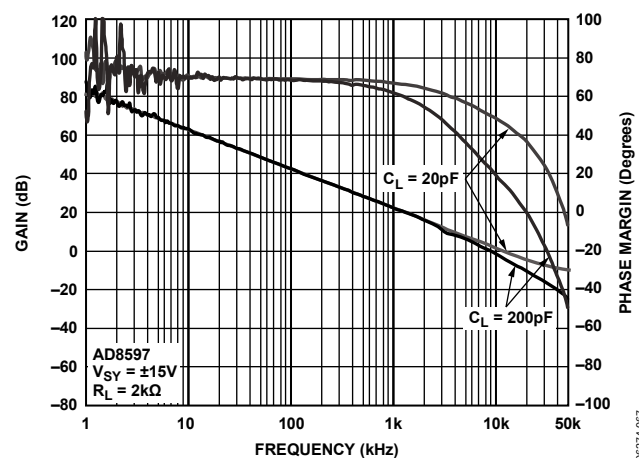


Figure 33. Gain and Phase vs. Frequency

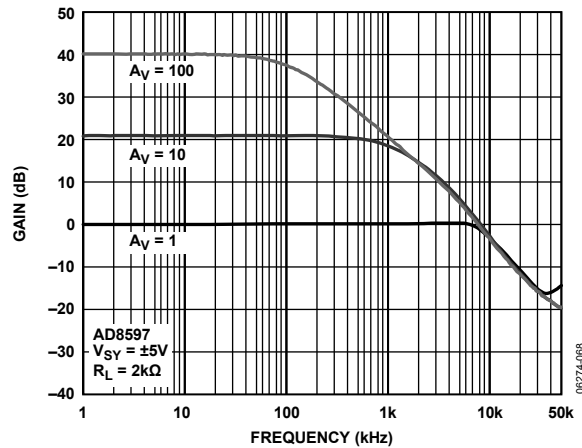


Figure 34. Closed-Loop Gain vs. Frequency

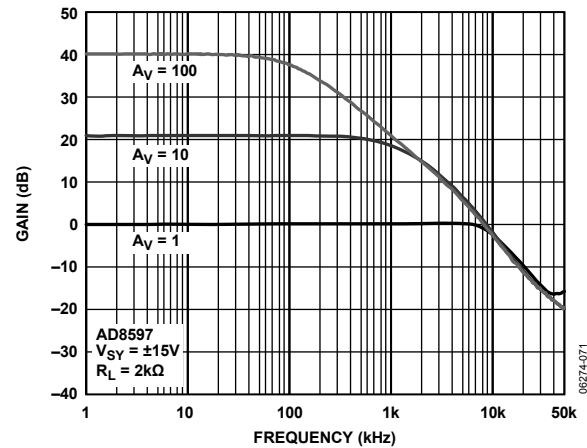


Figure 37. Closed-Loop Gain vs. Frequency

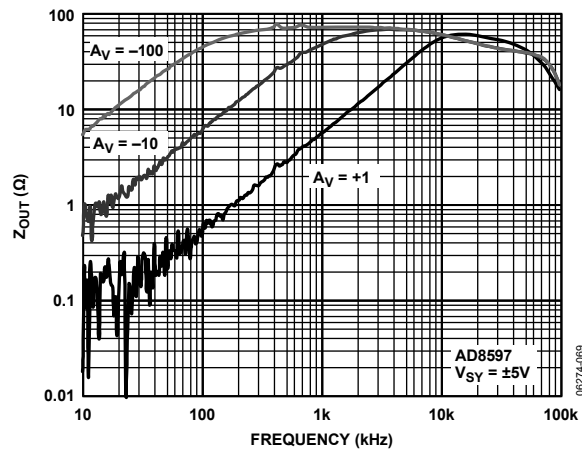


Figure 35. Closed-Loop Output Impedance vs. Frequency

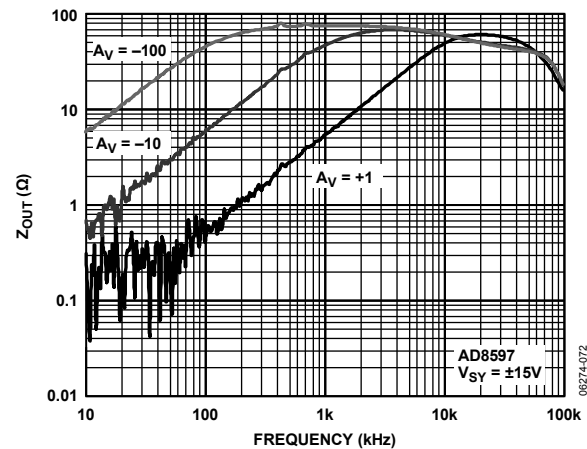


Figure 38. Closed-Loop Output Impedance vs. Frequency

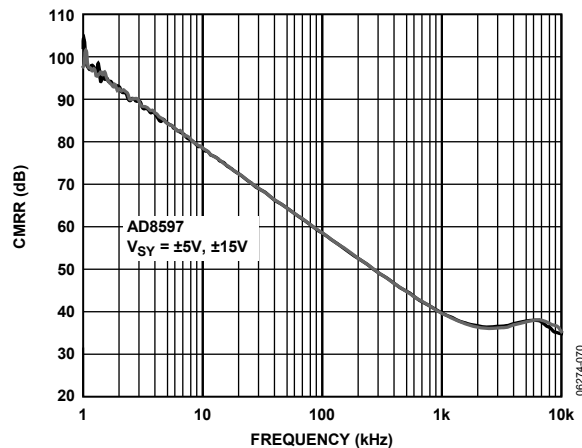


Figure 36. Common-Mode Rejection Ratio vs. Frequency

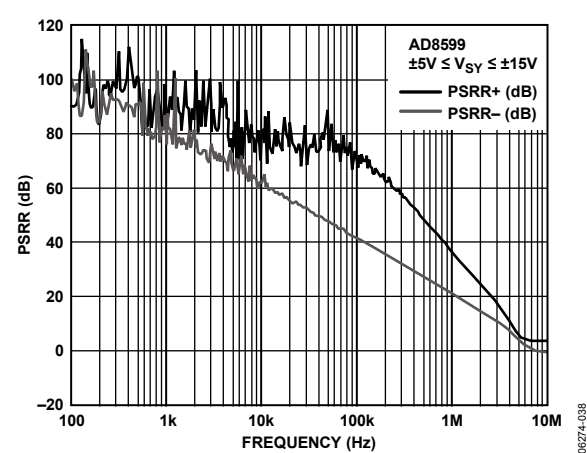


Figure 39. Power Supply Rejection Ratio vs. Frequency

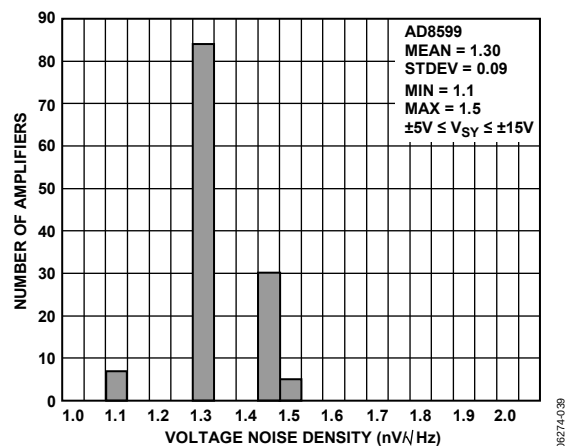


Figure 40. Voltage Noise Density at 10 Hz

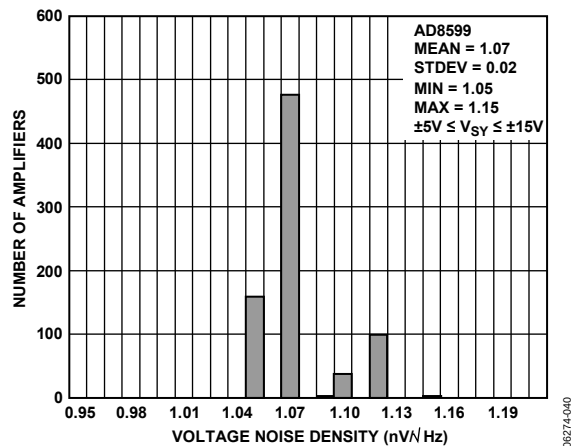


Figure 43. Voltage Noise Density at 1 kHz

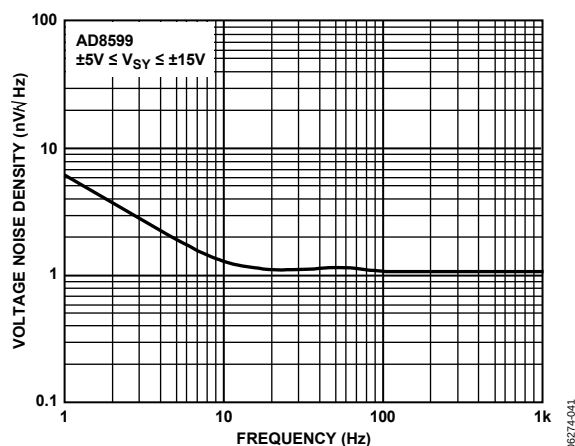


Figure 41. Voltage Noise Density vs. Frequency

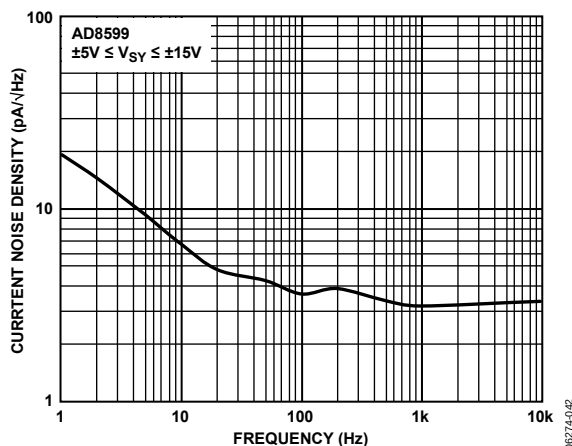


Figure 44. Current Noise Density vs. Frequency

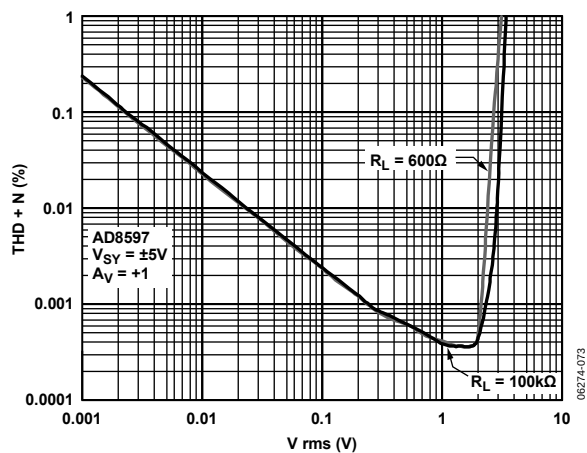


Figure 42. THD + N vs. Amplitude

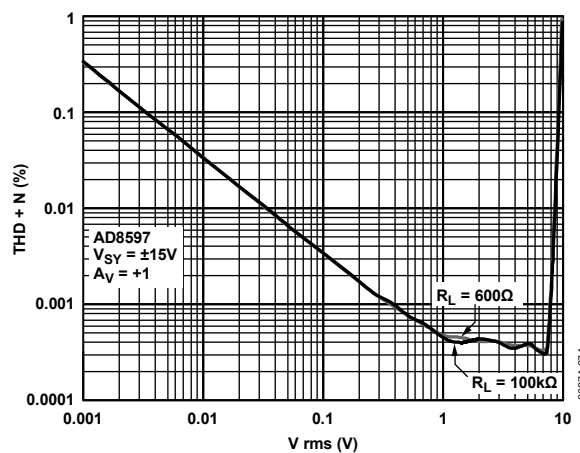


Figure 45. THD + N vs. Amplitude

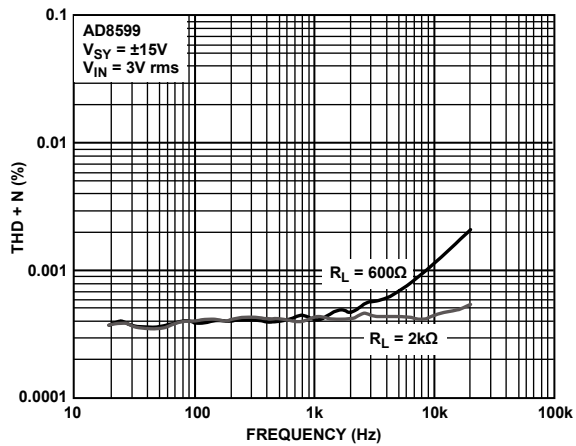


Figure 46. THD + N vs. Frequency

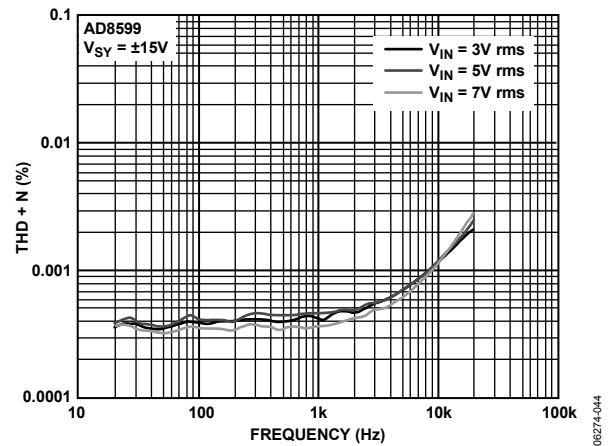


Figure 49. THD + N vs. Frequency

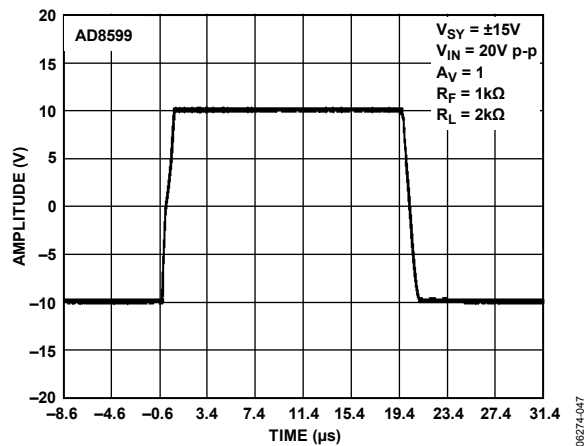


Figure 47. Large Signal Response

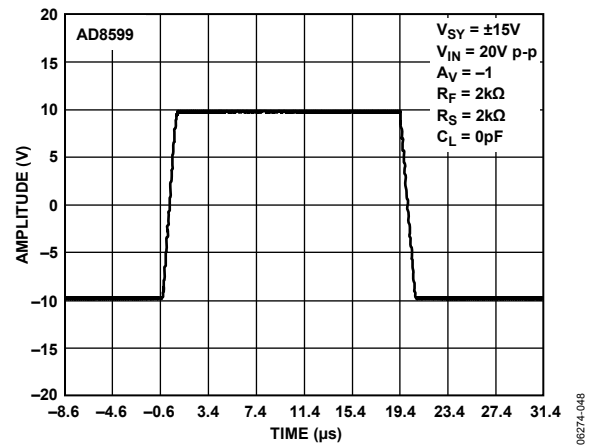


Figure 50. Large Signal Response

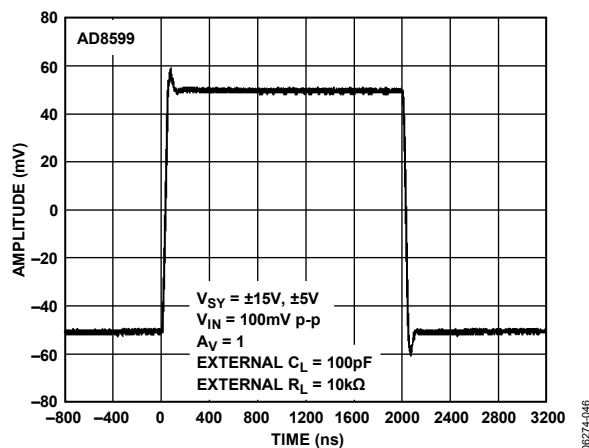


Figure 48. Small Signal Response

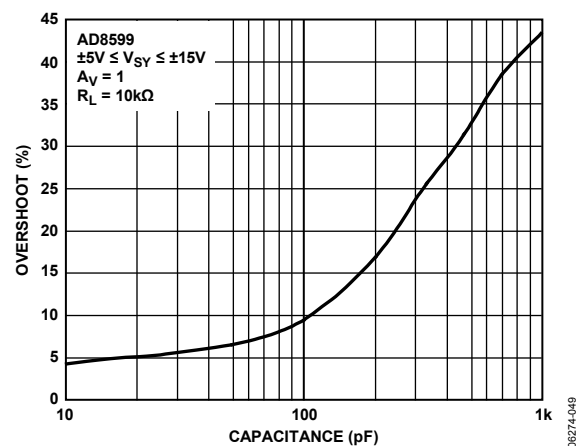


Figure 51. Overshoot vs. Capacitance

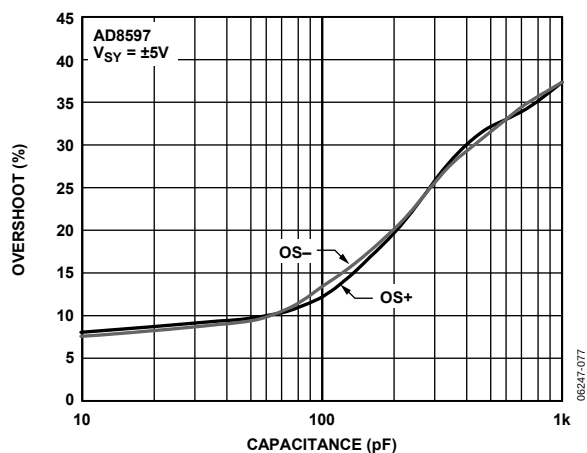


Figure 52. Overshoot vs. Capacitive Load

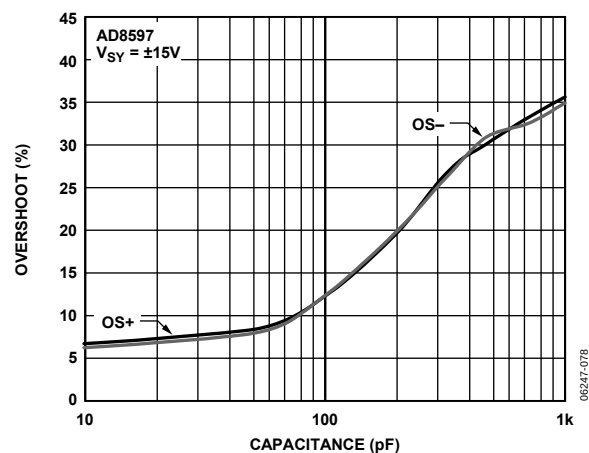


Figure 55. Overshoot vs. Capacitive Load

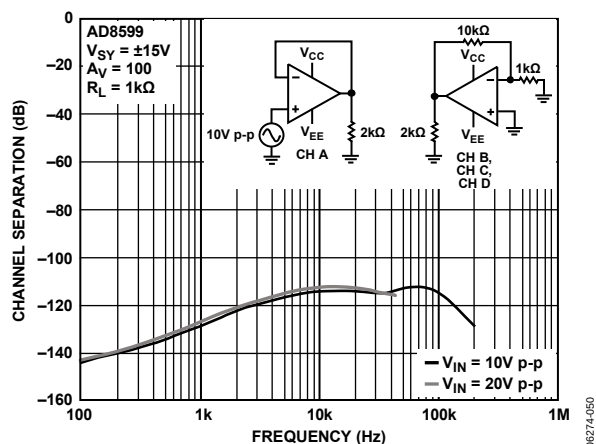


Figure 53. Channel Separation vs. Frequency

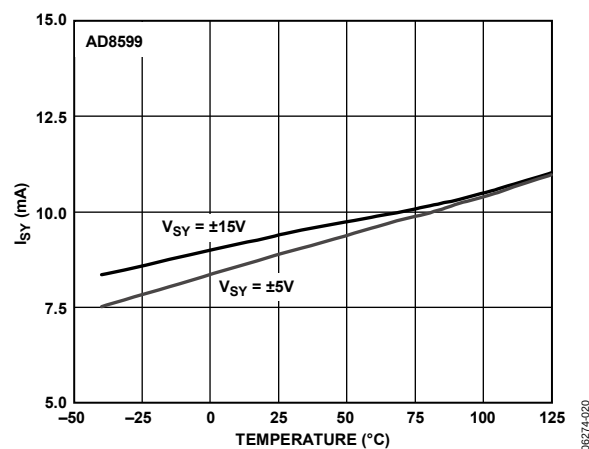


Figure 56. Supply Current vs. Temperature

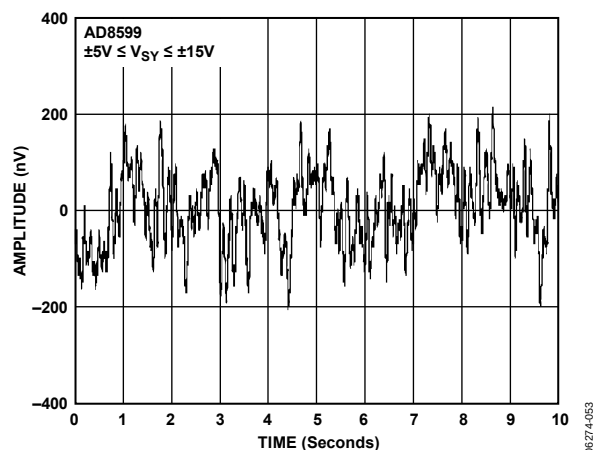


Figure 54. Peak-to-Peak Noise

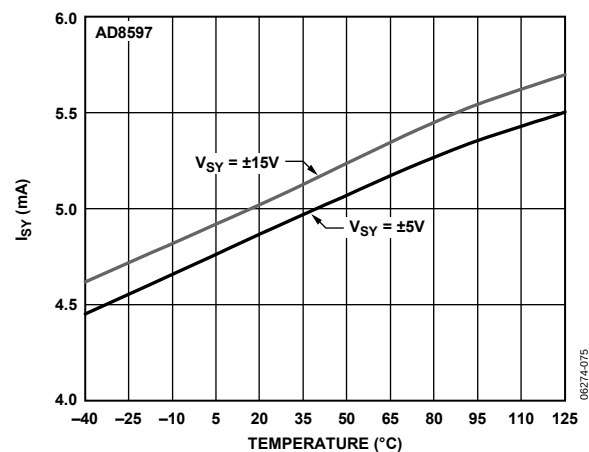


Figure 57. Supply Current vs. Temperature

FUNCTIONAL OPERATION

INPUT VOLTAGE RANGE

The AD8597/AD8599 are not rail-to-rail input amplifiers; therefore, care is required to ensure that both inputs do not exceed the input voltage range. Under normal negative feedback operating conditions, the amplifier corrects its output to ensure that the two inputs are at the same voltage. However, if either input exceeds the input voltage range, the loop opens and large currents begin to flow through the ESD protection diodes in the amplifier.

These diodes are connected between the inputs and each supply rail to protect the input transistors against an electrostatic discharge event and they are normally reverse-biased. However, if the input voltage exceeds the supply voltage, these ESD diodes can become forward-biased. Without current limiting, excessive amounts of current may flow through these diodes, causing permanent damage to the device. If inputs are subject to over-voltage, insert appropriate series resistors to limit the diode current to less than 5 mA maximum.

The input stage has two diodes between the input pins to protect the differential pair. Under high slew rate conditions, when the op amp is connected as a voltage follower, the diodes may become forward-biased and the source may try to drive the output. Place a small resistor in the feedback loop and in the noninverting input. The noise of a 100 Ω resistor at room temperature is ~ 1.25 nV/ $\sqrt{\text{Hz}}$, which is higher than the AD8597/AD8599. Thus, there is a tradeoff between noise performance and protection. If possible, place limiting earlier in the signal path. For further details, see the *Amplifier Input Protection... Friend or Foe?* article at http://www.analog.com/amplifier_input.

Because of the large transistors used to achieve low noise, the input capacitance may seem rather high. To take advantage of the low noise performance, impedance around the op amp must be low, less than 500 Ω . Under these conditions, the pole from the input capacitance must be greater than 50 MHz, which does not affect the signal bandwidth.

OUTPUT PHASE REVERSAL

Output phase reversal occurs in some amplifiers when the input common-mode voltage range is exceeded. As the common-mode voltage is moved outside the input voltage range, the outputs of these amplifiers can suddenly jump in the opposite direction to the supply rail. This is the result of the differential input pair shutting down that causes a radical shifting of internal voltages that results in the erratic output behavior.

The AD8597/AD8599 amplifiers are carefully designed to prevent any output phase reversal if both inputs are maintained within the specified input voltage range. If one or both inputs exceed the input voltage range but remain within the supply rails, the op amp specifications, such as CMRR, are not guaranteed, but the output remains close to the correct value.

NOISE AND SOURCE IMPEDANCE CONSIDERATIONS

The AD8597/AD8599 ultralow voltage noise of 1.1 nV/ $\sqrt{\text{Hz}}$ is achieved with special input transistors running at high collector current. Therefore, it is important to consider the total input-referred noise (e_N total), which includes contributions from voltage noise (e_N), current noise (i_N), and resistor noise ($\sqrt{4 kTR_S}$).

$$e_N \text{ total} = [e_N^2 + 4 kTR_S + (i_N \times R_S)^2]^{1/2} \quad (1)$$

where R_S is the total input source resistance.

This equation is plotted for the AD8597/AD8599 in Figure 58. Because optimum dc performance is obtained with matched source resistances, this case is considered even though it is clear from Equation 1 that eliminating the balancing source resistance lowers the total noise by reducing the total R_S by a factor of 2.

At a very low source resistance ($R_S < 50 \Omega$), the voltage noise of the amplifier dominates. As source resistance increases, the Johnson noise of R_S dominates until a higher resistance of $R_S > 2 \text{ k}\Omega$ is achieved; the current noise component is larger than the resistor noise.

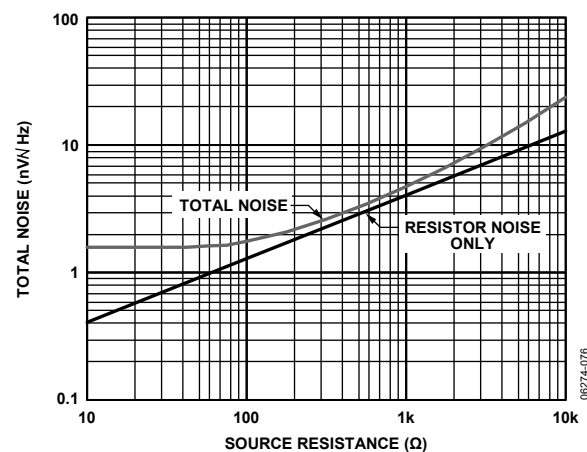


Figure 58. Noise vs. Source Resistance

The AD8597/AD8599 are the optimum choice for low noise performance if the source resistance is kept $< 1\text{ k}\Omega$. At higher values of source resistance, optimum performance with respect to only noise is obtained with other amplifiers from Analog Devices. Both voltage noise and current noise must be considered. For more information on avoiding noise from grounding problems and inadequate bypassing, see the [AN-345 Application Note, Grounding for Low- and High-Frequency Circuits](#). For

general noise theory with extensive calculations, see the [AN-358 Application Note, Noise and Operational Amplifier Circuits](#). A good selection table for low noise op amps can be found in [AN-940 Application Note, Low Noise Amplifier Selection Guide for Optimal Noise Performance](#). An interesting note on using one section of a monolithic dual to phase compensate the other section is in the [AN-107 Application Note, Active Feedback Improves Amplifier Phase Accuracy](#).

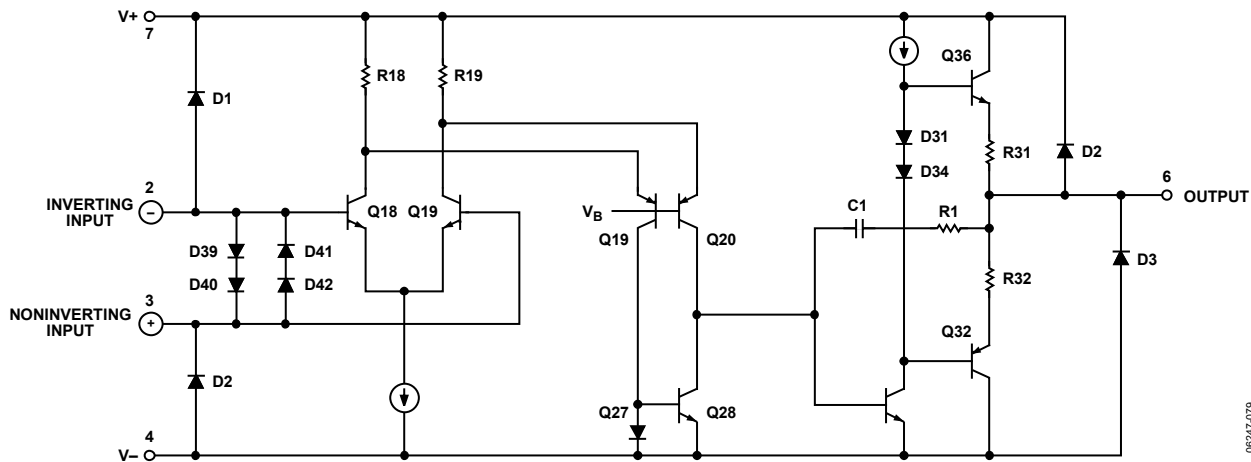
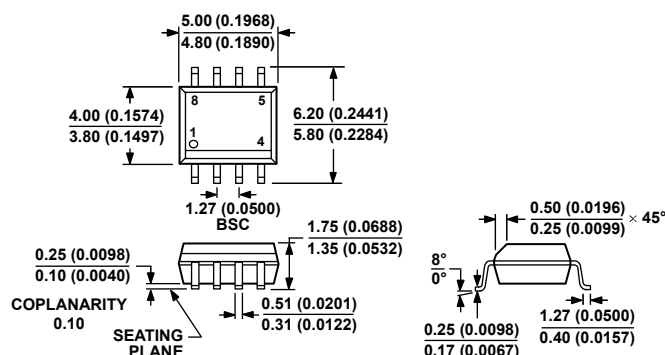


Figure 59. Simplified Schematic

06247-079

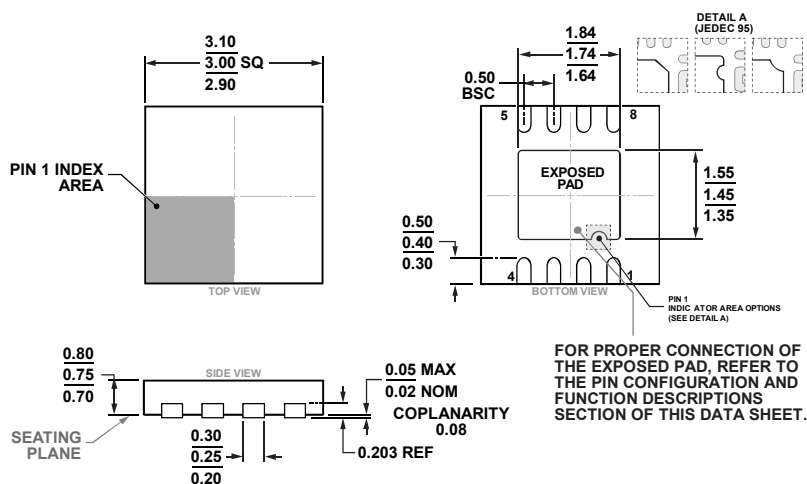
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 60. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-229-WEED-4

Figure 61. 8-Lead Lead Frame Chip Scale Package [LFCSFP]
3 mm x 3 mm Body and 0.75 mm Package Height
(CP-8-13)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
AD8597ACPZ-R2	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSFP]	CP-8-13	A22
AD8597ACPZ-REEL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSFP]	CP-8-13	A22
AD8597ACPZ-REEL7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSFP]	CP-8-13	A22
AD8597ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8597ARZ-REEL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8597ARZ-REEL7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8599ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8599ARZ-REEL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8599ARZ-REEL7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	

¹ Z = RoHS Complaint Part.

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