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8/07—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = 2.5 V ± 5%, V_{DRIVE} = 1.8 V to 3.6 V, V_{REF} = 5 V, MCLK = 1 MHz, common-mode input = $V_{REF}/2$, T_A = −40°C to +105°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT DATA RATE (ODR)					
AD7767	Decimate by 8			128	kHz
AD7767-1	Decimate by 16			64	kHz
AD7767-2	Decimate by 32			32	kHz
ANALOG INPUT[1]					
Differential Input Voltage	$V_{IN+} - V_{IN-}$			$\pm V_{REF}$	V p-p
Absolute Input Voltage	V_{IN+}	−0.1		$+V_{REF} + 0.1$	V
	V_{IN-}	−0.1		$+V_{REF} + 0.1$	V
Common-Mode Input Voltage		$V_{REF}/2 - 5\%$	$V_{REF}/2$	$V_{REF}/2 + 5\%$	V
Input Capacitance			22		pF
DYNAMIC PERFORMANCE					
AD7767	Decimate by 8, ODR = 128 kHz				
Dynamic Range[2]	Shorted inputs	108	109.5		dB
Signal-to-Noise Ratio (SNR)[2]	Full-scale input amplitude, 1 kHz tone	107	108.5		dB
Spurious-Free Dynamic Range (SFDR)[2]	Full-scale input amplitude, 1 kHz tone		−128	−116	dB
Total Harmonic Distortion (THD)[2]	Full-scale input amplitude, 1 kHz tone		−118	−105	dB
Intermodulation Distortion (IMD)[2]	Tone A = 49.7 kHz, Tone B = 50.3 kHz				
Second-Order Terms			−133		dB
Third-Order Terms			−109		dB
AD7767-1	Decimate by 16, ODR = 64 kHz				
Dynamic Range[2]	Shorted inputs	111	112.5		dB
Signal-to-Noise Ratio (SNR)[2]	Full-scale input amplitude, 1 kHz tone	110	111.5		dB
Spurious-Free Dynamic Range (SFDR)[2]	Full-scale input amplitude, 1 kHz tone		−128	−116	dB
Total Harmonic Distortion (THD)[2]	Full-scale input amplitude, 1 kHz tone		−118	−105	dB
Intermodulation Distortion (IMD)[2]	Tone A = 24.7 kHz, Tone B = 25.3 kHz				dB
Second-Order Terms			−133		dB
Third-Order Terms			−108		dB
AD7767-2	Decimate by 32, ODR = 32 kHz				
Dynamic Range[2]	Shorted inputs	114	115.5		dB
Signal-to-Noise Ratio (SNR)[2]	Full-scale input amplitude, 1 kHz tone	112	113.5		dB
Spurious-Free Dynamic Range (SFDR)[2]	Full-scale input amplitude, 1 kHz tone		−128	−116	dB
Total Harmonic Distortion (THD)[2]	Full-scale input amplitude, 1 kHz tone		−118	−105	dB
Intermodulation Distortion (IMD)[2]	Tone A = 11.7 kHz, Tone B = 12.3 kHz				dB
Second-Order Terms			−137		dB
Third-Order Terms			−108		dB
DC ACCURACY[1]	For all devices				
Resolution	No missing codes	24			Bits
Differential Nonlinearity[2]	Guaranteed monotonic to 24 bits				
Integral Nonlinearity[2]	18-bit linearity		±3	±7.6	ppm
Zero Error[2]			20		µV
Gain Error[2]			0.0075	0.075	% FS
Zero Error Drift[2]			15		nV/°C
Gain Error Drift[2]			0.4		ppm/°C
Common-Mode Rejection Ratio[2]	50 Hz tone		−110		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL FILTER RESPONSE[1]					
Group Delay			37/ODR		µs
Settling Time (Latency)	Complete settling		74/ODR		µs
Pass-Band Ripple				±0.005	dB
Pass Band			0.453 × ODR		Hz
−3 dB Bandwidth			0.49 × ODR		Hz
Stop-Band Frequency			0.547 × ODR		Hz
Stop-Band Attenuation		100			dB
REFERENCE INPUT[1]					
V_{REF+} Input Voltage		2.4		$2 \times AV_{DD}$	V
DIGITAL INPUTS (Logic Levels)[1]					
V_{IL}		−0.3		$+0.3 \times V_{DRIVE}$	V
V_{IH}		$0.7 \times V_{DRIVE}$		$V_{DRIVE} + 0.3$	V
Input Leakage Current				±1	µA/pin
Input Capacitance			5		pF
Master Clock Rate				1.024	MHz
Serial Clock Rate				$1/t_8$	Hz
DIGITAL OUTPUTS[1]					
Data Format	Serial 24 bits, twos complement (MSB first)				
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	$V_{DRIVE} - 0.3$			V
POWER REQUIREMENTS[1]					
AV_{DD}	± 5%		2.5		V
DV_{DD}	± 5%		2.5		V
V_{DRIVE}		1.7	2.5	3.6	V
CURRENT SPECIFICATIONS	MCLK = 1.024 MHz				
AD7767 Operational Current	128 kHz output data rate				
AI_{DD}			1.3	1.5	mA
DI_{DD}			3.9	4.8	mA
I_{REF}			0.35	0.425	mA
AD7767-1 Operational Current	64 kHz output data rate				
AI_{DD}			1.3	1.5	mA
DI_{DD}			2.2	2.85	mA
I_{REF}			0.35	0.425	mA
AD7767-2 Operational Current	32 kHz output data rate				
AI_{DD}			1.3	1.5	mA
DI_{DD}			1.37	1.86	mA
I_{REF}			0.35	0.425	mA
Static Current with MCLK Stopped	For all devices				
AI_{DD}			0.9	1	mA
DI_{DD}			1	93	µA
Power-Down Mode Current	For all devices				
AI_{DD}			0.1	6	µA
DI_{DD}			1	93	µA
POWER DISSIPATION	MCLK = 1.024 MHz				
AD7767 Operational Power	128 kHz output data rate		15	18	mW
AD7767-1 Operational Power	64 kHz output data rate		10.5	13	mW
AD7767-2 Operational Power	32 kHz output data rate		8.5	10.5	mW

[1] Specifications are for all devices, AD7767, AD7767-1, and AD7767-2.
[2] See the Terminology section.

TIMING SPECIFICATIONS

AV_{DD} = DV_{DD} = 2.5 V ± 5%, V_{DRIVE} = 1.7 V to 3.6 V, V_{REF} = 5 V, common-mode input = $V_{REF}/2$, T_A = −40°C (T_{MIN}) to +105°C (T_{MAX}), unless otherwise noted.[1]

Table 3.

Parameter	Limit at t_{MIN}, t_{MAX}	Unit	Description
$\overline{DRDY}$ OPERATION			
t_1	510	ns typ	MCLK rising edge to $\overline{DRDY}$ falling edge
t_2[2]	100	ns min	MCLK high pulse width
t_3[2]	900	ns max	MCLK low pulse width
t_4	265	ns typ	MCLK rising edge to $\overline{DRDY}$ rising edge (AD7767)
	128	ns typ	MCLK rising edge to $\overline{DRDY}$ rising edge (AD7767-1)
	71	ns typ	MCLK rising edge to $\overline{DRDY}$ rising edge (AD7767-2)
t_5	294	ns typ	$\overline{DRDY}$ pulse width (AD7767)
	435	ns typ	$\overline{DRDY}$ pulse width (AD7767-1)
	492	ns typ	$\overline{DRDY}$ pulse width (AD7767-2)
t_{READ}[3]	$t_{\overline{DRDY}} - t_5$	ns typ	$\overline{DRDY}$ low period, read data during this period
$t_{\overline{DRDY}}$[3]	$n \times 8 \times t_{MCLK}$	ns typ	$\overline{DRDY}$ period
Read OPERATION			
t_6	0	ns min	$\overline{DRDY}$ falling edge to $\overline{CS}$ setup time
t_7	6	ns max	$\overline{CS}$ falling edge to SDO tristate disabled
t_8	60	ns max	Data access time after SCLK falling edge (V_{DRIVE} = 1.7 V)
	50	ns max	Data access time after SCLK falling edge (V_{DRIVE} = 2.3 V)
	25	ns max	Data access time after SCLK falling edge (V_{DRIVE} = 2.7 V)
	24	ns max	Data access time after SCLK falling edge (V_{DRIVE} = 3.0 V)
t_9	10	ns min	SCLK falling edge to data valid hold time (V_{DRIVE} = 3.6 V)
t_{10}	10	ns min	SCLK high pulse width
t_{11}	10	ns min	SCLK low pulse width
t_{SCLK}	$1/t_8$	sec min	Minimum SCLK period
t_{12}	6	ns max	Bus relinquish time after $\overline{CS}$ rising edge
t_{13}	0	ns min	$\overline{CS}$ rising edge to $\overline{DRDY}$ rising edge
Read OPERATION WITH $\overline{CS}$ LOW			
t_{14}	0	ns min	$\overline{DRDY}$ falling edge to data valid setup time
t_{15}	0	ns max	$\overline{DRDY}$ rising edge to data valid hold time
DAISY-CHAIN OPERATION			
t_{16}	1	ns min	SDI valid to SCLK falling edge setup time
t_{17}	2	ns max	SCLK falling edge to SDI valid hold time
$\overline{SYNC}/\overline{PD}$ OPERATION			
t_{18}	1	ns typ	$\overline{SYNC}/\overline{PD}$ falling edge to MCLK rising edge
t_{19}	20	ns typ	MCLK rising edge to $\overline{DRDY}$ rising edge going into $\overline{SYNC}/\overline{PD}$ mode
t_{20}	1	ns min	$\overline{SYNC}/\overline{PD}$ rising edge to MCLK rising edge
t_{21}	510	ns typ	MCLK rising edge to $\overline{DRDY}$ falling edge coming out of $\overline{SYNC}/\overline{PD}$ mode
$t_{SETTLING}$[3]	(592 × n) + 2	t_{MCLK}	Filter settling time after a reset or power-down

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.7 V.
[2] t_2 and t_3 allow a ~90% to 10% duty cycle to be used for the MCLK input, where the minimum is 10% for the clock high time and 90% for MCLK low time. The maximum MCLK frequency is 1.024 MHz.
[3] n = 1 for AD7767, n = 2 for the AD7767-1, n = 4 for the AD7767-2.

TIMING DIAGRAMS

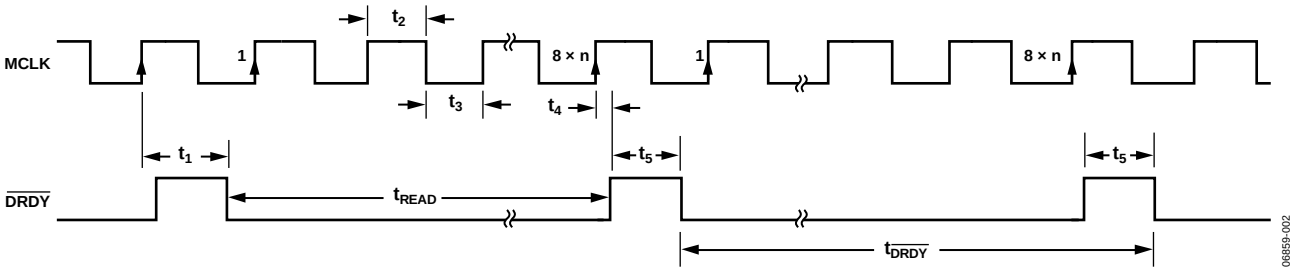


Figure 2. $\overline{DRDY}$ vs. MCLK Timing Diagram, n = 1 for AD7767 (Decimate by 8), n = 2 for AD7767-1 (Decimate by 16), n = 4 for AD7767-2 (Decimate by 32)

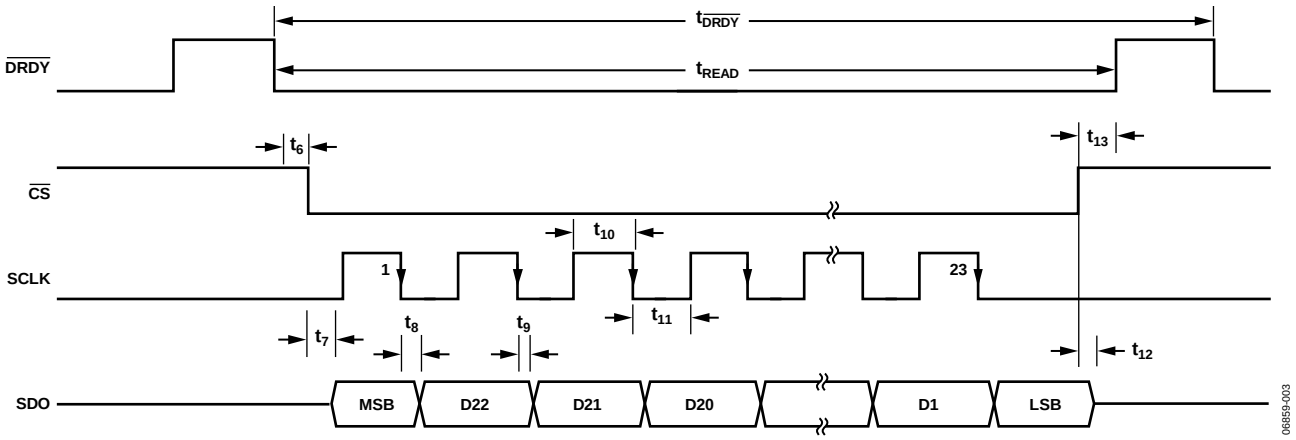


Figure 3. Serial Timing Diagram, Reading Data Using $\overline{CS}$

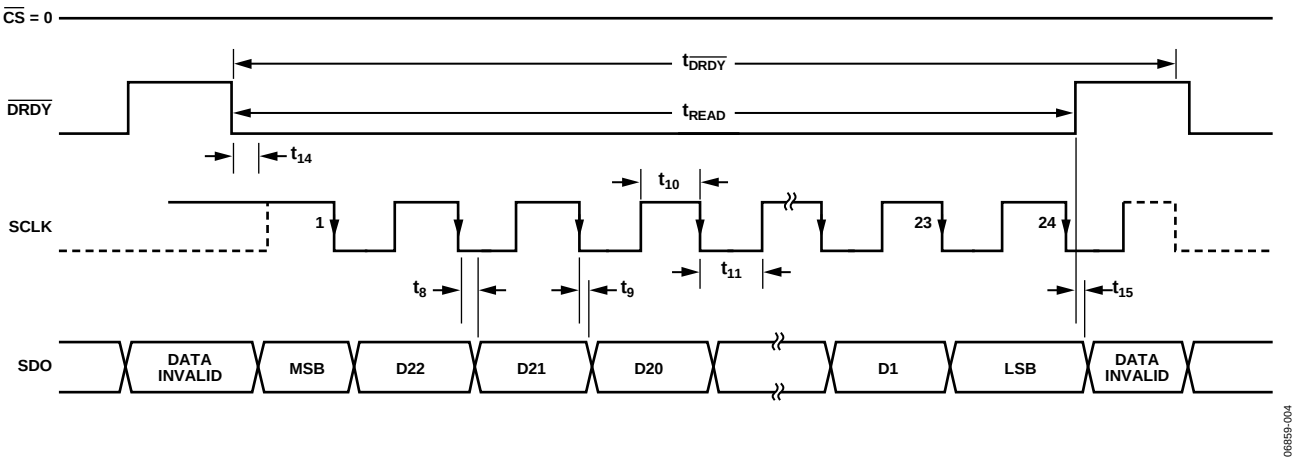


Figure 4. Serial Timing Diagram, Reading Data Setting $\overline{CS}$ Logic Low

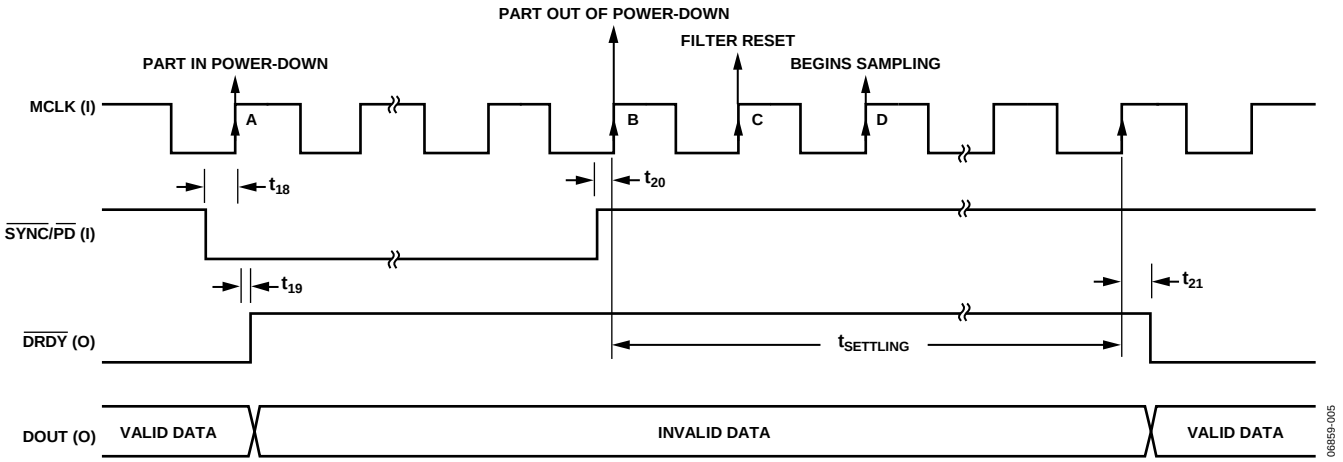


Figure 5. Reset, Synchronization, and Power-Down Timing (For More Information, See the Power-Down, Reset, and Synchronization Section)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +3 V
DV_{DD} to DGND	−0.3 V to +3 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_{REF+} to REFGND	−0.3 V to +7 V
REFGND to AGND	−0.3 V to +0.3 V
V_{DRIVE} to DGND	−0.3 V to +6 V
V_{IN+}, V_{IN-} to AGND	−0.3 V to V_{REF+} + 0.3 V
Digital Inputs to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Outputs to DGND	−0.3 V to V_{DRIVE} + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package	
θ_{JA} Thermal Impedance	150.4°C/W
θ_{JC} Thermal Impedance	27.6°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	1 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

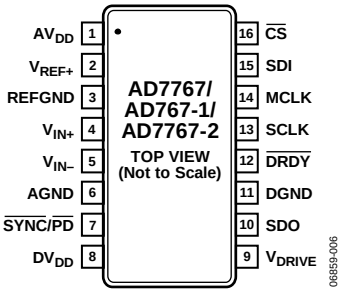


Figure 6. 16-Lead TSSOP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AV_{DD}	+2.5 V Analog Power Supply.
2	V_{REF+}	Reference Input for the AD7767. An external reference must be applied to this input pin. The V_{REF+} input can range from 2.4 V to 5 V. The reference voltage input is independent of the voltage magnitude applied to the AV_{DD} pin.
3	REFGND	Reference Ground. Ground connection for the reference voltage. The input reference voltage (V_{REF+}) should be decoupled to this pin.
4	V_{IN+}	Positive Input of the Differential Analog Input.
5	V_{IN-}	Negative Input of the Differential Analog Input.
6	AGND	Power Supply Ground for Analog Circuitry.
7	$\overline{SYNC}/\overline{PD}$	Synchronization and Power-Down Input Pin. This pin has dual functionality. It can be used to synchronize multiple AD7767 devices and/or to put the AD7767 device into power-down mode. See the Power-Down, Reset, and Synchronization section for further details.
8	DV_{DD}	2.5 V Digital Power Supply Input. In cases where an logic voltage of 2.5 V is used for interfacing (2.5 V applied to V_{DRIVE} pin), the DVDD and V_{DRIVE} pin may be connected to the same voltage supply rail.
9	V_{DRIVE}	Logic Power Supply Input, 1.8 V to 3.6 V. The voltage supplied at this pin determines the operating voltage of the digital logic interface.
10	SDO	Serial Data Output. The conversion result from the AD7767 is output on the SDO pin as a 24-bit, twos complement, MSB first, serial data stream.
11	DGND	Digital Logic Power Supply Ground.
12	$\overline{DRDY}$	Data Ready Output. A falling edge on the $\overline{DRDY}$ signal indicates that a new conversion data result is available in the output register of the AD7767. See the AD7767 Interface section for further details.
13	SCLK	Serial Clock Input. The SCLK input provides the serial clock for all serial data transfers with the AD7767 device. See the AD7767 Interface section for further details.
14	MCLK	Master Clock Input. The AD7767 sampling frequency is equal to the MCLK frequency.
15	SDI	Serial Data Input. This is the daisy-chain input of the AD7767. See the Daisy Chaining section for further details.
16	$\overline{CS}$	Chip Select Input. The $\overline{CS}$ input selects the AD7767 device and acts as an enable on the SDO pin. In cases where $\overline{CS}$ is used, the MSB of the conversion result is clocked onto the SDO line on the $\overline{CS}$ falling edge. The $\overline{CS}$ input allows multiple AD7767 devices to share the same SDO line. This allows the user to select the appropriate device by supplying it with a logic low $\overline{CS}$ signal, which enables the SDO pin of the device concerned. See the AD7767 Interface section for further details.

TYPICAL PERFORMANCE CHARACTERISTICS

AV_{DD} = DV_{DD} = 2.5 V ± 5%, V_{DRIVE} = 1.8 V to 3.6 V, V_{REF} = 5 V, MCLK = 1 MHz, common-mode input = $V_{REF}/2$. T_A = 25°C, unless otherwise noted. All FFTs were generated using 8192 samples using a four-term Blackman-Harris window.

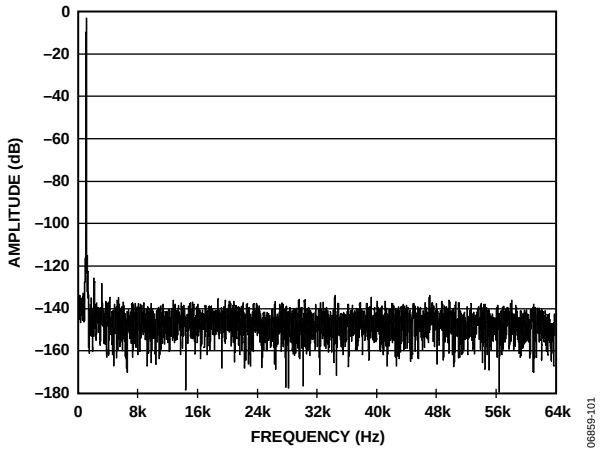


Figure 7. AD7767 FFT, 1 kHz, −0.5 dB Input Tone

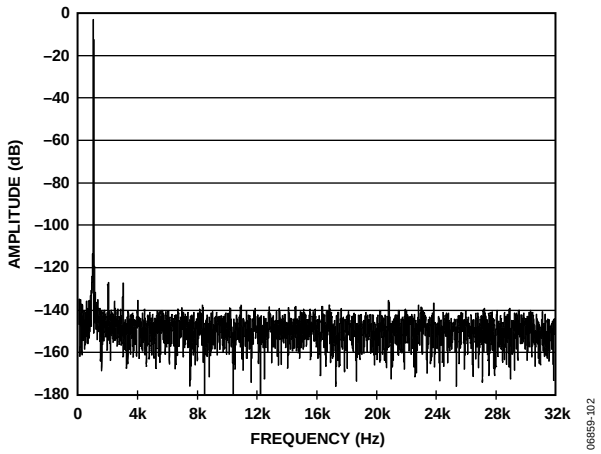


Figure 8. AD7767-1 FFT, 1 kHz, −0.5 dB Input Tone

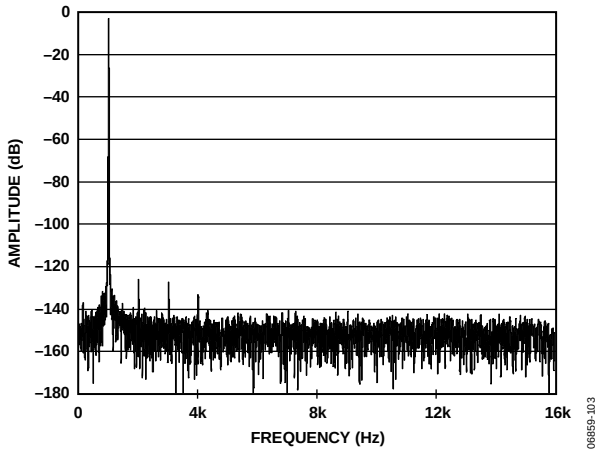


Figure 9. AD7767-2 FFT, 1 kHz, −0.5 dB Input Tone

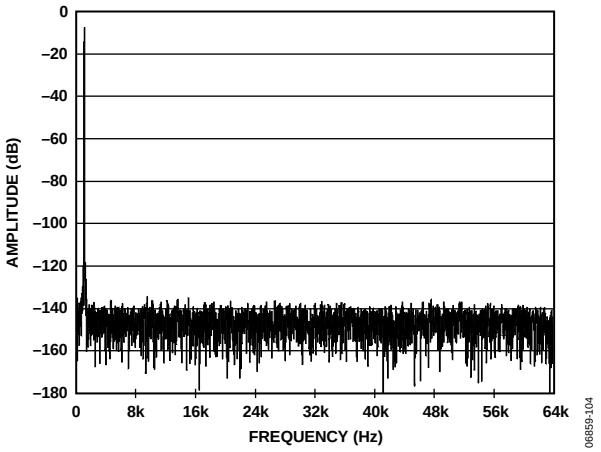


Figure 10. AD7767 FFT, 1 kHz, −6 dB Input Tone

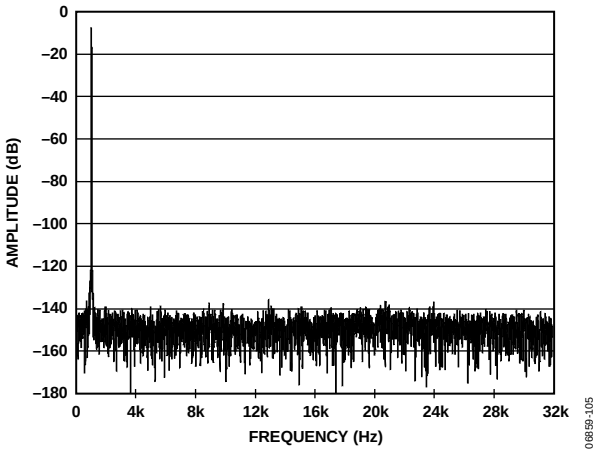


Figure 11. AD7767-1 FFT, 1 kHz, −6 dB Input Tone

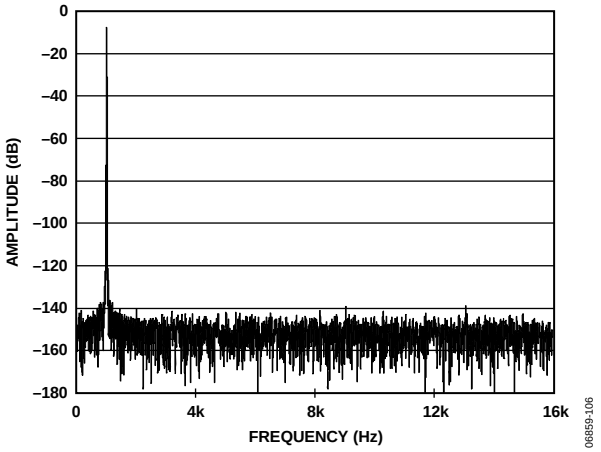


Figure 12. AD7767-2 FFT, 1 kHz, −6 dB Input Tone

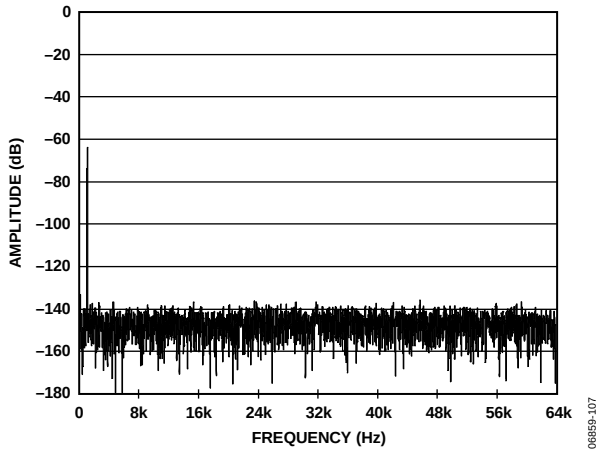


Figure 13. AD7767 FFT, 1 kHz, –60 dB Input Tone

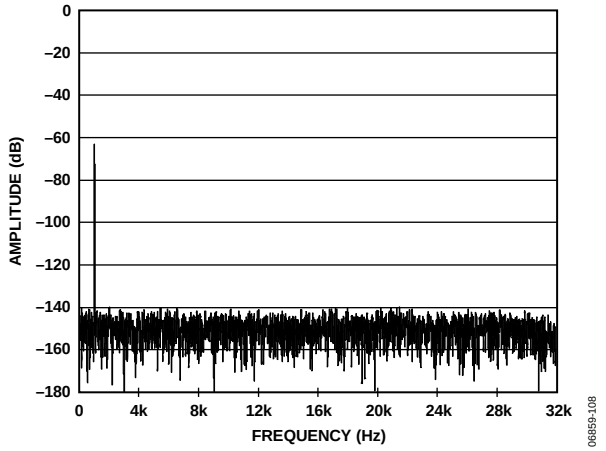


Figure 14. AD7767-1 FFT, 1 kHz, –60 dB Input Tone

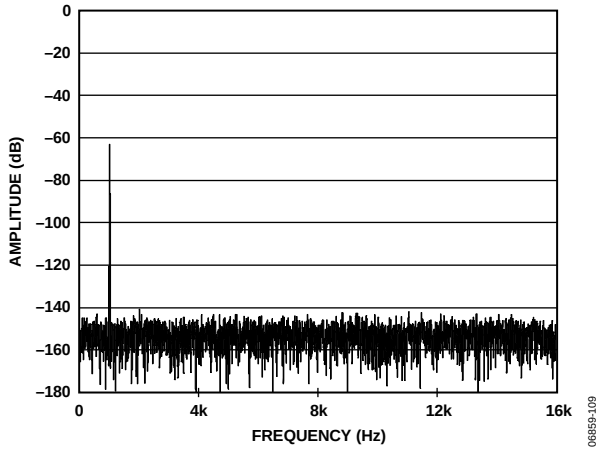


Figure 15. AD7767-2 FFT, 1 kHz, –60 dB Input Tone

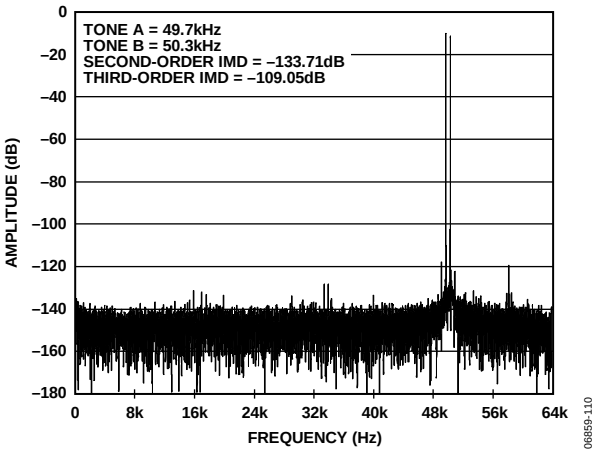


Figure 16. AD7767 IMD FFT, 50 kHz Center Frequency

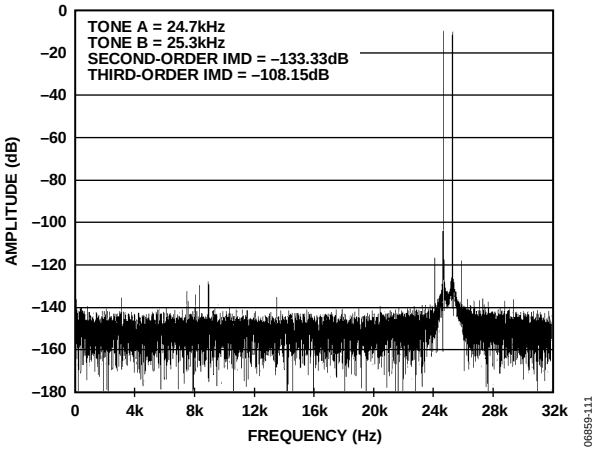


Figure 17. AD7767-1 IMD FFT, 25 kHz Center Frequency

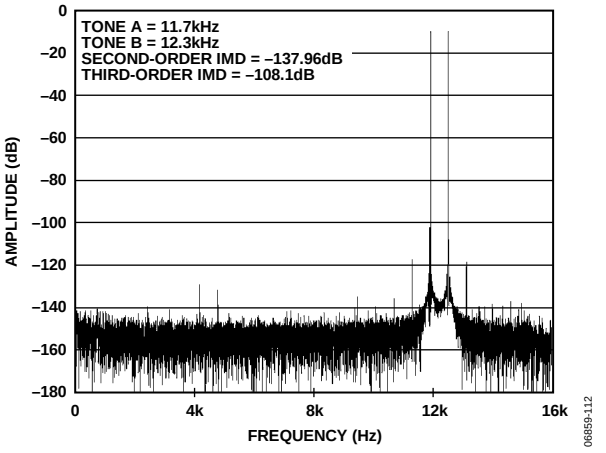


Figure 18. AD7767-2 IMD FFT, 12 kHz Center Frequency

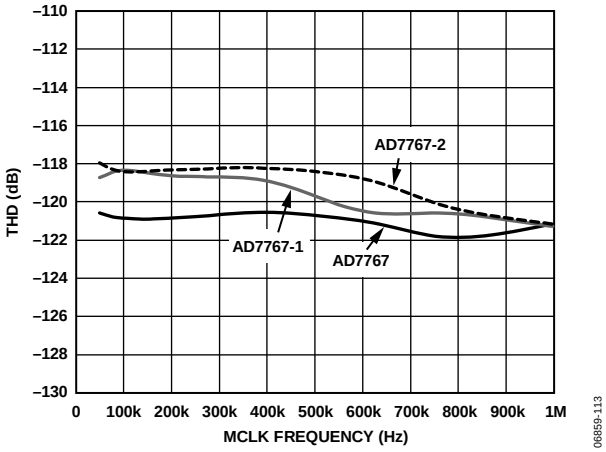


Figure 19. AD7767/AD7767-1/AD7767-2 THD vs. MCLK Frequency

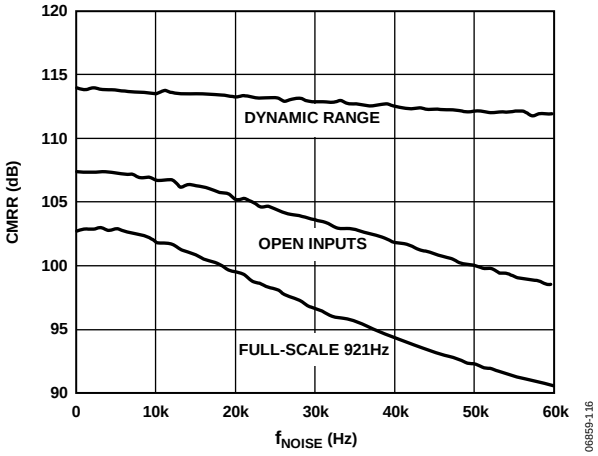


Figure 22. AD7767 CMRR vs. Common-Mode Ripple Frequency (f_{NOISE})

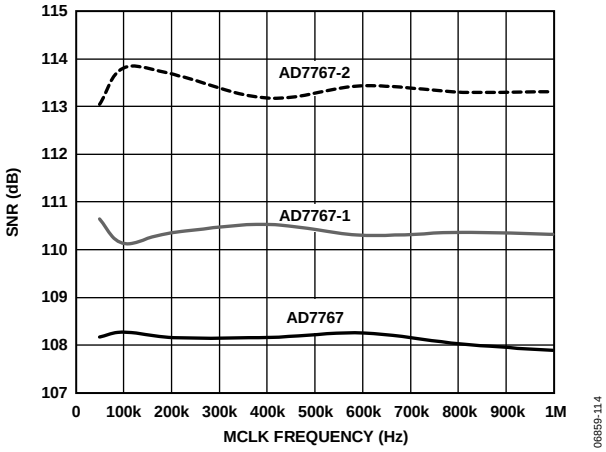


Figure 20. AD7767/AD7767-1/AD7767-2 SNR vs. MCLK Frequency

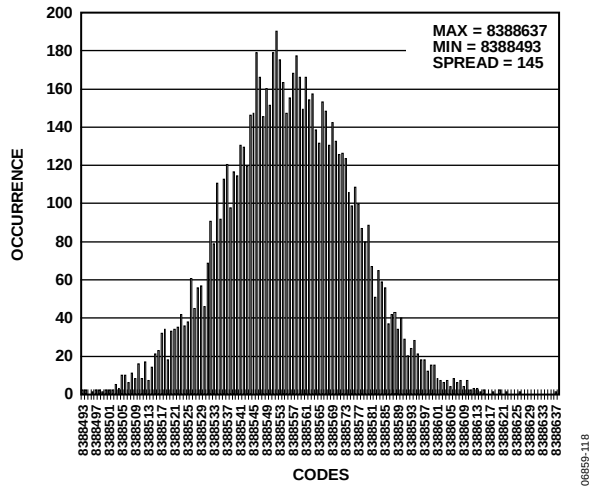


Figure 23. AD7767 24-Bit Histogram

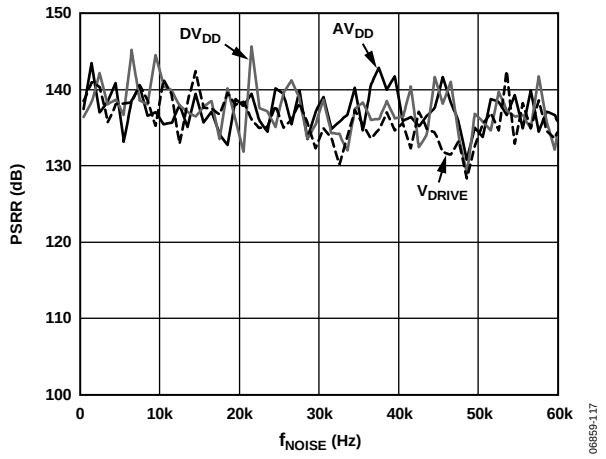


Figure 21. AD7767 Power Supply Sensitivity vs. Supply Ripple Frequency (f_{NOISE}) with Decoupling Capacitors

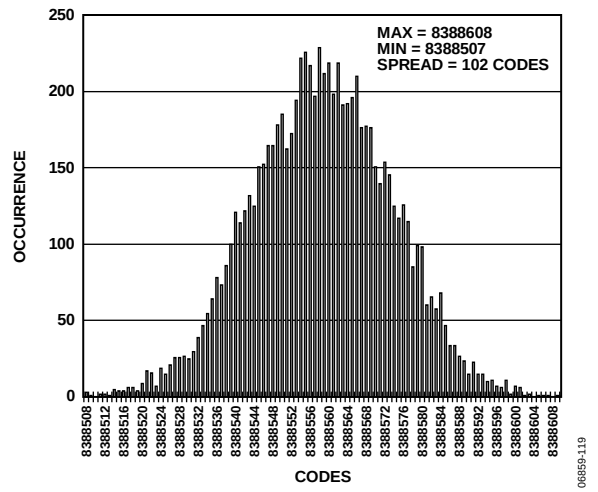


Figure 24. AD7767-1 24-Bit Histogram

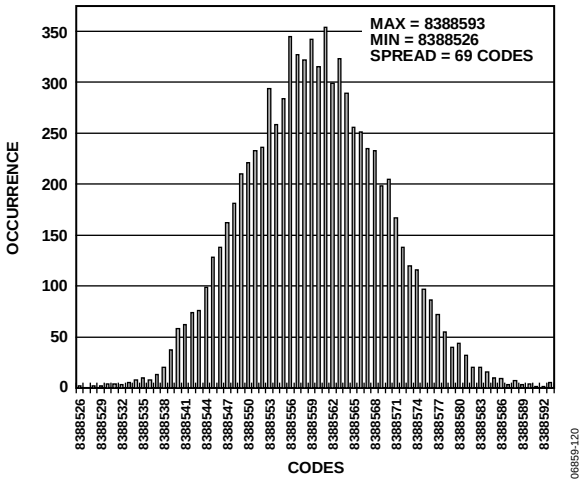


Figure 25. AD7767-2 24-Bit Histogram

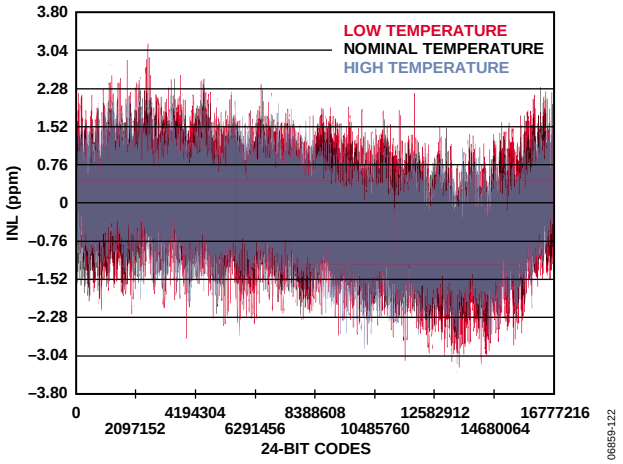


Figure 27. AD7767/AD7767-1/AD7767-2 24-Bit INL

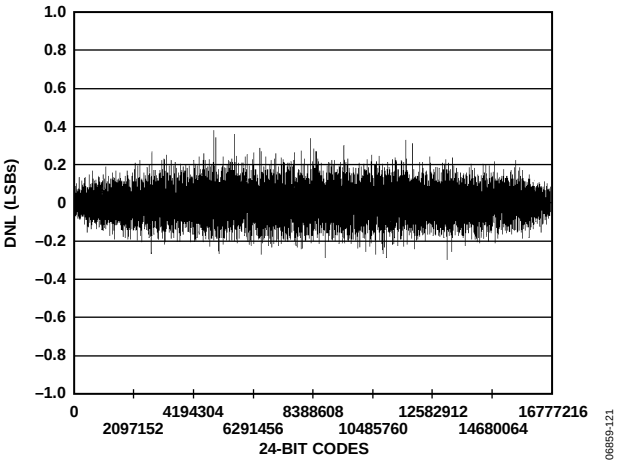


Figure 26. AD7767/AD7767-1/AD7767-2 24-Bit DNL

TERMINOLOGY

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the actual input signal's rms value to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7767, it is defined as

$$THD\,(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second to the sixth harmonics.

Nonharmonic Spurious-Free Dynamic Range (SFDR)
SFDR is the ratio of the rms signal amplitude to the rms value of the peak spurious spectral component, excluding harmonics.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for the dynamic range is expressed in decibels.

Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7767 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used.

In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Zero Error
Zero error is the difference between the ideal midscale input voltage (when both inputs are shorted together) and the actual voltage producing the midscale output code.

Zero Error Drift
Zero error drift is the change in the actual zero error value due to a temperature change of 1°C. It is expressed as a percentage of full scale at room temperature.

Gain Error
The first transition (from 100 … 000 to 100 … 001) should occur ½ LSB above the nominal negative full scale for an analog voltage. The last transition (from 011 … 110 to 011 … 111) should occur 1½ LSB below the nominal full scale for an analog voltage. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition, from the difference between the ideal levels.

Gain Error Drift
Gain error drift is the change in the actual gain error value due to a temperature change of 1°C. It is expressed as a percentage of full scale at room temperature.

Common-Mode Rejection Ratio (CMRR)
CMRR is defined as the ratio of the power in the ADC output at full-scale frequency f to the power of a 100 mV sine wave applied to the common-mode voltage of the V_{IN+} and V_{IN-} inputs at frequency f_S.

$$CMRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where Pf is the power at the frequency f in the ADC output, and Pf_S is the power at the frequency f_S in the ADC output.

THEORY OF OPERATION

The AD7767/AD7767-1/AD7767-2 operate using a fully differential analog input applied to a successive approximation (SAR) core. The output of the oversampled SAR is filtered using a linear-phase digital FIR filter. The fully filtered data is output in a serial format, with the MSB being clocked out first.

AD7767/AD7767-1/AD7767-2 TRANSFER FUNCTION

The conversion results of the AD7767/AD7767-1/AD7767-2 are output in a twos complement, 24-bit serial format. The fully differential inputs V_{IN+} and V_{IN-} are scaled by the AD7767/AD7767-1/AD7767-2 relative to the reference voltage input (V_{REF+}) as shown in Figure 28.

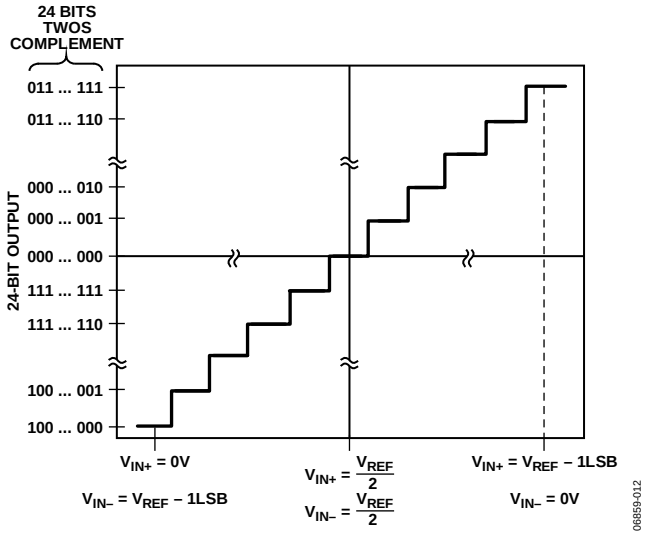


Figure 28. AD7767/AD7767-1/AD7767-2 Transfer Function

CONVERTER OPERATION

Internally, the input waveform applied to the SAR core is converted and an equivalent digital word is output to the digital filter at a rate equal to MCLK. By employing oversampling, the quantization noise of the converter is spread across a wide bandwidth from 0 to f_{MCLK}. This means that the noise energy contained in the signal band of interest is reduced (see Figure 29).

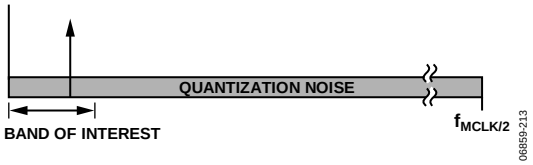


Figure 29. Quantization Noise

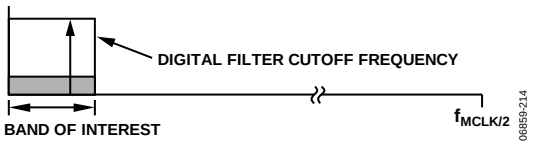


Figure 30. Digital Filter Cutoff Frequency

The digital filtering that follows the converter output acts to remove the out-of-band quantization noise (see Figure 30). This also has the effect of reducing the data rate from f_{MCLK} at the input of the filter to $f_{MCLK}/8$, $f_{MCLK}/16$, or $f_{MCLK}/32$ at the digital output, depending on which model of the device is being used.

The digital filter consists of three separate filter blocks. Figure 31 shows the three constituent blocks of the filter. The order of decimation of the first filter block is set as 2, 4, or 8. The remaining sections each operate with a decimation of 2.

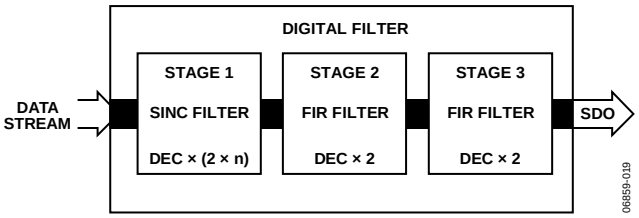


Figure 31. FIR Filter Stages
(n = 1 for AD7767, n = 2 for AD7767-1, n = 4 for AD7767-2)

Table 6 shows the three available models of the AD7767, listing the change in output data rate relative to the order of decimation rate implemented. This brings into focus the trade-off that exists between extra filtering and reduction in bandwidth, whereby using a filter option with a larger decimation rate increases the noise performance while decreasing the usable input bandwidth.

Table 6. AD7767 Models

Model	Decimation Rate	Output Data Rate (ODR)
AD7767	8	128 kHz
AD7767-1	16	64 kHz
AD7767-2	32	32 kHz

Note that the output data rates shown in Table 6 are realized when using the maximum MCLK input frequency of 1.024 MHz. The output data rate scales linearly with the MCLK frequency, as does the digital power dissipated in the device.

The settling time of the filter implemented on the AD7767, AD7767-1, and AD7767-2 is related to the length of the filter employed. The response of the filter in the time domain sets the filter settling time. Table 7 shows the filter settling times of the AD7767/AD7767-1/AD7767-2.

The frequency responses of the digital filters on the AD7767, AD7767-1, and AD7767-2 are shown in Figure 32, Figure 33, and Figure 34, respectively. At the Nyquist frequency (output data rate/2), the digital filter provides 6 dB of attenuation. In each case, the filter provides stop-band attenuation of 100 dB and pass-band ripple of ±0.005 dB.

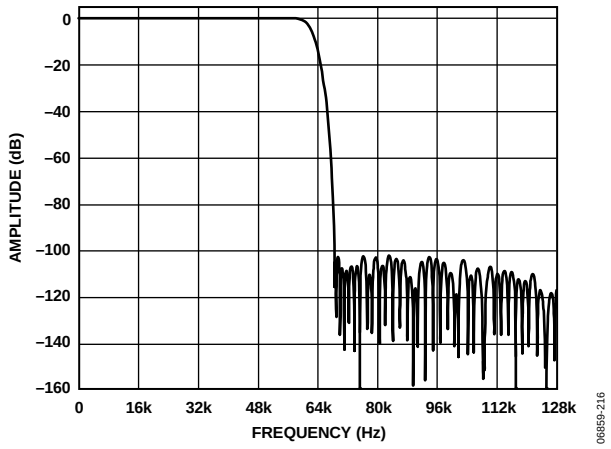


Figure 32. AD7767 Digital Filter Frequency Response

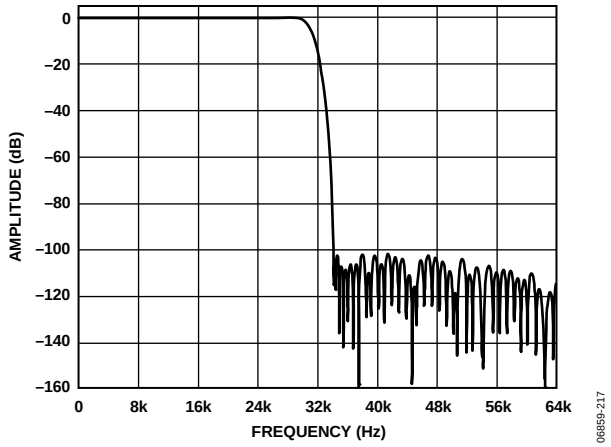


Figure 33. AD7767-1 Digital Filter Frequency Response

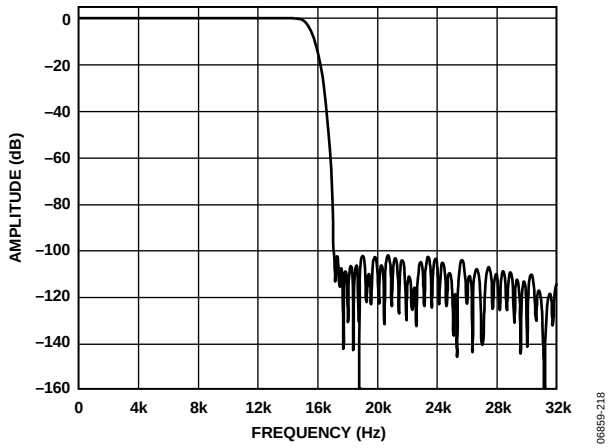


Figure 34. AD7767-2 Digital Filter Frequency Response

ANALOG INPUT STRUCTURE

The AD7767/AD7767-1/AD7767-2 are configured as a differential input structure. A true differential signal is sampled between the analog inputs V_{IN+} and V_{IN-}, Pin 4 and Pin 5, respectively. Using differential inputs provides rejection of signals that are common to both the V_{IN+} and V_{IN-} pins.

Figure 35 shows the equivalent analog input circuit of the AD7767/AD7767-1/AD7767-2. The two diodes on each of the differential inputs provide ESD protection for the analog inputs.

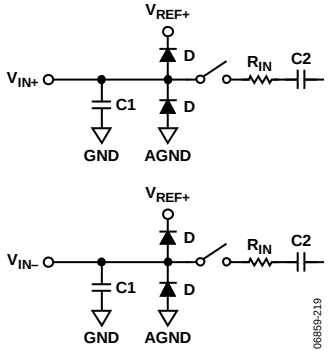


Figure 35. Equivalent Analog Input Structure

Take care to ensure that the analog input signal does not exceed the reference supply voltage (V_{REF+}) by more than 0.3 V, as specified in the Absolute Maximum Ratings section. If the input voltage exceeds this limit, the diodes become forward biased and start to conduct current. The diodes can handle 130 mA maximum.

The impedance of the analog inputs can be modeled as a parallel combination of C1 and the network formed by the series connection of R_{IN}, C1, and C2. The value of C1 is dominated by the pin capacitance. R_{IN} is typically 1.4 kΩ, the lumped component of serial resistors and the R_{ON} of the switches. C2 is typically 22 pF, and its value is dominated by the sampling capacitor.

SUPPLY AND REFERENCE VOLTAGES

The AD7767/AD7767-1/AD7767-2 operate from a 2.5 V supply applied to the DV_{DD} and AV_{DD} pins. The interface is specified to operate between 1.7 V and 3.6 V. The AD7767/AD7767-1/AD7767-2 operate from a reference input in the range of 2.2 V to 2 × AV_{DD} applied to the V_{REF+} pin. The nominal reference supply voltage is 5 V, but a 2.5 V supply can also be used. When using a 5 V reference, the recommended reference devices are the ADR445, ADR435, or ADR425; when using 2.5 V, the ADR441, ADR431, or ADR421 are recommended. The voltage applied to the reference input (V_{REF+}) operates both as a reference supply and as a power supply to the AD7767/AD7767-1/AD7767-2 device. Therefore, when using a 5 V reference input, the full-scale differential input range of the AD7767/AD7767-1/AD7767-2 is 10 V. See the Driving the AD7767 section for details on the maximum input voltage.

AD7767 INTERFACE

The AD7767 provides the user with a flexible serial interface, enabling the user to implement the most desirable interfacing scheme for their application. The AD7767 interface comprises seven different signals. Five of these signals are inputs: MCLK, $\overline{CS}$, $\overline{SYNC}/\overline{PD}$, SCLK, and SDI. The other two signals are outputs: $\overline{DRDY}$ and SDO.

INITIAL POWER-UP

On initial power-up, apply a continuous MCLK signal. It is recommended that the user reset the AD7767 to clear the filters and ensure correct operation. The reset is completed as shown in Figure 5, with all events occurring relative to the rising edge of MCLK. A negative pulse on the $\overline{SYNC}/\overline{PD}$ input initiates the reset, and the $\overline{DRDY}$ output switches to logic high and remains high until valid data is available. Following the power-up of the AD7767 by transitioning the $\overline{SYNC}/\overline{PD}$ pin to logic high, a settling time is required before valid data is output by the device. This settling time, $t_{SETTLING}$, is a function of the MCLK frequency and the decimation rate. Table 7 lists the settling time of each AD7767 model and should be referenced when reviewing Figure 5.

Table 7. Filter Settling Time After $\overline{SYNC}/\overline{PD}$

Model	Decimation Rate	$t_{SETTLING}$[1]
AD7767	8	$(594 \times t_{MCLK}) + t_{21}$
AD7767-1	16	$(1186 \times t_{MCLK}) + t_{21}$
AD7767-2	32	$(2370 \times t_{MCLK}) + t_{21}$

[1] $t_{SETTLING}$ is measured from the first MCLK rising edge after the rising edge of $\overline{SYNC}/\overline{PD}$ to the falling edge of $\overline{DRDY}$.

READING DATA

The AD7767 outputs its data conversion results in an MSB-first, twos complement, 24-bit format on the serial data output pin (SDO). MCLK is the master clock, which controls all the AD7767 conversions. The SCLK is the serial clock input for the device. All data transfers take place with respect to the SCLK signal.

The $\overline{DRDY}$ line is used as a status signal to indicate when the data is available to be read from the AD7767. The falling edge of $\overline{DRDY}$ indicates that a new data-word is available in the output register of the device. $\overline{DRDY}$ stays low during the period that output data is permitted to be read from the SDO pin. The $\overline{DRDY}$ signal returns to logic high to indicate when not to read from the device. Ensure that a data read is not attempted during this period while the output register is being updated.

The AD7767 offers the option of using a chip select input signal ($\overline{CS}$) in its data read cycle. The $\overline{CS}$ signal is a gate for the SDO pin and allows many AD7767 devices to share the same serial bus. It acts as an instruction signal to each of these devices indicating permission to use the bus. When $\overline{CS}$ is logic high, the SDO line of the AD7767 is tristated.

There are two distinct patterns that can be initiated to read data from the AD7767 device: a pattern for when the $\overline{CS}$ falling edge occurs after the $\overline{DRDY}$ falling edge and a pattern for when the $\overline{CS}$ falling edge occurs before the $\overline{DRDY}$ falling edge (when $\overline{CS}$ is set to logic low).

When the $\overline{CS}$ falling edge occurs after the $\overline{DRDY}$ falling edge, the MSB of the conversion result is available on the SDO line on the $\overline{CS}$ falling edge. The remaining bits of the conversion result (MSB − 1, MSB − 2, and so on) are clocked onto the SDO line by the falling edges of SCLK that follow the $\overline{CS}$ falling edge. Figure 3 details this interfacing scheme.

When $\overline{CS}$ is tied low, the AD7767 serial interface can operate in 3-wire mode as shown in Figure 4. In this case, the MSB of the conversion result is available on the SDO line on the falling edge of $\overline{DRDY}$. The remaining bits of the data conversion result (MSB − 1, MSB − 2, and so on) are clocked onto the SDO line by the subsequent SCLK falling edges.

POWER-DOWN, RESET, AND SYNCHRONIZATION

The AD7767 $\overline{SYNC}/\overline{PD}$ pin allows the user to synchronize multiple AD7767 devices. This pin also allows the user to reset and power down the AD7767 device. These features are implemented relative to the rising edges of MCLK and are shown in Figure 5, marked as A, B, C, and D.

To power down, reset, or synchronize a device, the AD7767 $\overline{SYNC}/\overline{PD}$ pin should be taken low. On the first rising edge of MCLK, the AD7767 is powered down. The $\overline{DRDY}$ pin transitions to logic high, indicating that the data in the output register is no longer valid. The status of the $\overline{SYNC}/\overline{PD}$ pin is checked on each subsequent rising edge of MCLK. On the first rising edge of MCLK after the $\overline{SYNC}/\overline{PD}$ pin is taken high, the AD7767 is taken out of power-down. On the next rising edge, the filter of the AD7767 is reset. On the following rising edge, the first new sample is taken.

A settling time, $t_{SETTLING}$, from the filter reset must elapse before valid data is output by the device (see Table 7). The $\overline{DRDY}$ output goes logic low after $t_{SETTLING}$ to indicate when valid data is available on SDO for readback.

DAISY CHAINING

Daisy chaining devices allows numerous devices to use the same digital interface lines by cascading the outputs of multiple ADCs on a single data line. This feature is especially useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register where data is clocked on the falling edge of SCLK.

The block diagram in Figure 36 shows how devices must be connected to achieve daisy-chain functionality. The scheme shown operates by passing the output data of the SDO pin of an AD7767 device to the SDI input of the next AD7767 device in the chain. The data then continues through the chain until it is clocked onto the SDO pin of the first device in the chain.

READING DATA IN DAISY-CHAIN MODE

An example of a daisy chain of four AD7767 devices is shown in Figure 36 and Figure 37. In the case illustrated in Figure 36, the output of the AD7767 labeled A is the output of the full daisy chain. The last device in the chain (the AD7767 labeled D) has its serial data input (SDI) pin connected to ground. All the devices in the chain must use common MCLK, SCLK, $\overline{CS}$, and $\overline{SYNC}/\overline{PD}$ signals.

To enable the daisy-chain conversion process, apply a common $\overline{SYNC}/\overline{PD}$ pulse to all devices, synchronizing all the devices in the chain (see the Power-Down, Reset, and Synchronization section).

After applying a $\overline{SYNC}/\overline{PD}$ pulse to all the devices, there is a delay (as listed in Table 7) before valid conversion data appears at the output of the chain of devices. As shown in Figure 37, the first conversion result is output from the AD7767 device labeled A. This 24-bit conversion result is followed by the conversion results from the devices labeled B, C, and D, respectively, with all conversion results output in an MSB-first sequence. The stream of conversion results is clocked through each device in the chain and is eventually clocked onto the SDO pin of the AD7767 device labeled A. The conversion results of all the devices in the chain must be clocked onto the SDO pin of the final device in the chain while its $\overline{DRDY}$ signal is active low.

This is illustrated in the examples shown (Figure 37 and Figure 38), where the conversion results from the devices labeled A, B, C, and D are clocked onto SDO (A) during the time between the falling edge of $\overline{DRDY}$ (A) and the rising edge of $\overline{DRDY}$ (A).

CHOOSING THE SCLK FREQUENCY

As shown in Figure 37, the number of SCLK falling edges that occur during the period when $\overline{DRDY}$ (A) is active low must match the number of devices in the chain multiplied by 24 (the number of bits that must be clocked through onto SDO (A) for each device).

The period of SCLK (t_{SCLK}) required for a known daisy-chain length using a known common MCLK frequency must, therefore, be established in advance. Note that the maximum SCLK frequency is governed by t_8 and is specified in the Timing Specifications table for different V_{DRIVE} voltages.

In the case where $\overline{CS}$ is tied logic low,

$$t_{SCLK} \leq \left[\frac{t_{READ}}{24 \times K} \right] \quad (1)$$

where:
K is the number of AD7767 devices in the chain.
t_{SCLK} is the period of the SCLK.
t_{READ} equals $t_{\overline{DRDY}} - t_5$.

In the case where $\overline{CS}$ is used in the daisy-chain interface,

$$t_{SCLK} \leq \left[\frac{(t_{READ}) - (t_6 + t_7 + t_{13})}{24 \times K} \right] \quad (2)$$

where:
K is the number of AD7767 devices in the chain.
t_{SCLK} is the period of the SCLK.
t_{READ} equals $t_{\overline{DRDY}} - t_5$.

Note that the maximum value of SCLK is governed by t_8 and is specified in the Timing Specifications table for different V_{DRIVE} voltages.

DAISY-CHAIN MODE CONFIGURATION AND TIMING DIAGRAMS

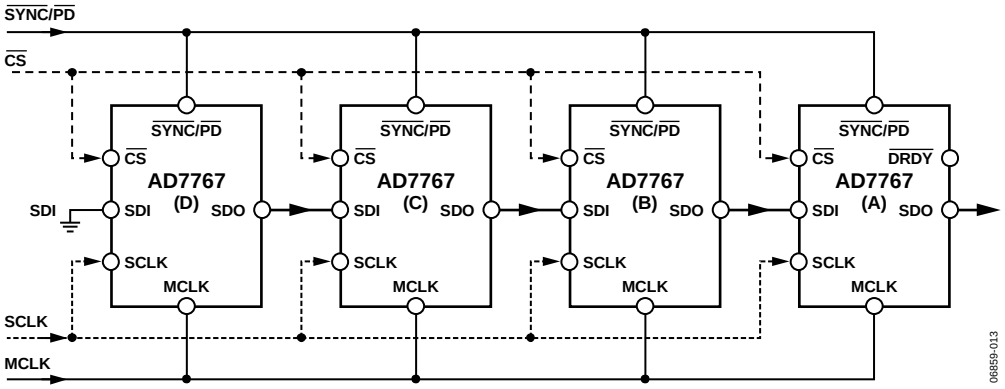


Figure 36. Daisy-Chain Configuration with Four AD7767 Devices

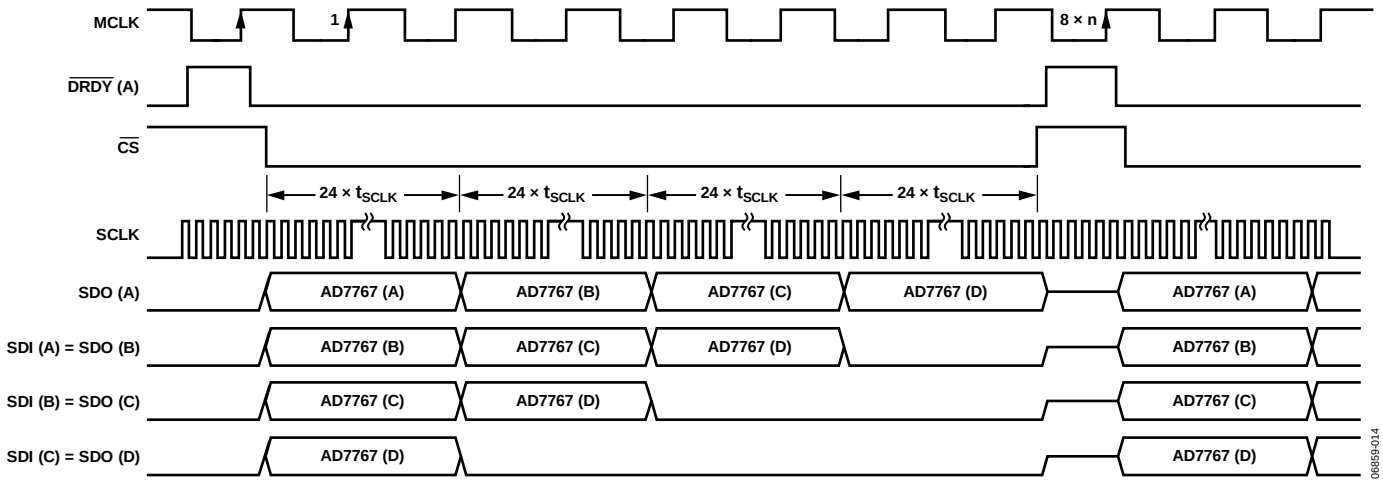


Figure 37. Daisy-Chain Timing Diagram (n = 1 for AD7767, n = 2 for AD7767-1, n = 4 for AD7767-2) When Driving the AD7767

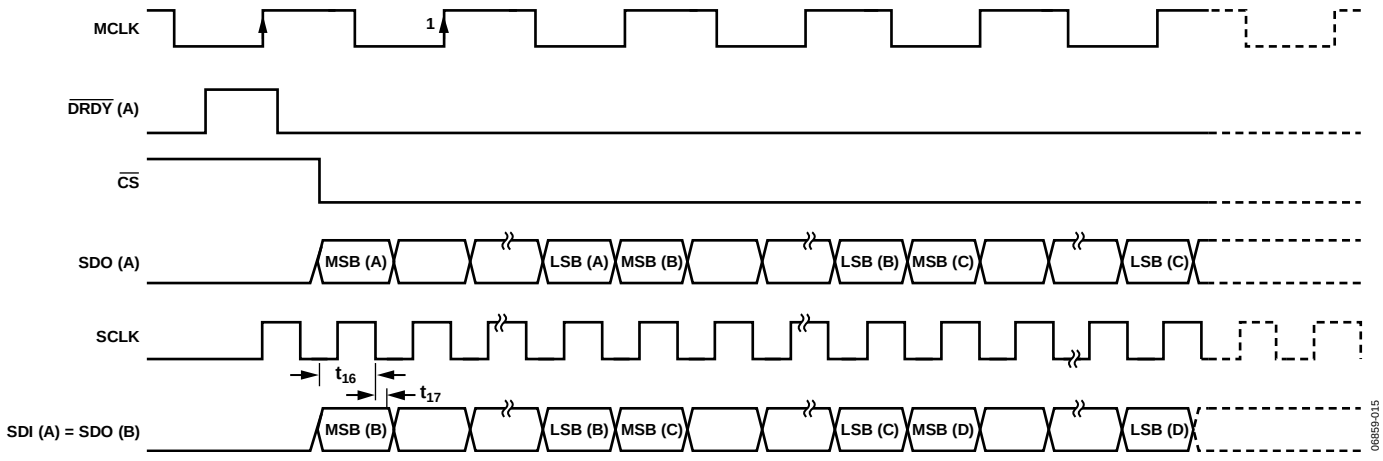


Figure 38. Daisy-Chain SDI Setup and Hold Timing

DRIVING THE AD7767

The AD7767 must be driven with fully differential inputs. The common-mode voltage of the differential inputs to the AD7767 device and therefore the limits on the differential inputs are set by the reference voltage (V_{REF}) applied to the device. The common-mode voltage of the AD7767 is $V_{REF}/2$. When the AD7767 V_{REF+} pin has a 5 V supply (using ADR445, ADR435, or ADR425), the common mode is at 2.5 V, meaning that the maximum inputs that can be applied on the AD7767 differential inputs are a 5 V p-p input around 2.5 V.

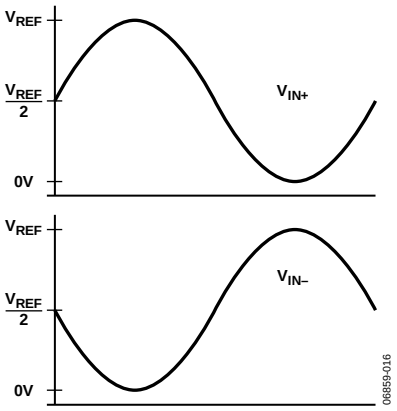


Figure 39. Maximum Differential Inputs to the AD7767

An analog voltage of 2.5 V supplies the AD7767 AV_{DD} pin. However, the AD7767 allows the user to apply a reference voltage of up to 5 V. This provides the user with an increased full-scale range, offering the user the option of using the AD7767 with a greater LSB voltage. Figure 39 shows the maximum inputs to the AD7767.

DIFFERENTIAL SIGNAL SOURCE

An example of recommended driving circuitry that can be used in conjunction with the AD7767/AD7767-1/AD7767-2 is shown in Figure 40. Figure 40 shows how the ADA4841-1 device can be used to drive an input to the AD7767/AD7767-1/AD7767-2 from a differential source. Each of the differential paths is driven by an ADA4841-1 device.

SINGLE-ENDED SIGNAL SOURCE

For applications using a single-ended analog signal, either bipolar or unipolar, the ADA4941-1 single-ended-to-differential driver creates a fully differential input to the AD7767/AD7767-1/AD7767-2. The schematic is shown in Figure 41.

R1 and R2 set the attenuation ratio between the input range and the ADC range (V_{REF}). R1, R2, and C_F are chosen depending on the desired input resistance, signal bandwidth, antialiasing, and noise contribution. The ratio of R2 to R1 should be equal to the ratio of REF to the peak-to-peak input voltage. For example, for the ±10 V range with a 4 kΩ impedance, R2 = 1 kΩ and R1 = 4 kΩ.

R3 and R4 set the common mode on the IN– input, and R5 and R6 set the common mode on the IN+ input of the ADC. The common mode, which is equal to the voltage present at $V_{OFFSET1}$, should be close to $V_{REF}/2$. The voltage present should roughly be set to the ratio of $V_{OFFSET1}$ to 1 + R2/R1.

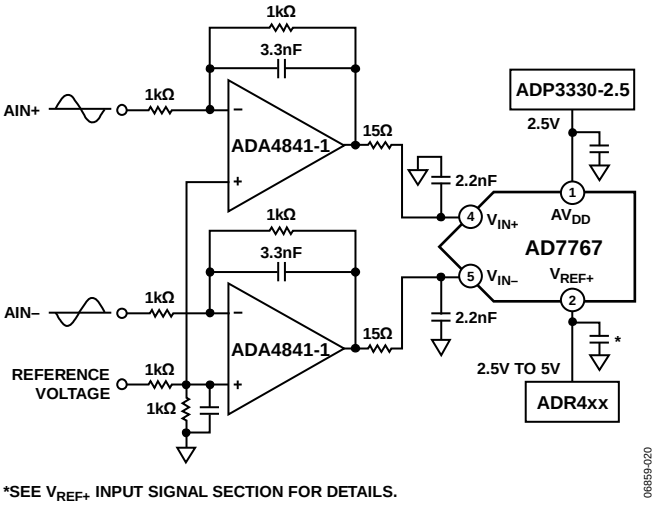


Figure 40. Driving the AD7767 from a Fully Differential Source

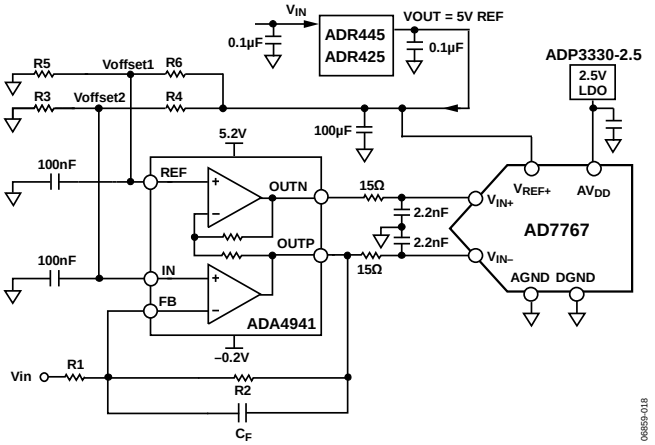


Figure 41. Driving the AD7767 from a Single-Ended Source

Table 8. Resistor Values Required When Using the Differential to Single-Ended Circuit with ADA4941 (See Figure 41)

V_{IN} (V)	$V_{OFFSET1}$ (V)	$V_{OFFSET2}$ (V)	OUT+ (V)	OUT– (V)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	R3 = R5 = R6 (kΩ)
+20, –20	2.5	2.203	–0.01, +4.96	5.01, 0.04	8.06	1	12.7	10
+10, –10	2.5	2.000	0.01, 4.99	4.99, 0.01	4.02	1	15	10
+5, –5	2.5	1.667	0.00, 5.00	5.00, 0.00	2	1	20	10

ANTIALIASING

The AD7767/AD7767-1/AD7767-2 sample the analog input at a maximum rate of 1.024 MHz. The on-board digital filter provides up to 100 dB attenuation for any possible aliasing frequency in the range from the beginning of the filter stop band (0.547 × ODR) to where the image of the digital filter pass band occurs. This occurs at MCLK minus the filter stop band (MCLK − 0.547 × ODR), as shown in Figure 42.

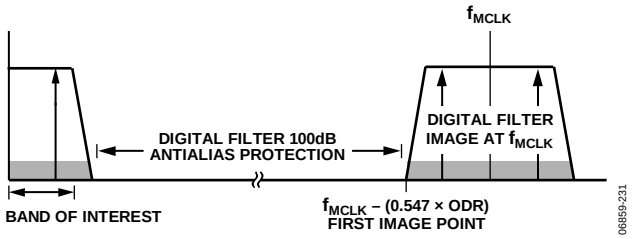


Figure 42. AD7767/AD7767-1/AD7767 Spectrum

Table 9 shows the attenuation achieved by various orders of front-end antialias filters prior to the signal entering the AD7767/AD7767-1/AD7767-2 at the image of the digital filter stop band, which is 1.024 MHz − 0.547 × ODR.

Table 9. Antialias Filter Order, Attenuation at at First Image Point

Model	Filter Order	Attenuation at 1.024 MHz – 0.547 × ODR
AD7767	First	27 dB
	Second	50 dB
	Third	70 dB
AD7767-1	First	33 dB
	Second	62 dB
	Third	89 dB
AD7767-2	First	38 dB
	Second	74 dB
	Third	110 dB

The AD7764 and AD7765 Σ-Δ devices are available to customers that require extra antialias protection. These devices sample the signal internally at a rate of 20 MHz to achieve up to a maximum of 156 kHz or 312 kHz output data rate. This means that the first alias point of these devices when run at the maximum speeds is 19.921 MHz and 19.843 MHz, respectively.

POWER DISSIPATION

The AD7767/AD7767-1/AD7767-2 offer exceptional performance at ultralow power. Figure 43, Figure 44, and Figure 45 show how the current consumption of the AD7767/AD7767-1/AD7767-2 scales with the MCLK frequency applied to the device. Both the digital and analog currents scale as the MCLK frequency is reduced. The actual throughput equals the MCLK frequency applied divided by the decimation rate employed by the device in use. For instance, operating the AD7767 device with an MCLK of 800 kHz results in an output data rate of 100 kHz due to the decimate-by-8 filtering.

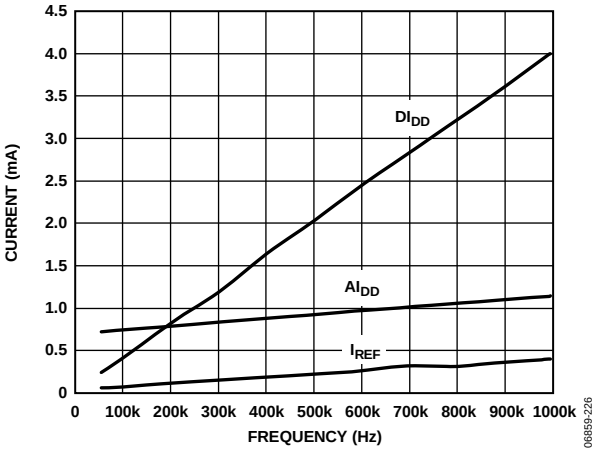


Figure 43. AD7767 Current vs. MCLK Frequency

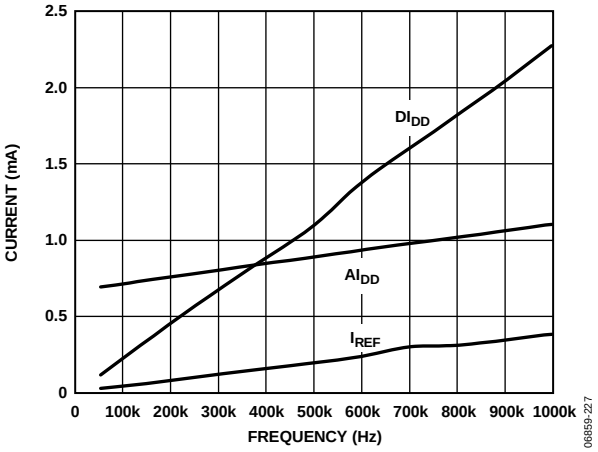


Figure 44. AD7767-1 Current vs. MCLK Frequency

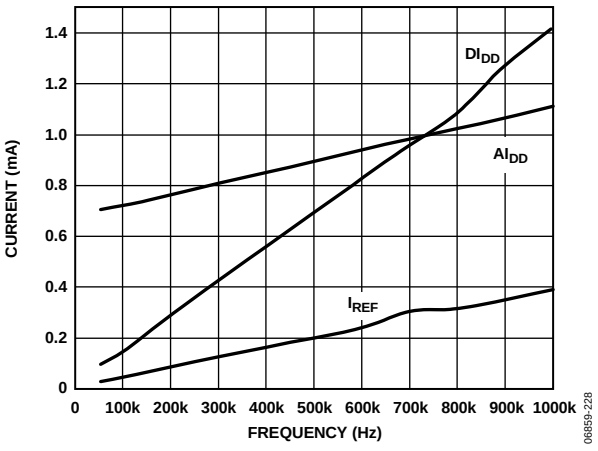


Figure 45. AD7767-2 Current vs. MCLK Frequency

V_{REF+} INPUT SIGNAL

The AD7767/AD7767-1/AD7767-2 V_{REF+} pin is supplied with a voltage in the range of 2.4 V to 2 × AV_{DD} (nominally 5 V). It is recommended that the V_{REF+} input be generated by a low noise voltage reference. Examples of such references are the ADR445, ADR435, ADR425 (5 V output), and ADR421 (2.5 V output). Typical reference supply circuits are shown in Figure 46.

The reference voltage input pin (V_{REF+}) also acts as a power supply to the AD7767/AD7767-1/AD7767-2 device. For a 5 V V_{REF+} input, a full-scale input of 5 V on both V_{IN+} and V_{IN-} can be applied while voltage supplies to pins AV_{DD} remain at 2.5 V. This configuration reduces the number of different supplies required.

The output of the low noise voltage reference does not require a buffer; however, decoupling the output of the low noise reference is important. Place a 0.1 µF capacitor at the output of the voltage reference devices (ADR445, ADR435, ADR425, and ADR421) and follow the decoupling advice provided for the reference device chosen.

As mentioned, the nominal supply to the V_{REF+} pin is 5 V to achieve the full dynamic range available. When a 2.5 V V_{REF+} input is used (that is, in low power applications), the signal-to-noise ratio and dynamic range figures (generated using a 5 V V_{REF+} input) quoted in the Specifications section decrease by 6 dB, a direct result of halving the available input range.

The AD7767/AD7767-1/AD7767-2 device requires a 100 µF capacitor to ground, which acts as a decoupling capacitor and as a reservoir of charge for the V_{REF+} pin. Place this capacitor as close to the AD7767/AD7767-1/AD7767-2 device as possible. Reducing the value of this capacitor (C40 in Figure 46) to 10 µF typically degrades noise performance by 1 dB. C40 can be an electrolytic or tantalum capacitor.

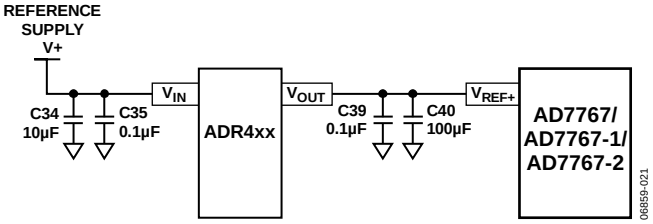


Figure 46. AD7767/AD7767-1/AD7767-2 Reference Input Configuration

MULTIPLEXING ANALOG INPUT CHANNELS

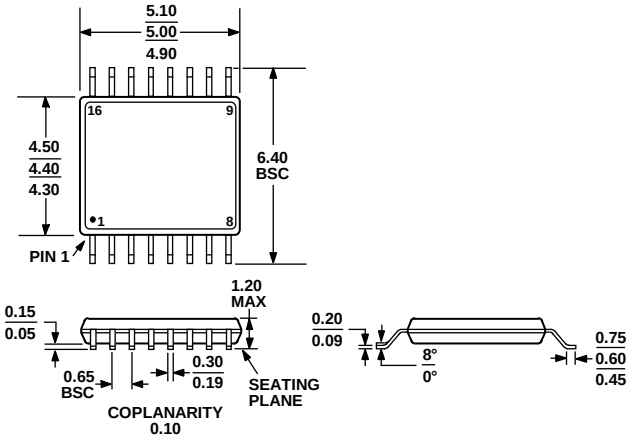
The AD7767/AD7767-1/AD7767-2 can be used with a multiplexer configuration. As per any converter that uses a digital filtering block, the maximum switching rate or the output data rate per channel is a function of the digital filter settling time.

A user multiplexing the analog inputs to a converter that employs a digital filter must wait the full digital filter settling time before a valid conversion result can be achieved; after this settling time, the channel can be switched. Then, the full settling time must again be observed before a valid conversion result is available and the input is switched once more.

The AD7767 filter settling time equals 74 divided by the output data rate in use. The maximum switching frequency in a multiplexed application is, therefore, 1/(74/ODR), where the output data rate (ODR) is a function of the applied MCLK frequency and the decimation rate employed by the device in question. For example, applying a 1.024 MHz MCLK frequency to the AD7767 results in a maximum output data rate of 128 kHz, which in turn allows a 1.729 kHz multiplexer switching rate.

The AD7767-1 and the AD7767-2 employ digital filters with longer settling time to achieve greater precision; thus, the maximum switching frequency for these devices is 864 Hz and 432 Hz, respectively.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 47. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7767BRUZ	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7767BRUZ-RL7	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7767BRUZ-1	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7767BRUZ-1-RL7	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7767BRUZ-2	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7767BRUZ-2-RL7	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
EVAL-AD7767EDZ		Evaluation Board	
EVAL-AD7767-1EDZ		Evaluation Board	
EVAL-AD7767-2EDZ		Evaluation Board	
EVAL-CED1Z		Converter Evaluation and Development Board	

[1] Z = RoHS Compliant Part.

NOTES

D06859-0-5/10(C)