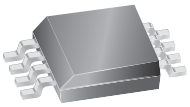
Dual Channel Hall Effect Direction Detection Sensor IC

Features and Benefits

- Precisely aligned dual Hall elements
- Tightly matched magnetic switchpoints
- Speed and direction outputs
- Individual Hall element outputs (L package)
- Fast power-on time
- Output short circuit protection
- Operation from an unregulated power supply
- Wide operating temperature range
- Wide operating voltage range
- Integrated EMC-ESD protection

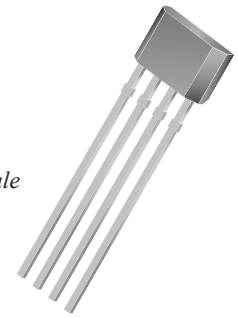
Packages

8-pin SOIC (suffix L)



Not to scale

4-pin SIP (suffix K)



Description

The A3423 is a dual-channel Hall-effect sensor IC ideal for use in speed and direction sensing applications incorporating encoder ring-magnet targets. The A3423 provides various output signals that indicate speed and direction of target rotation. The Hall elements are both photolithographically aligned to better than 1 µm. Maintaining accurate displacement between the two active Hall elements eliminates the major manufacturing hurdle encountered in fine-pitch detection applications. The A3423 is a highly sensitive, temperature-stable magnetic device ideal for use in harsh automotive and industrial environments.

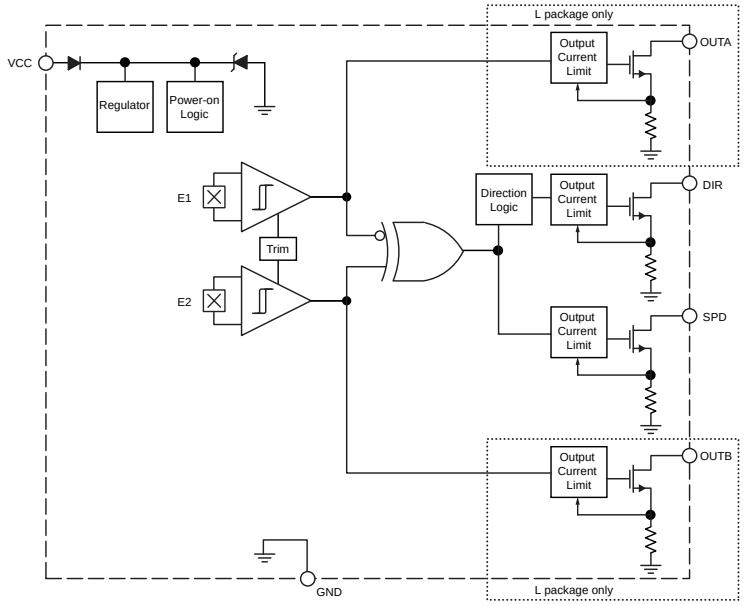
The Hall elements of the A3423 are spaced 1.63 mm apart, which provides excellent speed and direction information for small-geometry targets. Extremely low-drift amplifiers guarantee symmetry between the switches to maintain signal quadrature. An on-chip regulator allows the use of this device over a wide operating voltage range of 3.8 to 24 V.

End-of-line trimming of the Hall element switchpoints provides tight matching capability. The continuous-time nature of the Hall elements delivers a fast start-up of the device and low noise.

The A3423 has integrated protection against transients on the supply and output pins and short-circuit protection on all outputs.

The A3423 is available in a 4-pin SIP and a plastic 8-pin SOIC surface mount package (the SOIC version is currently in development). Both packages are lead (Pb) free, with 100% matte tin leadframe plating.

Functional Block Diagram



Selection Guide

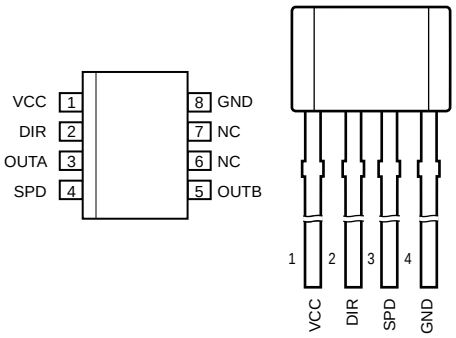
Part Number	Package	Packing[1]	T_A (°C)
A3423EK-T	4-pin through hole SIP	Bulk bag, 500 pieces/bag	–40 to 85
A3423ELTR-T	8-pin surface mount SOIC[2]	Tape and reel, 3000 pieces/reel	
A3423LK-T	4-pin through hole SIP	Bulk bag, 500 pieces/bag	–40 to 150
A3423LLTR-T	8-pin surface mount SOIC[2]	Tape and reel, 3000 pieces/reel	

[1]Contact Allegro for additional packing options.
[2]SOIC package currently in development.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}	–40°C to 150°C	30	V
Reverse Battery Voltage	V_{RB}		–30	V
Output Off Voltage	V_{OUT}		V_{CC}	V
Output Sink Current	$I_{OUT(SINK)}$		30	mA
Magnetic Flux Density	B		Unlimited	G
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
		Range L	–40 to 150	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Maximum Junction Temperature	T_J(max)		165	°C

Pin-out Diagrams



L Package K Package

Terminal List Table

Number		Name	Description
K	L		
1	1	VCC	Input power supply; tie to GND with bypass capacitor
2	2	DIR	Output signal indicating direction of target movement
–	3	OUTA	Analog output indicating B at E1 Hall element
3	4	SPD	Output signal indicating speed of target movement
–	5	OUTB	Analog output indicating B at E2 Hall element
–	6, 7	NC	No connection
4	8	GND	Ground connection

OPERATING CHARACTERISTICS valid at T_A = –40°C to 150°C, $T_J \le T_J$ (max), through full operating air gap range, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Electrical Characteristics						
Supply Voltage	V_{CC}	Operating, $T_J \le 165$°C	3.8	–	24	V
Output Leakage Current	I_{OFF}	All outputs $V_{OUT} \le V_{CC}$(max)	–	<1	10	µA
Undervoltage Lockout	$V_{CC(UV)}$		–	–	3.7	V
Undervoltage Hysteresis	$V_{CC(hys)}$	Lockout ($V_{CC(UV)}$) – Shutdown	–	0.4	–	V
Output Rise Time	t_r	C_{LOAD} = 20 pF, R_{LOAD} = 1 kΩ	–	200	–	ns
Output Fall Time	t_f	C_{LOAD} = 20 pF, R_{LOAD} = 1 kΩ	–	300	–	ns
Supply Current	I_{CC}		3.4	8.2	14	mA
Low Output Voltage	V_{sat}	All outputs; I_{OUT} = 15 mA; $B > B_{OP(A)}$, $B > B_{OP(B)}$	–	210	500	mV
Output Current Limit	I_{OM}	All outputs	30	–	60	mA
Speed Output Delay*	t_d	Delay between direction changing and speed output transition	0.5	2.5	5	µs
Power-on Time	t_{ON}	$B > B_{OP} + 5$ G	–	2	5	µs
Transient Protection Characteristics						
Supply Zener Voltage	$V_{Z(sup)}$	I_{CC} = 17 mA, T_A = 25°C	30	–	–	V
Output Zener Voltage	$V_{Z(out)}$	I_{OUT} = 3 mA, T_A = 25°C	30	–	–	V
Supply Zener Current	$I_{Z(sup)}$	V_{supply} = 30 V, T_A = 25°C	–	–	17	mA
Output Zener Current	$I_{Z(out)}$	V_{OUT} = 30 V, T_A = 25°C	–	–	3	mA
Reverse Battery Current	I_{RCC}	V_{RCC} = –28 V, T_A = 25°C	–	–	15	mA
Magnetic Characteristics						
Operate Point (Channel A and Channel B)	B_{OP}	$B_{(A)} > B_{OP(A)}$, $B_{(B)} > B_{OP(B)}$	–35	15	55	G
Release Point (Channel A and Channel B)	B_{RP}	$B_{(A)} < B_{OP(A)}$, $B_{(B)} < B_{OP(B)}$	–55	–15	35	G
Hysteresis (Channel A and Channel B)	B_{hys}	$B_{OP} – B_{RP}$	10	30	60	G
Operate Symmetry	$SYM_{OP(AB)}$	$B_{OP(A)} – B_{OP(B)}$	–50	–	50	G
Release Symmetry	$SYM_{RP(AB)}$	$B_{RP(A)} – B_{RP(B)}$	–50	–	50	G

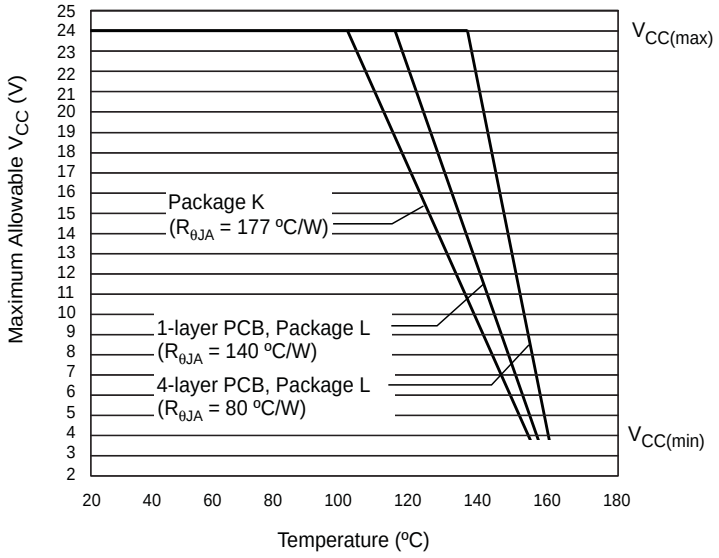
* Valid only after the first speed (SPD pin) signal transition. First speed signal transition has no delay.

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

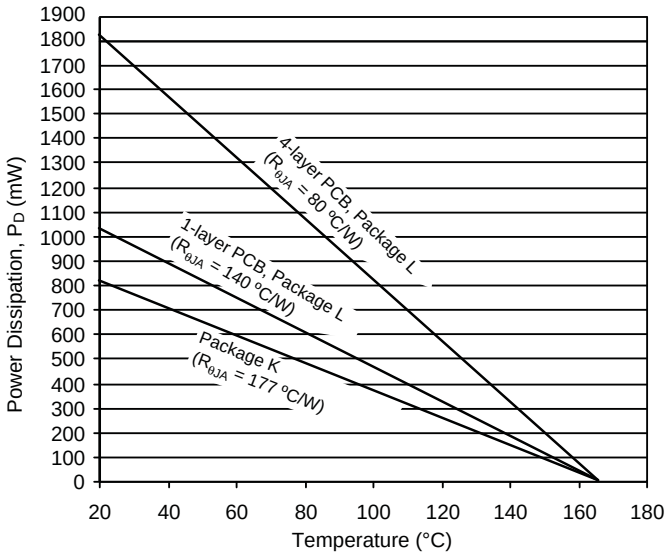
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package K, 1-layer PCB with copper limited to solder pads	177	ºC/W
		Package L, 1-layer PCB with copper limited to solder pads	140	ºC/W
		Package L, 4-layer PCB	80	ºC/W

*Additional thermal information available on Allegro website.

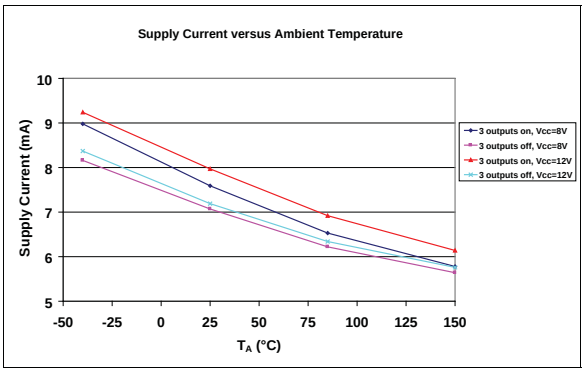
Power Derating Curve

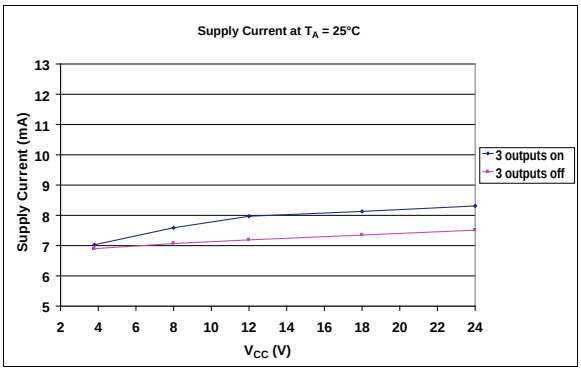


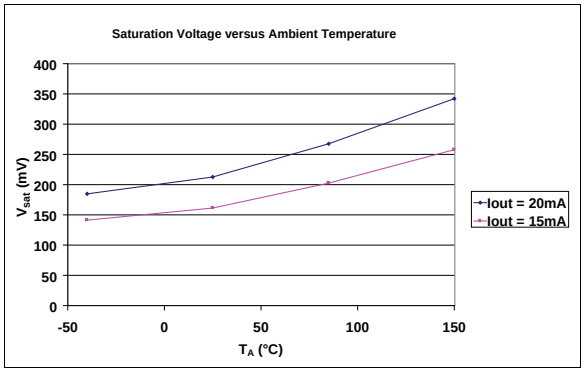
Power Dissipation versus Ambient Temperature

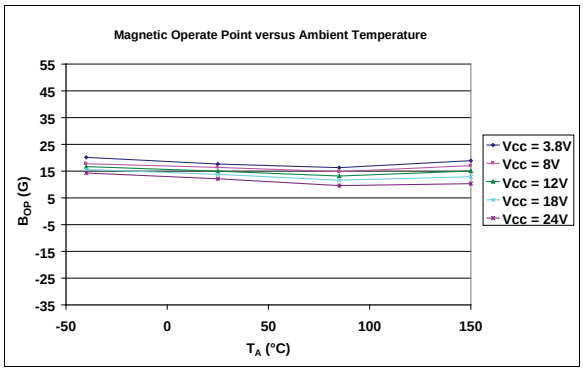


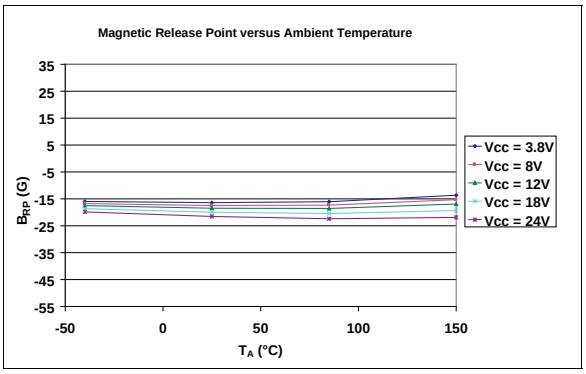
Performance Characteristics

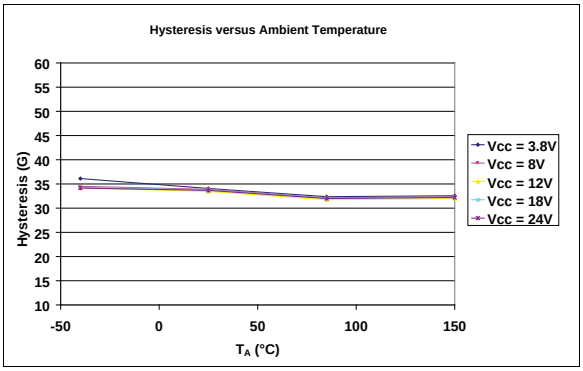












Functional Description

The integrated circuit contains an internal voltage regulator that powers the Hall elements and both the analog and digital circuitry. This regulator allows operation over a wide supply voltage range and provides some immunity to supply noise. The device also contains logic circuitry that decodes the direction of rotation of the ring magnet.

Quadrature/Direction Detection Internal logic circuitry provides outputs representing the speed and direction of the magnetic field across the face of the package. For the direction signal to be appropriately updated, a quadrature relationship must be maintained between the target magnetic pole width, the pitch between the two Hall elements (E1 and E2) in the device, and, to a lesser extent, the magnetic switchpoints.

For optimal design, the device should be actuated by a ring magnet that presents to the front of the device a field with a pole width two times the Hall element-to-element spacing. This will produce a sinusoidal magnetic field whose period (denoted as *T*) is then four times the element-to-element spacing. A quadrature relationship can also be maintained for a ring magnet with fields having a period that satisfies the relationship:

$$nT/4 = 1.63 \text{ mm},$$

where *n* is any odd integer. Therefore, ring magnets with pole-pair spacing equal to 6.52 mm ($n = 1$), 2.17 mm ($n = 3$), 1.3 mm ($n = 5$), and so forth, are permitted.

The response of the device to the magnetic field produced by a rotating ring magnet is shown in the Performance Characteristics section. Note the phase shift between the two integrated Hall elements.

Outputs The device provides up to four saturated outputs: target direction (DIR pin), E1 element output (OUTA pin), E2 element output (OUTB pin), and target speed (SPD pin).

DIR provides the direction output of the device and is defined as off (high) for targets moving in the direction from E1 to E2 and on (low) for the direction E2 to E1. SPD provides an XORed output of the two Hall elements (see figure 1). Because of internal delays, DIR is always updated before SPD and is updated at every transition of OUTA and OUTB (internal) allowing the use of up-down counters without the loss of pulses.

Power-on State At power on, the logic circuitry is reset to provide an off (high) state for all the outputs. If any of the channels is subjected to a field greater than B_{OP}, the internal logic will set accordingly, and the outputs will switch to the expected state.

Power-on Time This characteristic, t_{ON}, is the elapsed time from when the supply voltage reaches the device supply minimum until the device output becomes valid (see figure 2).

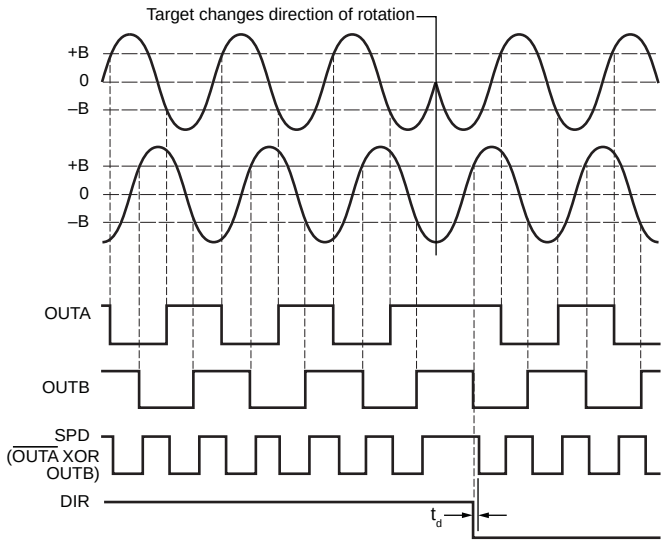


Figure 1

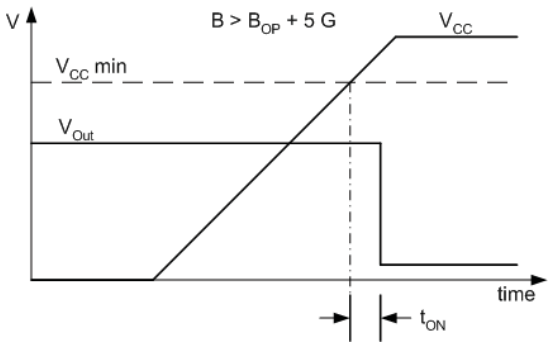


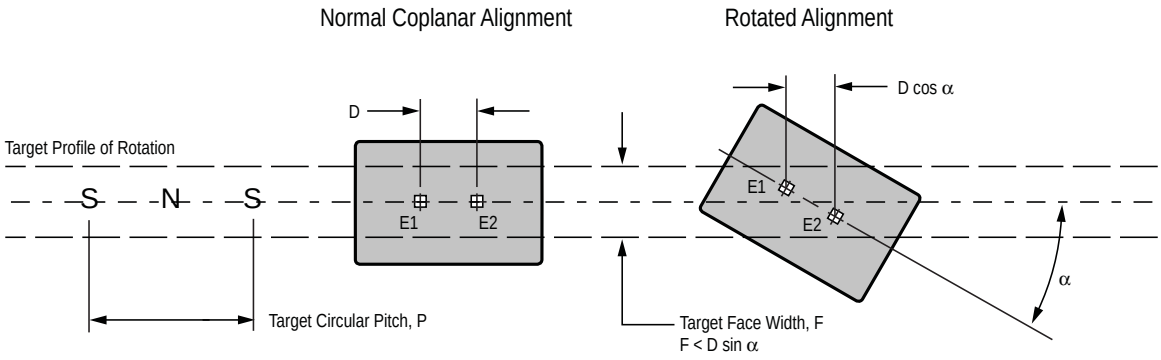
Figure 2

Application Information

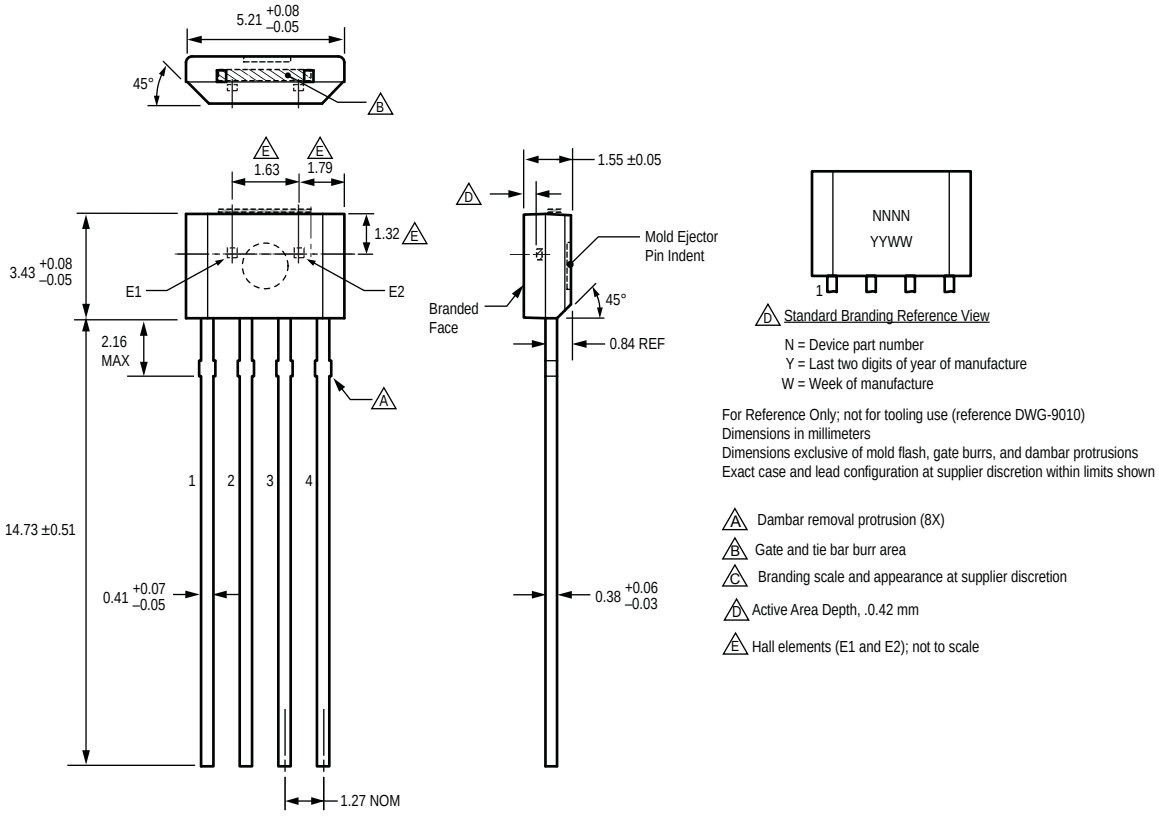
Operation with Fine-Pitch Ring Magnets. For targets with a circular pitch of less than 4 mm, a performance improvement can be observed by rotating the front face of the device (see below). This rotation decreases the effective Hall element-to-element spacing, provided that the Hall elements are not rotated beyond the width of the target.

Applications. It is strongly recommended that an external 0.01 µF bypass capacitor be connected (in close proximity to the device) between the supply and ground of the device to reduce both external noise and noise generated by the internal logic.

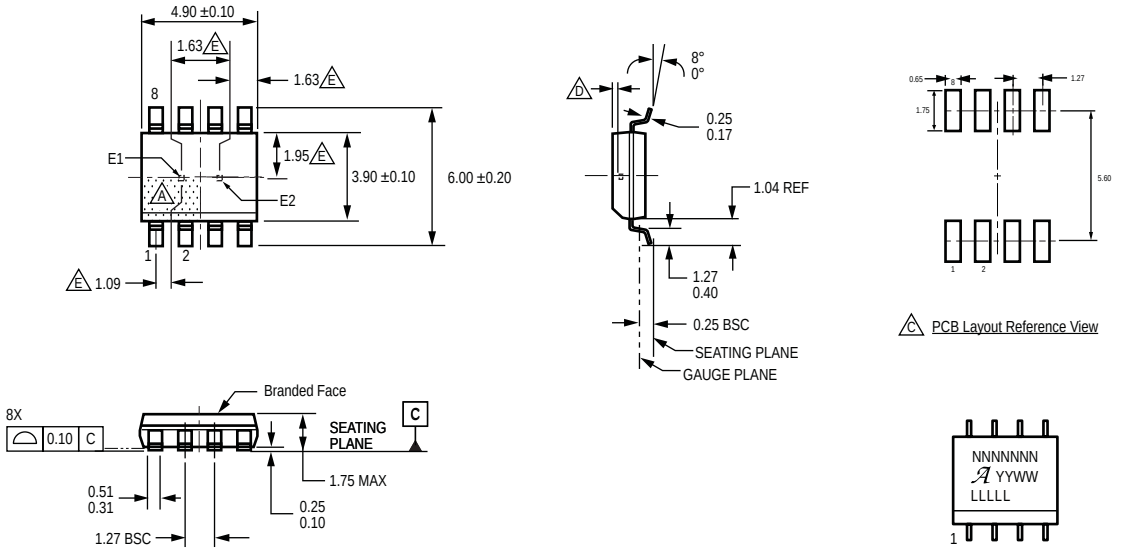
The simplest form of magnet that will operate these devices is a ring magnet. Other methods of operation, such as linear magnets, are possible. Extensive applications information on magnets and Hall-effect sensor ICs is also available in the "Hall-Effect IC Applications Guide" which can be found in the latest issue of Application Note 27701, at www.allegromicro.com/techpub2/an/an27701.pdf.



Package K, 4-Pin SIP



Package L, 8-Pin SOIC



For Reference Only; not for tooling use (reference MS-012AA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Branding scale and appearance at supplier discretion

C Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

D Active Area Depth 0.40 NOM

E Hall elements (E1 and E2); not to scale

B Standard Branding Reference View

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

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