

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections to the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

| | |
|---|---------------------------------------|
| V_{CC} | -0.3V to +7.0V |
| Input Voltage at Control and Driver Input (\overline{RE} , DE, and DI) | -0.3V to +7.0V |
| Receiver Output Voltage (RO) | -0.3V to ($V_{CC} + 0.3V$) |
| Driver Output Voltage (A, B, Y and Z) | $\pm 18V$ |
| Receiver Input Voltage (A and B, half or full duplex) | $\pm 18V$ |
| Transient Voltage Pulse, through 100 Ω | $\pm 70V$ |
| Driver Output Current | $\pm 250mA$ |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Package Power Dissipation 8-Pin SO $\Theta_{JA} = 128.4^{\circ}C/W$ 14-Pin SO $\Theta_{JA} = 86^{\circ}C/W$ | Maximum Junction Temperature = +150°C |

CAUTION:

ESD (Electrostatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING INFORMATION

| PART NUMBER | DUPLEX | DATA RATE | PACKAGE | TEMPERATURE RANGE |
|-------------|--------|-----------|--------------------|-------------------|
| XR3080XID-F | Full | 250kbps | 14-pin Narrow SOIC | -40°C to +85°C |
| XR3081XID-F | Full | 250kbps | 8-pin Narrow SOIC | -40°C to +85°C |
| XR3082XID-F | Half | 250kbps | 8-pin Narrow SOIC | -40°C to +85°C |
| XR3083XID-F | Full | 1Mbps | 14-pin Narrow SOIC | -40°C to +85°C |
| XR3084XID-F | Full | 1Mbps | 8-pin Narrow SOIC | -40°C to +85°C |
| XR3085XID-F | Half | 1Mbps | 8-pin Narrow SOIC | -40°C to +85°C |
| XR3086XID-F | Full | 20Mbps | 14-pin Narrow SOIC | -40°C to +85°C |
| XR3087XID-F | Full | 20Mbps | 8-pin Narrow SOIC | -40°C to +85°C |
| XR3088XID-F | Half | 20Mbps | 8-pin Narrow SOIC | -40°C to +85°C |

NOTE: Tape and Reel part numbers are XR30xxXIDTR-F, -F = Green / RoHS Compliant

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: $V_{CC} = +5.0V \pm 10\%$, $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $V_{CC} = 5.0V$, $T_A = +25^\circ C$.

| SYMBOL | PARAMETERS | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---------------------------------------|--|------|--------------|-----------|------------|---|
| DRIVER DC CHARACTERISTICS | | | | | | |
| V_{CC} | Supply Voltage Range | 4.5 | | 5.5 | V | |
| V_{OD} | Differential Driver Output | 3 | | V_{CC} | V | No Load |
| | | 3 | | V_{CC} | V | $R_L = 100\Omega$ (RS-422), Figure 3 |
| | | 2.1 | | V_{CC} | V | $R_L = 54\Omega$ (RS-485), Figure 3 |
| | | 2.1 | | V_{CC} | V | $-7V \leq V_{CM} \leq +12V$, Figure 4 |
| ΔV_{OD} | Change in Magnitude of Differential Output Voltage | | | ± 0.2 | V | $R_L = 100\Omega$ (RS-422), or $R_L = 54\Omega$ (RS-485), Figure 3 , Note 1 |
| V_{CM} | Driver Common-Mode Output Voltage (steady state) | | $V_{CC} / 2$ | 3 | V | |
| ΔV_{CM} | Change in Magnitude of Common-Mode Output Voltage | | | ± 0.2 | V | |
| V_{IH} | Logic Input Thresholds (DI, DE, \overline{RE}) | 2.0 | | | V | Logic Input High |
| V_{IL} | | | | | V | Logic Input Low |
| V_{HYS} | Input Hysteresis (DI, DE, \overline{RE}) | | 100 | | mV | |
| I_{IN} | Logic Input Current (DI, DE, \overline{RE}) | | | ± 1 | μA | $0V \leq V_{IN} \leq V_{CC}$, After first transition, Note 2 |
| | Logic Input Current (DE and \overline{RE}) | | 100 | ± 200 | μA | Until first transition, Note 2 |
| $I_{A, B}$ | Input Current (A and B) | | | 125 | μA | $V_{OUT} = +12V$, $DE = 0V$, $V_{CC} = 0V$ or $5.5V$ |
| | | -100 | | | μA | $V_{OUT} = -7V$, $DE = 0V$, $V_{CC} = 0V$ or $5.5V$ |
| I_{OL} | Output Leakage (Y and Z) Full Duplex (Note 2) | | | 125 | μA | $V_{OUT} = +12V$, $DE = 0V$, $V_{CC} = 0V$ or $5.5V$ |
| | | -100 | | | μA | $V_{OUT} = -7V$, $DE = 0V$, $V_{CC} = 0V$ or $5.5V$ |
| I_{OSD} | Driver Short-Circuit Output Current | | | ± 250 | mA | $-7V \leq V_{OUT} \leq +12V$, Figure 5 |
| DRIVER THERMAL CHARACTERISTICS | | | | | | |
| T_{TS} | Thermal Shutdown Temperature | | 175 | | $^\circ C$ | Junction temperature, Note 4 |
| T_{TSH} | Thermal Shutdown Hysteresis | | 15 | | $^\circ C$ | Note 4 |

Unless otherwise noted: $V_{CC} = +5.0V \pm 10\%$, $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $V_{CC} = 5.0V$, $T_A = +25^\circ C$.

| SYMBOL | PARAMETERS | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|------------------------------------|---|--------------|----------|----------|------------|---|
| RECEIVER DC CHARACTERISTICS | | | | | | |
| V_{TH} | Receiver Differential Threshold Voltage ($V_A - V_B$) | -200 | -125 | -50 | mV | $-7V \leq V_{CM} \leq +12V$ |
| ΔV_{OH} | Receiver Input Hysteresis | | 25 | | mV | $V_{CM} = 0V$ |
| V_{OH} | Receiver Output High Voltage (RO) | $V_{CC}-1.5$ | | | V | $I_{OUT} = -4mA$ |
| V_{OL} | Receiver Output Low Voltage (RO) | | | 0.4 | V | $I_{OUT} = 4mA$ |
| I_{OZR} | High-Z Receiver Output Current | | | ± 1 | μA | $0V \leq V_{OUT} \leq V_{CC}$ |
| R_{IN} | Receiver Input Resistance | 96 | | | k Ω | $-7V \leq V_{CM} \leq +12V$ |
| I_{OSC} | Receiver Output Short-Circuit Current | | | ± 95 | mA | $0V \leq V_{RO} \leq V_{CC}$ |
| SUPPLY CURRENT | | | | | | |
| I_{CC} | Supply Current | | 425 | 600 | μA | No Load, $\overline{RE} = 0V$, $DE = V_{CC}$ $DI = 0V$ |
| | | | 330 | 600 | μA | No Load, $\overline{RE} = V_{CC}$, $DE = V_{CC}$ $DI = 0V$ |
| | | | 300 | 600 | μA | No Load, $\overline{RE} = 0V$, $DE = 0V$ Receiver A and B inputs open |
| I_{SHDN} | Supply Current in Shutdown Mode | | 0.001 | 1 | μA | $\overline{RE} = V_{CC}$, $DE = 0V$ |
| ESD PROTECTION | | | | | | |
| | ESD Protection for A, B, Y, and Z | | ± 15 | | kV | Human Body Model |
| | | | ± 15 | | kV | IEC 61000-4-2 Airgap |
| | | | ± 8 | | kV | IEC 61000-4-2 Contact |
| | ESD Protection for all other pins | | ± 4 | | kV | Human Body Model |

Unless otherwise noted: $V_{CC} = +5.0V \pm 10\%$, $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $V_{CC} = 5.0V$, $T_A = +25^\circ C$.

| SYMBOL | PARAMETERS | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|--|------|------|------|-------|---|
| DRIVER AC CHARACTERISTICS | | | | | | |
| XR3080X, XR3081X and XR3082X (250kbps) | | | | | | |
| t_{DPLH} | Driver Prop. Delay (Low to High) | 350 | | 1500 | ns | $C_L = 50pF$, $R_L = 54\Omega$, Figure 6 |
| t_{DPHL} | Driver Prop. Delay (High to Low) | 350 | | 1500 | ns | |
| $ t_{DPLH} - t_{DPHL} $ | Differential Driver Output Skew | | 20 | 200 | ns | |
| t_{DR} , t_{DF} | Driver Differential Output Rise or Fall Time | 400 | | 1500 | ns | |
| | Maximum Data Rate | 250 | | | kbps | $1/t_{UI}$, Duty Cycle 40 to 60% |
| t_{DZH} | Driver Enable to Output High | | 200 | 2500 | ns | $C_L = 50pF$, $R_L = 500\Omega$, Figure 7 |
| t_{DZL} | Driver Enable to Output Low | | 200 | 2500 | ns | |
| t_{DZH} | Driver Disable from Output High | | 6 | 100 | ns | |
| t_{DLZ} | Driver Disable from Output Low | | 6 | 100 | ns | |
| $t_{DZH(SHDN)}$ | Driver Enable from Shutdown to Output High | | | 5500 | ns | $C_L = 50pF$, $R_L = 500\Omega$, Figure 7 |
| $t_{DZL(SHDN)}$ | Driver Enable from Shutdown to Output Low | | | 5500 | ns | |
| t_{SHDN} | Time to Shutdown | 50 | 200 | 600 | ns | Notes 3 and 4 |
| RECEIVER AC CHARACTERISTICS | | | | | | |
| XR3080X, XR3081X and XR3082X (250kbps) | | | | | | |
| t_{RPLH} | Receiver Prop. Delay (Low to High) | | | 200 | ns | $C_L = 15pF$, $V_{ID} = \pm 2V$, V_{ID} Rise and Fall times < 15ns Figure 8 |
| t_{RPHL} | Receiver Prop. Delay (High to Low) | | | 200 | ns | |
| $ t_{RPLH} - t_{RPHL} $ | Receiver Propagation Delay Skew | | | 30 | ns | |
| | Maximum Data Rate | 250 | | | kbps | $1/t_{UI}$, Duty Cycle 40 to 60% |
| t_{RZH} | Receiver Enable to Output High | | | 50 | ns | $C_L = 15pF$, $R_L = 1k\Omega$, Figure 9 |
| t_{RZL} | Receiver Enable to Output Low | | | 50 | ns | |
| t_{RZH} | Receiver Disable from Output High | | | 50 | ns | |
| t_{RLZ} | Receiver Disable from Output Low | | | 50 | ns | |
| $t_{RZH(SHDN)}$ | Receiver Enable from Shutdown to Output High | | | 3500 | ns | $C_L = 15pF$, $R_L = 1k\Omega$, Figure 9 |
| $t_{RZL(SHDN)}$ | Receiver Enable from Shutdown to Output Low | | | 3500 | ns | |
| t_{SHDN} | Time to Shutdown | 50 | 200 | 600 | ns | Notes 3 and 4 |

Unless otherwise noted: $V_{CC} = +5.0V \pm 10\%$, $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $V_{CC} = 5.0V$, $T_A = +25^\circ C$.

| SYMBOL | PARAMETERS | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|--|------|------|------|-------|---|
| DRIVER AC CHARACTERISTICS XR3083X, XR3084X and XR3085X (1Mbps) | | | | | | |
| t_{DPLH} | Driver Prop. Delay (Low to High) | | 150 | 500 | ns | $C_L = 50pF$, $R_L = 54\Omega$, Figure 6 |
| t_{DPHL} | Driver Prop. Delay (High to Low) | | 150 | 500 | ns | |
| $ t_{DPLH} - t_{DPHL} $ | Differential Driver Output Skew | | 5 | 50 | ns | |
| t_{DR} , t_{DF} | Driver Differential Output Rise or Fall Time | 100 | 200 | 300 | ns | |
| | Maximum Data Rate | 1 | | | Mbps | $1/t_{UI}$, Duty Cycle 40 to 60% |
| t_{DZH} | Driver Enable to Output High | | 1000 | 2500 | ns | $C_L = 50pF$, $R_L = 500\Omega$, Figure 7 |
| t_{DZL} | Driver Enable to Output Low | | 1000 | 2500 | ns | |
| t_{DHZ} | Driver Disable from Output High | | 60 | 100 | ns | |
| t_{DLZ} | Driver Disable from Output Low | | 60 | 100 | ns | |
| $t_{DZH(SHDN)}$ | Driver Enable from Shutdown to Output High | | 2500 | 4500 | ns | $C_L = 50pF$, $R_L = 500\Omega$, Figure 7 |
| $t_{DZL(SHDN)}$ | Driver Enable from Shutdown to Output Low | | 2500 | 4500 | ns | |
| t_{SHDN} | Time to Shutdown | 50 | 200 | 600 | ns | Notes 3 and 4 |
| RECEIVER AC CHARACTERISTICS XR3083X, XR3084X and XR3085X (1Mbps) | | | | | | |
| t_{RPLH} | Receiver Prop. Delay (Low to High) | | | 200 | ns | $C_L = 15pF$, $V_{ID} = \pm 2V$, V_{ID} Rise and Fall times < 15ns Figure 8 |
| t_{RPHL} | Receiver Prop. Delay (High to Low) | | | 200 | ns | |
| $ t_{RPLH} - t_{RPHL} $ | Receiver Propagation Delay Skew | | | 30 | ns | |
| | Maximum Data Rate | 1 | | | Mbps | $1/t_{UI}$, Duty Cycle 40 to 60% |
| t_{RZH} | Receiver Enable to Output High | | | 50 | ns | $C_L = 15pF$, $R_L = 1k\Omega$, Figure 9 |
| t_{RZL} | Receiver Enable to Output Low | | | 50 | ns | |
| t_{RHZ} | Receiver Disable from Output High | | | 50 | ns | |
| t_{RLZ} | Receiver Disable from Output Low | | | 50 | ns | |
| $t_{RZH(SHDN)}$ | Receiver Enable from Shutdown to Output High | | | 3500 | ns | $C_L = 15pF$, $R_L = 1k\Omega$, Figure 9 |
| $t_{RZL(SHDN)}$ | Receiver Enable from Shutdown to Output Low | | | 3500 | ns | |
| t_{SHDN} | Time to Shutdown | 50 | 200 | 600 | ns | Notes 3 and 4 |

Unless otherwise noted: $V_{CC} = +5.0V \pm 10\%$, $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $V_{CC} = 5.0V$, $T_A = +25^\circ C$.

| SYMBOL | PARAMETERS | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|--|--|------|------|------|-------|---|
| DRIVER AC CHARACTERISTICS | | | | | | |
| XR3086X, XR3087X and XR3088X (20Mbps) | | | | | | |
| t_{DPLH} | Driver Prop. Delay (Low to High) | | | 20 | ns | $C_L = 50pF$, $R_L = 54\Omega$, Figure 6 |
| t_{DPHL} | Driver Prop. Delay (High to Low) | | | 20 | ns | |
| $ t_{DPLH} - t_{DPHL} $ | Differential Driver Output Skew | | | 5 | ns | |
| t_{DR} , t_{DF} | Driver Differential Output Rise or Fall Time | | | 15 | ns | |
| | Maximum Data Rate | 20 | | | Mbps | $1/t_{UI}$, Duty Cycle 40 to 60% |
| t_{DZH} | Driver Enable to Output High | | | 30 | ns | $C_L = 50pF$, $R_L = 500\Omega$, Figure 7 |
| t_{DZL} | Driver Enable to Output Low | | | 30 | ns | |
| t_{DZH} | Driver Disable from Output High | | | 30 | ns | |
| t_{DLZ} | Driver Disable from Output Low | | | 30 | ns | |
| $t_{DZH(SHDN)}$ | Driver Enable from Shutdown to Output High | | | 250 | ns | $C_L = 50pF$, $R_L = 500\Omega$, Figure 7 |
| $t_{DZL(SHDN)}$ | Driver Enable from Shutdown to Output Low | | | 250 | ns | |
| t_{SHDN} | Time to Shutdown | 50 | 200 | 600 | ns | Notes 3 and 4 |
| RECEIVER AC CHARACTERISTICS | | | | | | |
| XR3086X, XR3087X and XR3088X (20Mbps) | | | | | | |
| t_{RPLH} | Receiver Prop. Delay (Low to High) | | | 40 | ns | $C_L = 15pF$, $V_{ID} = \pm 2V$, V_{ID} Rise and Fall times < 15ns Figure 8 |
| t_{RPHL} | Receiver Prop. Delay (High to Low) | | | 40 | ns | |
| $ t_{RPLH} - t_{RPHL} $ | Receiver Propagation Delay Skew | | | 5 | ns | |
| | Maximum Data Rate | 20 | | | Mbps | $1/t_{UI}$, Duty Cycle 40 to 60% |
| t_{RZH} | Receiver Enable to Output High | | | 30 | ns | $C_L = 15pF$, $R_L = 1k\Omega$, Figure 9 |
| t_{RZL} | Receiver Enable to Output Low | | | 30 | ns | |
| t_{RZH} | Receiver Disable from Output High | | | 30 | ns | |
| t_{RLZ} | Receiver Disable from Output Low | | | 30 | ns | |
| $t_{RZH(SHDN)}$ | Receiver Enable from Shutdown to Output High | | | 2200 | ns | $C_L = 15pF$, $R_L = 1k\Omega$, Figure 9 |
| $t_{RZL(SHDN)}$ | Receiver Enable from Shutdown to Output Low | | | 2200 | ns | |
| t_{SHDN} | Time to Shutdown | 50 | 200 | 600 | ns | Notes 3 and 4 |

NOTE:

1. *Change in Magnitude of Differential Output Voltage and Change in Magnitude of Common Mode Output Voltage are the changes in output voltage when DI input changes state.*
2. *The hot swap feature disables the DE and \overline{RE} inputs for the first 10 μ s after power is applied. Following this time period these inputs are weakly pulled to their disabled state (low for DE, high for \overline{RE}) until the first transition, after which they become high impedance inputs.*
3. *The transceivers are put into shutdown by bringing \overline{RE} High and DE Low simultaneously for at least 600ns. If the control inputs are in this state for less than 50ns, the device is guaranteed to not enter shutdown. If the enable inputs are held in this state for at least 600ns the device is assured to be in shutdown. Note that the receiver and driver enable times increase significantly when coming out of shutdown.*
4. *This spec is guaranteed by design and bench characterization.*

BLOCK DIAGRAMS

FIGURE 1. HALF DUPLEX (XR3082X, XR3085X, XR3088X)

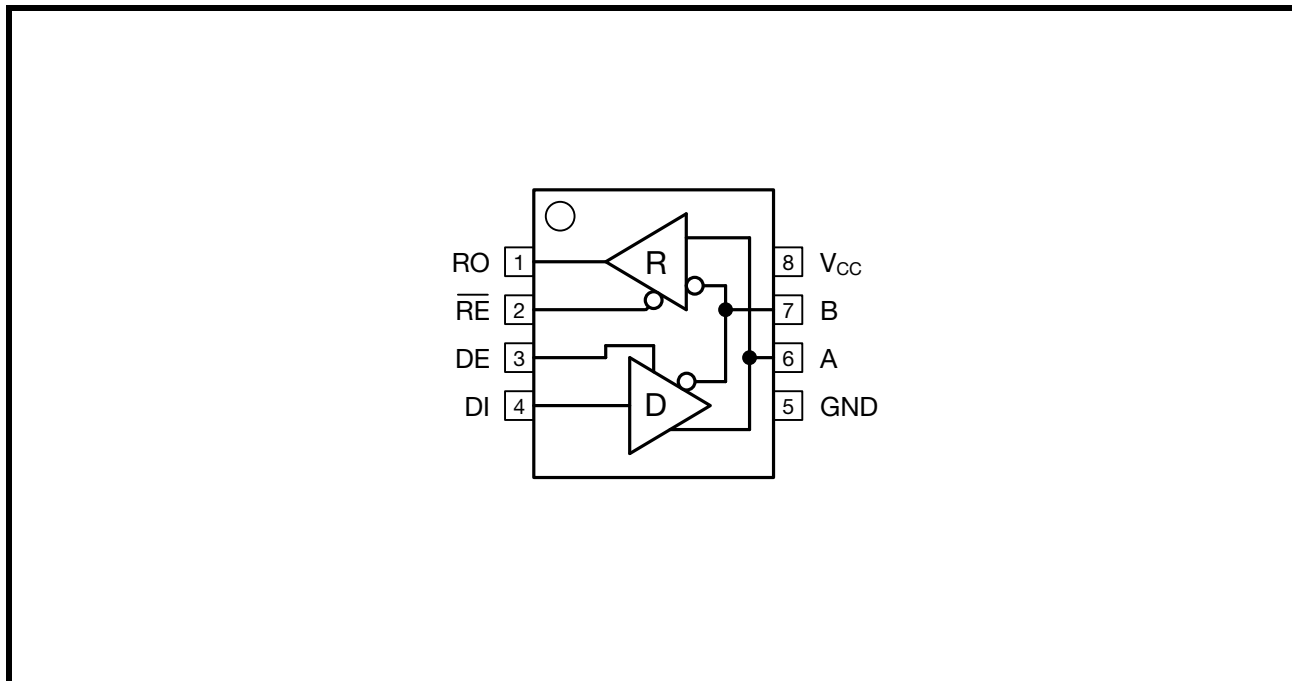
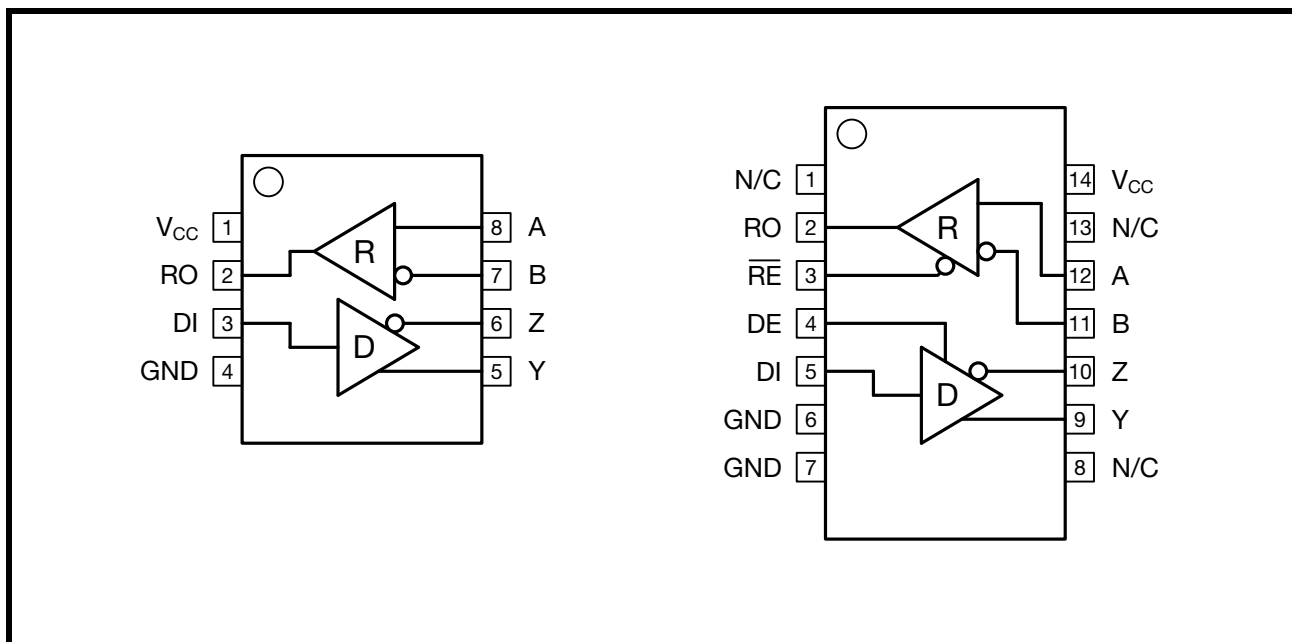


FIGURE 2. FULL DUPLEX (XR3080X, XR3081X, XR3083X, XR3084X, XR3086X, XR3087X)



TEST FIGURES

FIGURE 3. DIFFERENTIAL DRIVER OUTPUT VOLTAGE

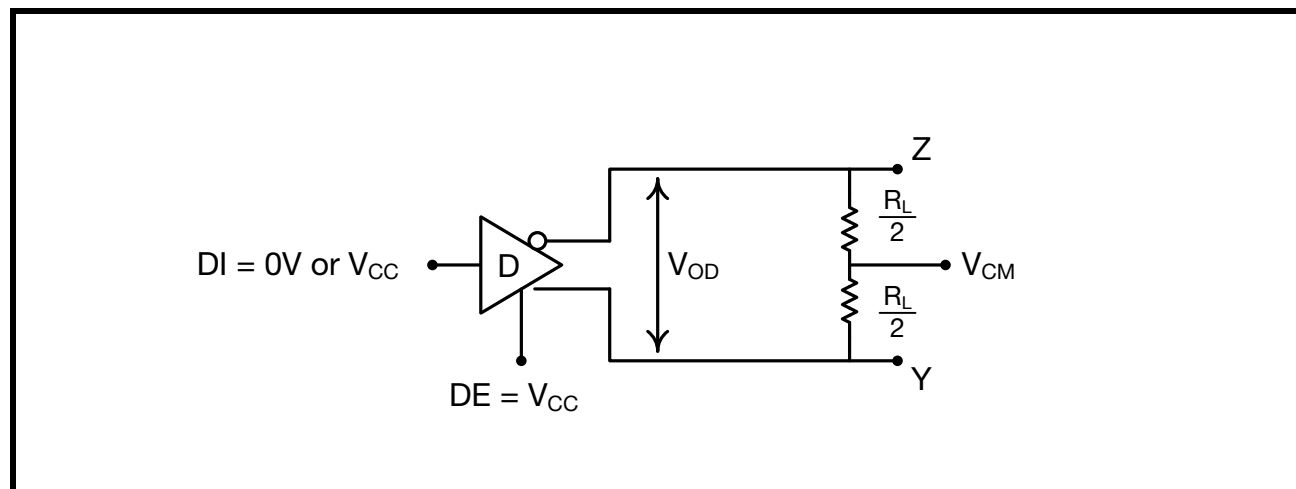


FIGURE 4. DIFFERENTIAL DRIVER OUTPUT VOLTAGE OVER COMMON MODE

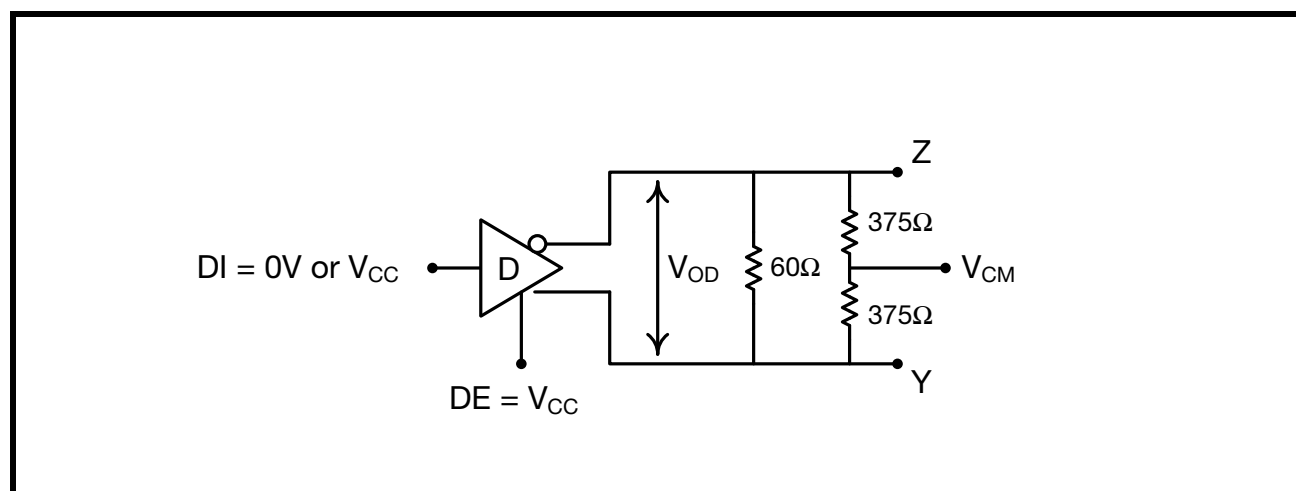


FIGURE 5. DRIVER OUTPUT SHORT CIRCUIT CURRENT

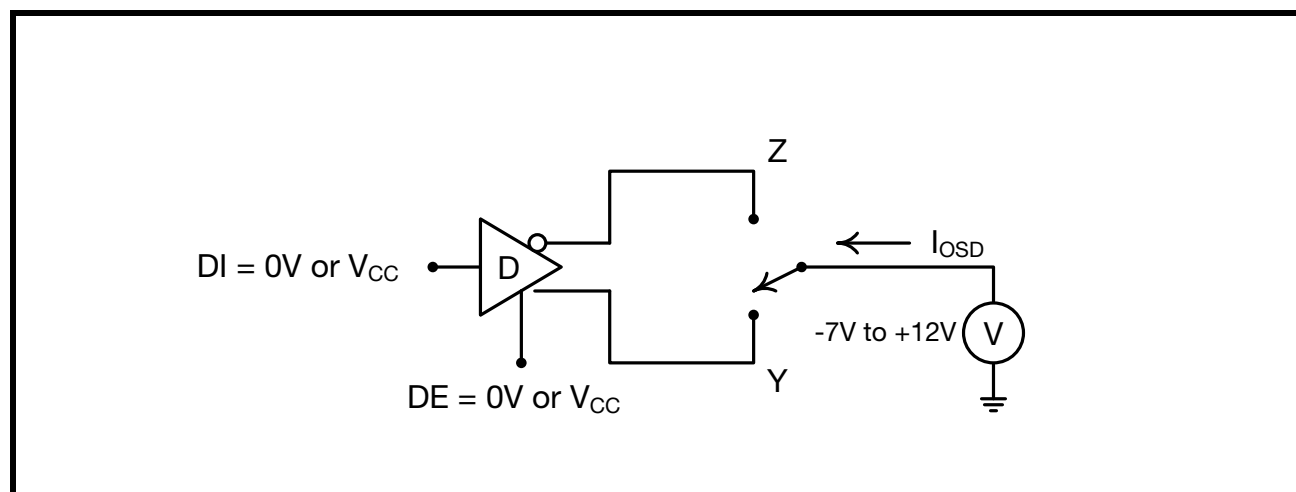


FIGURE 6. DRIVER PROPAGATION DELAY TEST CIRCUIT & TIMING DIAGRAM

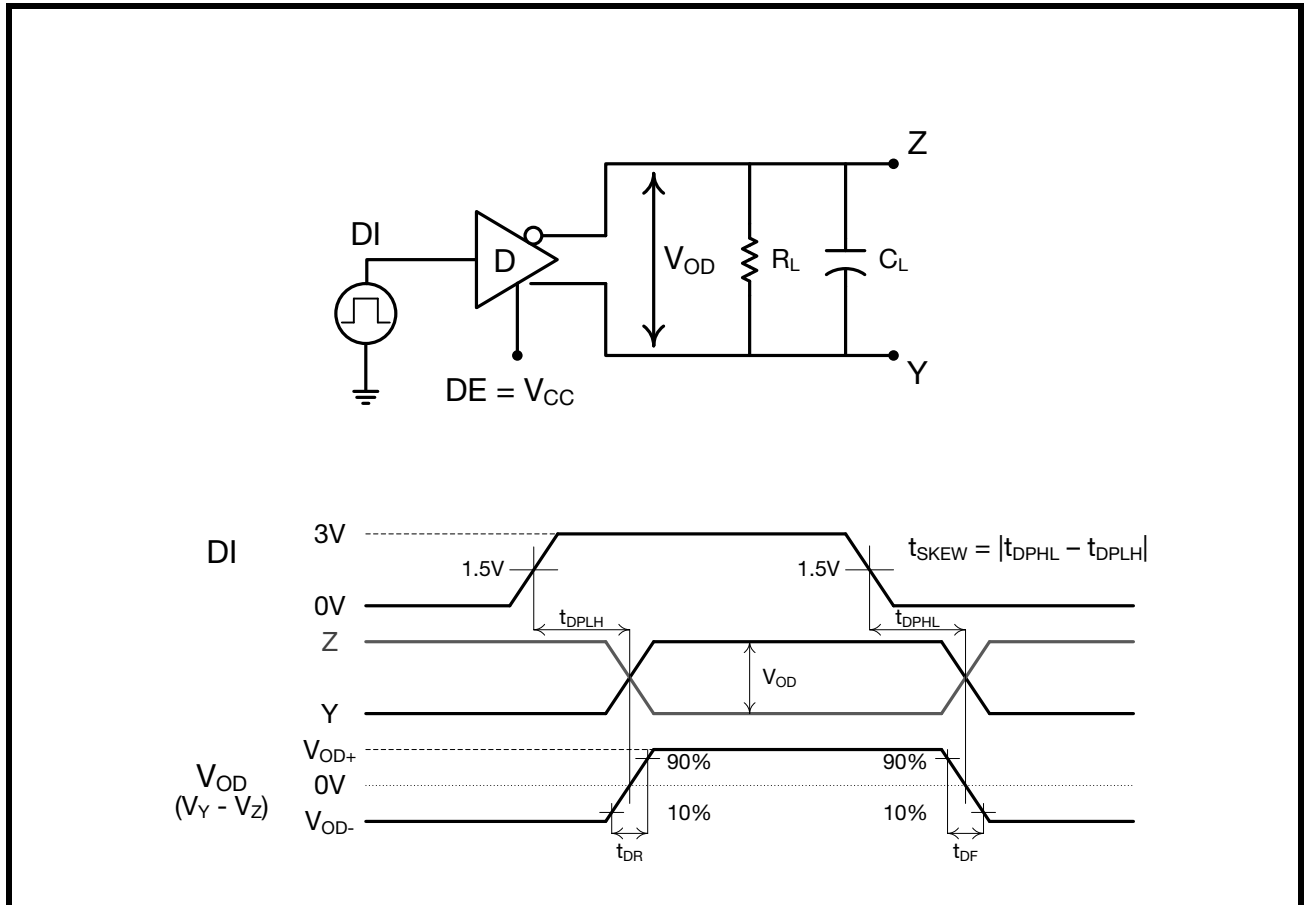


FIGURE 7. DRIVER ENABLE AND DISABLE TIMING TEST CIRCUITS & TIMING DIAGRAMS

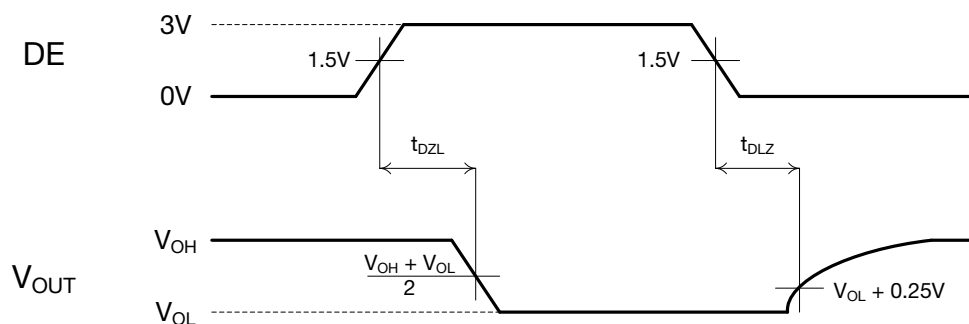
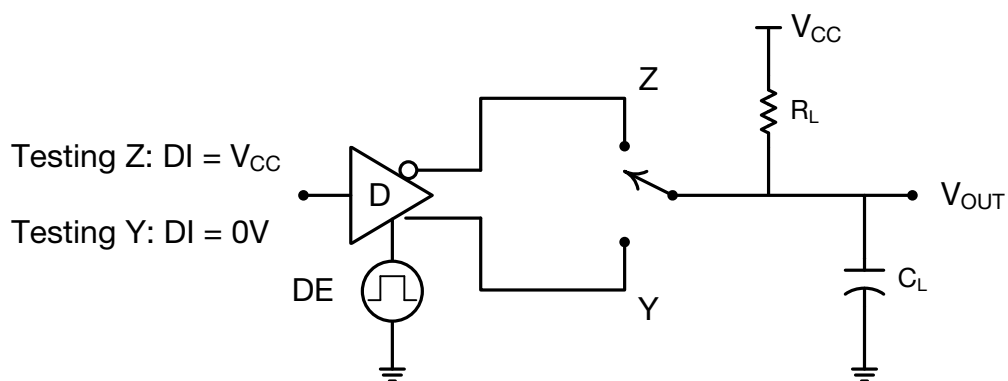
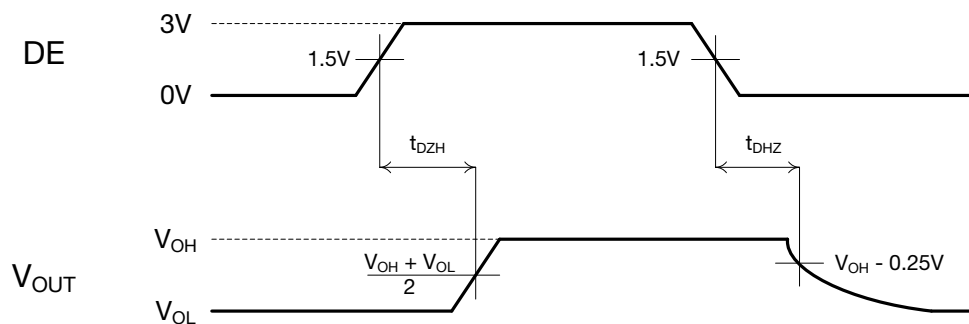
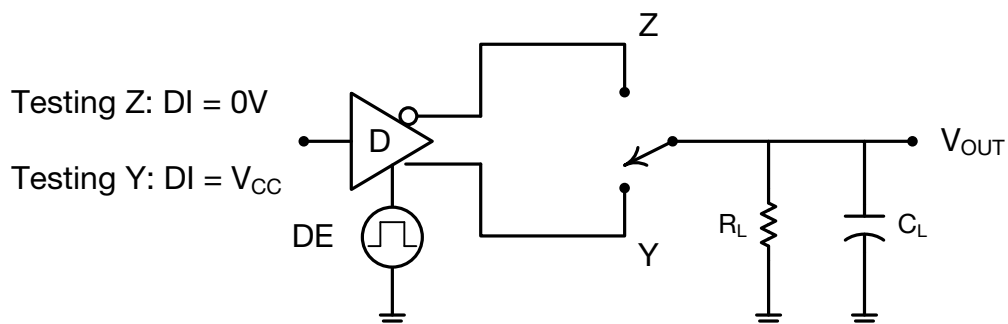


FIGURE 8. RECEIVER PROPAGATION DELAY TEST CIRCUIT & TIMING DIAGRAM

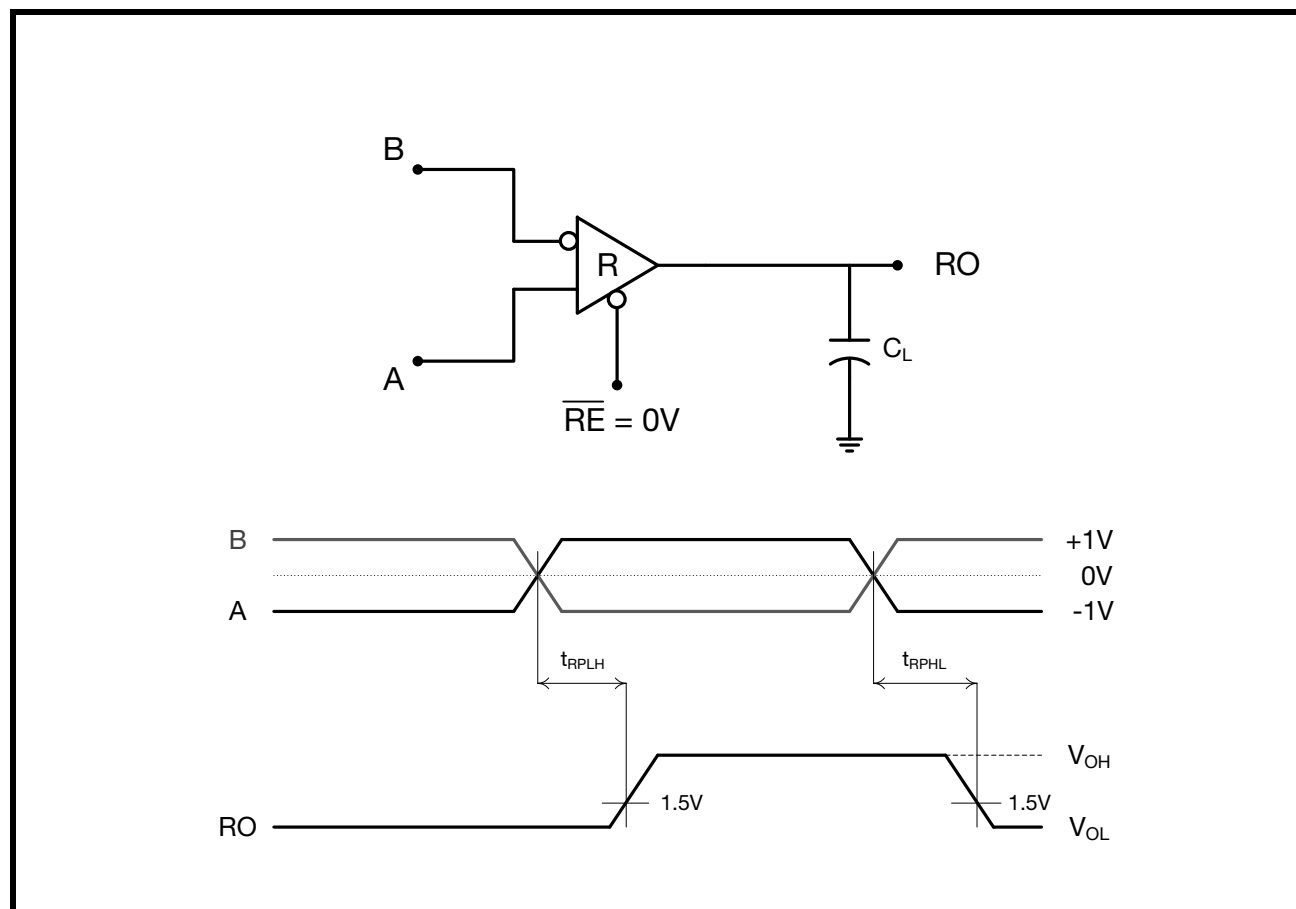
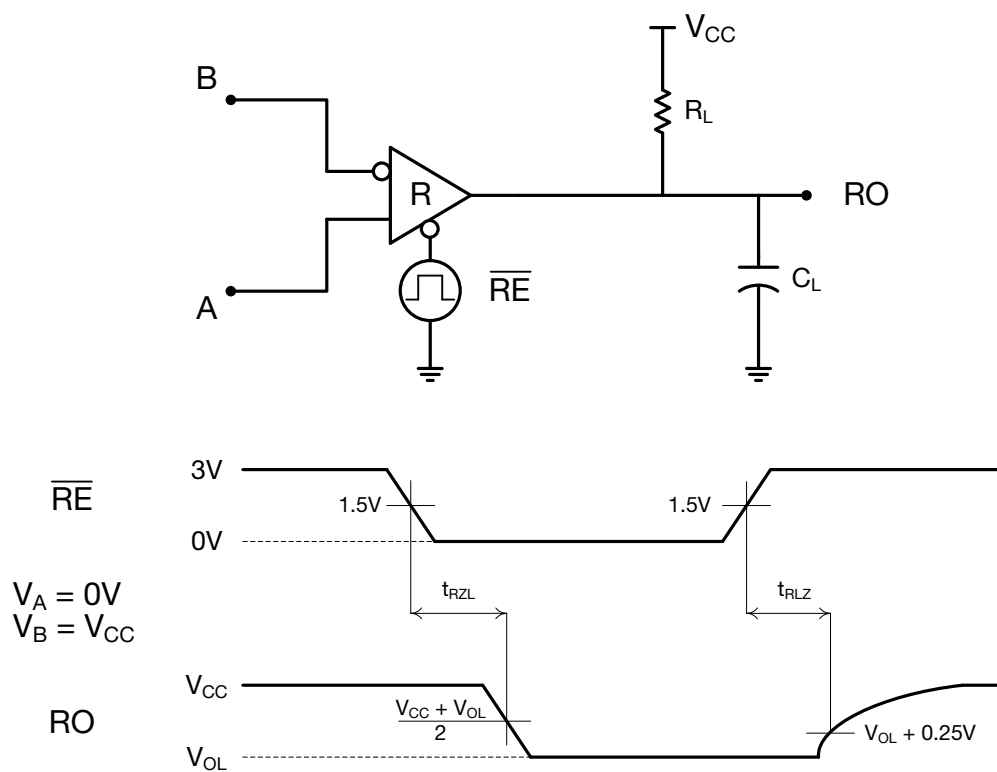
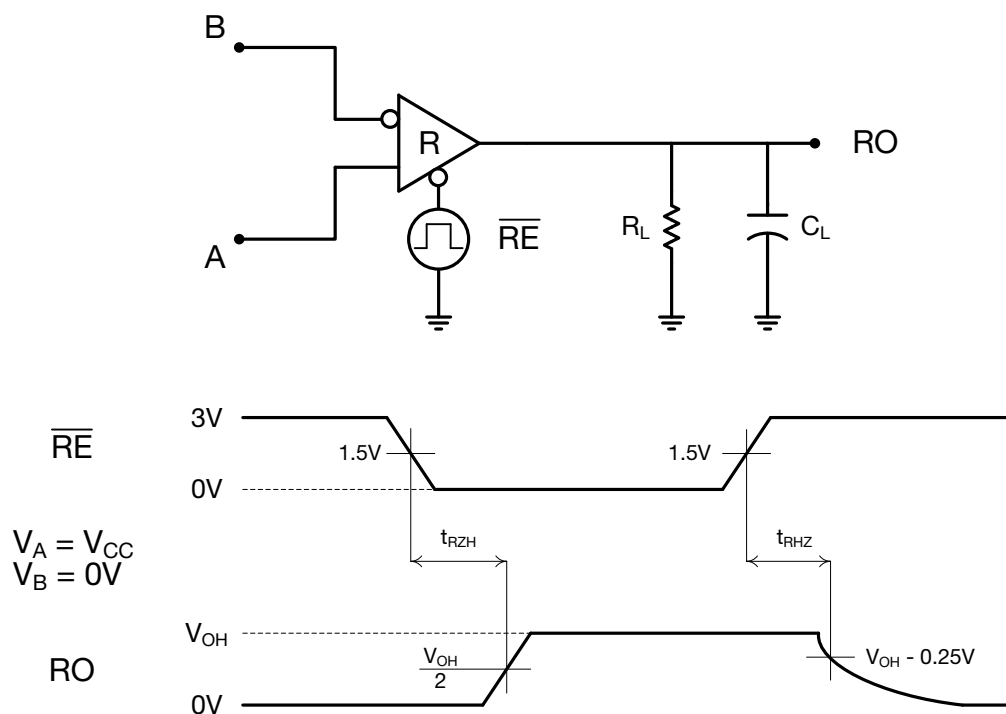


FIGURE 9. RECEIVER ENABLE AND DISABLE TEST CIRCUITS & TIMING DIAGRAMS



PIN DESCRIPTIONS

| PIN NUMBER | | | PIN NAME | TYPE | DESCRIPTION |
|-------------------------------|-------------------------------|-------------------------------|-----------------|------|--|
| HALF DUPLEX | FULL DUPLEX | | | | |
| XR3082X XR3085X XR3088X | XR3081X XR3084X XR3087X | XR3080X XR3083X XR3086X | | | |
| 1 | 2 | 2 | RO | Out | Receiver Output. When \overline{RE} is low and if (A-B) \leq -50mV, RO is high. If (A-B) \geq -200mV, RO is Low. |
| 2 | - | 3 | \overline{RE} | In | Receiver Output Enable (Hot Swap). When \overline{RE} is low, RO is enabled. When \overline{RE} is High, RO is high impedance. \overline{RE} should be high and DE should be low to enter shutdown mode. |
| 3 | - | 4 | DE | In | Driver Output Enable (Hot Swap). When DE is high, outputs are enabled. When DE is low, outputs are high impedance. DE should be low and \overline{RE} should be high to enter shutdown mode. |
| 4 | 3 | 5 | DI | In | Driver Input. With DE high, a low level on DI forces non-Inverting output low and inverting output high. Similarly, a high level on DI forces non-Inverting output high and inverting output low. |
| 5 | 4 | 6, 7 | GND | Pwr | Ground. |
| 6 | - | - | A | I/O | Non-Inverting Receiver Input and Non-Inverting Driver Output. |
| 7 | - | - | B | I/O | Inverting Receiver Input and Inverting Driver Output. |
| 8 | 1 | 14 | V _{CC} | Pwr | +5.0V Power Supply Input. Bypass to ground with 0.1 μ F capacitor. |
| - | 8 | 12 | A | In | Non-Inverting Receiver Input. |
| - | 7 | 11 | B | In | Inverting Reciever Input. |
| - | 5 | 9 | Y | Out | Non-Inverting Driver Output. |
| - | 6 | 10 | Z | Out | Inverting Driver Output. |
| - | - | 1, 8, 13 | N/C | - | No Connect, not internally connected. |

PRODUCT DESCRIPTION

The XR3080-88X RS-485/422 devices are part of Exar's X Series high performance serial interface product line. The analog bus pins can survive direct shorts up to $\pm 18V$, and are protected against ESD events up to $\pm 15kV$. The Profibus compliant differential output delivers 40% higher SNR than other RS-485/422 devices, affording additional noise margin or extended cable lengths.

ENHANCED FAILSAFE

Ordinary RS-485 differential receivers will be in an indeterminate state whenever the data bus is not being actively driven. The enhanced failsafe feature of the XR3080-88X family guarantees a logic-high receiver output when the receiver inputs are open, shorted, or when they are connected to a terminated transmission line with all drivers disabled. In a terminated bus with all transmitters disabled, the receivers' differential input voltage is pulled to 0V by the termination. The XR3080-88X family interprets 0V differential as a logic high with a minimum 50mV noise margin while maintaining compliance with the EIA/TIA-485 standard of $\pm 200mV$. Although the XR3080-88X family does not need failsafe biasing resistors, it can operate without issue if biasing is used.

RECEIVER INPUT FILTERING

XR3080-85X receivers incorporate internal filtering in addition to input hysteresis. This filtering enhances noise immunity by ignoring signals that do not meet a minimum pulse width of 30ns. Receiver propagation delay increases slightly due to this filtering. The high speed XR3086X, XR3087X and XR3088X devices do not have this input filtering.

HOT-SWAP CAPABILITY

When V_{CC} is first applied the XR3080-88X family holds the driver enable and receiver enable inactive for approximately 10 microseconds. During power ramp-up other system ICs may drive unpredictable values, or tristated lines may be influenced by stray capacitance. The hot-swap feature prevents the XR3080-88X family from driving any output signal until power has stabilized. After the initial $10\mu s$, the driver and receiver enable pins are weakly pulled to their disabled states (low for DE, high for \overline{RE}) until the first transition. After the first transition, the DE and \overline{RE} pins operate as high impedance inputs.

If circuit boards are inserted into an energized backplane (commonly called "live insertion" or "hot-swap") power may suddenly be applied to all circuits. Without the hot-swap capability, this situation could improperly enable the transceiver's driver or receiver, driving invalid data onto shared busses and possibly causing driver contention or device damage.

DRIVER OUTPUT PROTECTION

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. First, a driver current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. Second, a thermal-shutdown circuit forces the driver outputs into a high-impedance state if junction temperature becomes excessive.

LINE LENGTH

The RS-485/RS-422 standard covers line lengths up to 4000ft. Maximum achievable line length is a function of signal attenuation and noise. Termination prevents signal reflections by eliminating the impedance mismatches on a transmission line. Line termination is generally used if rise and fall times are shorter than the round-trip signal propagation time. Higher output drivers may allow longer cables to be used.

$\pm 15kV$ ESD PROTECTION

ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the XR3080-88X family have extra protection against static electricity. Exar uses state of the art structures to protect these pins against ESD of $\pm 15\text{kV}$ without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown and powered down. After an ESD event, the XR3080-88X keep operating without latch-up or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the XR3080-88X are characterized for protection to the following limits:

- $\pm 15\text{kV}$ using the Human Body Model
- $\pm 8\text{kV}$ using the Contact Discharge Model
- $\pm 15\text{kV}$ Air-gap Discharge Model

ESD TEST CONDITIONS

ESD performance depends on a variety of conditions. Contact Exar for a reliability report that documents test setup, methodology and results.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The XR3080-88X family helps you design equipment to meet IEC 61000-4-2, without sacrificing board-space and cost for external ESD-protection components.

The major differences between tests done using the Human body model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2. Series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that of human body model.

The air-gap test involves approaching the device with a charged probe. The contact discharge method connects the probe to the device before the probe is energized.

256 TRANSCEIVERS ON THE BUS

The standard RS-485 receiver input impedance is 12k Ohms (1 unit load). A standard driver can drive up to 32 unit loads. The XR3080-88X family of transceivers have a $1/8^{\text{th}}$ unit load receiver input impedance of $96\text{k}\Omega$, allowing up to 256 transceivers to be connected in parallel on a communication line. Any combination of these devices and other RS-485 transceivers up to a total of 32 unit loads may be connected to the line.

LOW POWER SHUTDOWN MODE

Low-power shutdown mode is initiated by bringing both $\overline{\text{RE}}$ high and DE low simultaneously. While in shutdown devices draw less than $1\mu\text{A}$ of supply current. DE and $\overline{\text{RE}}$ may be tied together and driven by a single control signal. Devices are guaranteed not to enter shutdown if $\overline{\text{RE}}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts will enter shutdown.

Enable times t_{ZH} and t_{ZL} apply when the part is not in low-power shutdown state. Enable times $t_{\text{ZH(SHDN)}}$ and $t_{\text{ZL(SHDN)}}$ apply when the parts are shutdown. The drivers and receivers take longer to become enabled from low-power shutdown $t_{\text{ZH(SHDN)}}$ and $t_{\text{ZL(SHDN)}}$ than from driver / receiver disable mode (t_{ZH} and t_{ZL}).

FUNCTION TABLES

TABLE 1: FULL DUPLEX 14 PIN - XR3080X, XR3083X AND XR3086X

| TRANSMITTING | | | | |
|-----------------|----|----|----------|---|
| Inputs | | | Outputs | |
| \overline{RE} | DE | DI | Y | Z |
| X | 1 | 1 | 1 | 0 |
| X | 1 | 0 | 0 | 1 |
| 0 | 0 | X | High-Z | |
| 1 | 0 | X | Shutdown | |

TABLE 2: FULL DUPLEX 8 PIN - XR3081X, XR3084X AND XR3087X

| TRANSMITTING | | |
|--------------|---------|---|
| Input | Outputs | |
| DI | Y | Z |
| 1 | 1 | 0 |
| 0 | 0 | 1 |

TABLE 3: HALF DUPLEX 8 PIN - XR3082X, XR3085X AND XR3088X

| TRANSMITTING | | | | |
|-----------------|----|----|----------|---|
| Inputs | | | Outputs | |
| \overline{RE} | DE | DI | A | B |
| X | 1 | 1 | 1 | 0 |
| X | 1 | 0 | 0 | 1 |
| 0 | 0 | X | High-Z | |
| 1 | 0 | X | Shutdown | |

TABLE 4: FULL DUPLEX 14 PIN - XR3080X, XR3083X AND XR3086X

| RECEIVING | | | |
|-----------------|----|---------------|----------|
| Inputs | | | Ouput |
| \overline{RE} | DE | $V_A - V_B$ | RO |
| 0 | X | $\geq -50mV$ | 1 |
| 0 | X | $\leq -200mV$ | 0 |
| 0 | X | Open/Shorted | 1 |
| 1 | 1 | X | High-Z |
| 1 | 0 | X | Shutdown |

TABLE 5: FULL DUPLEX 8 PIN - XR3081X, XR3084X AND XR3087X

| RECEIVING | |
|---------------|--------|
| Inputs | Output |
| $V_A - V_B$ | RO |
| $\geq -50mV$ | 1 |
| $\leq -200mV$ | 0 |
| Open/Shorted | 1 |

TABLE 6: HALF DUPLEX 8 PIN - XR3082X, XR3085X AND XR3088X

| RECEIVING | | | |
|-----------------|----|---------------|----------|
| Inputs | | | Output |
| \overline{RE} | DE | $V_A - V_B$ | RO |
| 0 | X | $\geq -50mV$ | 1 |
| 0 | X | $\leq -200mV$ | 0 |
| 0 | X | Open/Shorted | 1 |
| 1 | 1 | X | High-Z |
| 1 | 0 | X | Shutdown |

Note: Receiver inputs $-200mV \leq V_A - V_B \leq -50mV$ are considered indeterminate.

PRODUCT SELECTOR GUIDE

TABLE 7: SELECTION GUIDE

| PART NUMBER | DUPLEX | DATA RATE | SHUTDOWN | RECEIVER AND DRIVER ENABLE | TRANS ON BUS | FOOTPRINT |
|-------------|--------|-----------|----------|----------------------------|--------------|-----------|
| XR3080XID-F | Full | 250kbps | Yes | Yes | 256 | SN75180 |
| XR3081XID-F | Full | | No | No | 256 | SN75179 |
| XR3082XID-F | Half | | Yes | Yes | 256 | SN75176 |
| XR3083XID-F | Full | 1Mbps | Yes | Yes | 256 | SN75180 |
| XR3084XID-F | Full | | No | No | 256 | SN75179 |
| XR3085XID-F | Half | | Yes | Yes | 256 | SN75176 |
| XR3086XID-F | Full | 20Mbps | Yes | Yes | 256 | SN75180 |
| XR3087XID-F | Full | | No | No | 256 | SN75179 |
| XR3088XID-F | Half | | Yes | Yes | 256 | SN75176 |

PACKAGE DRAWINGS

FIGURE 10. 8 NSOIC

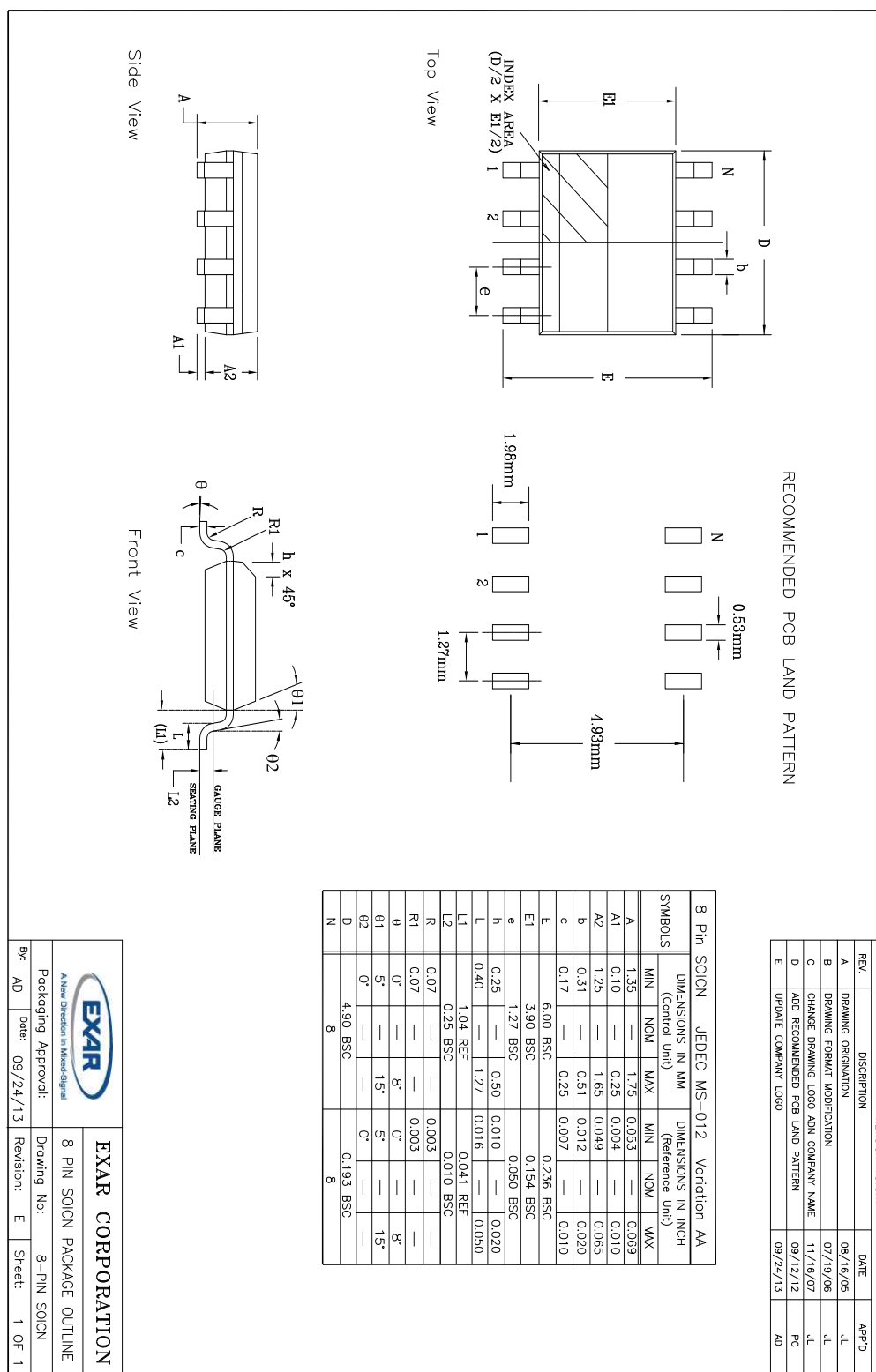
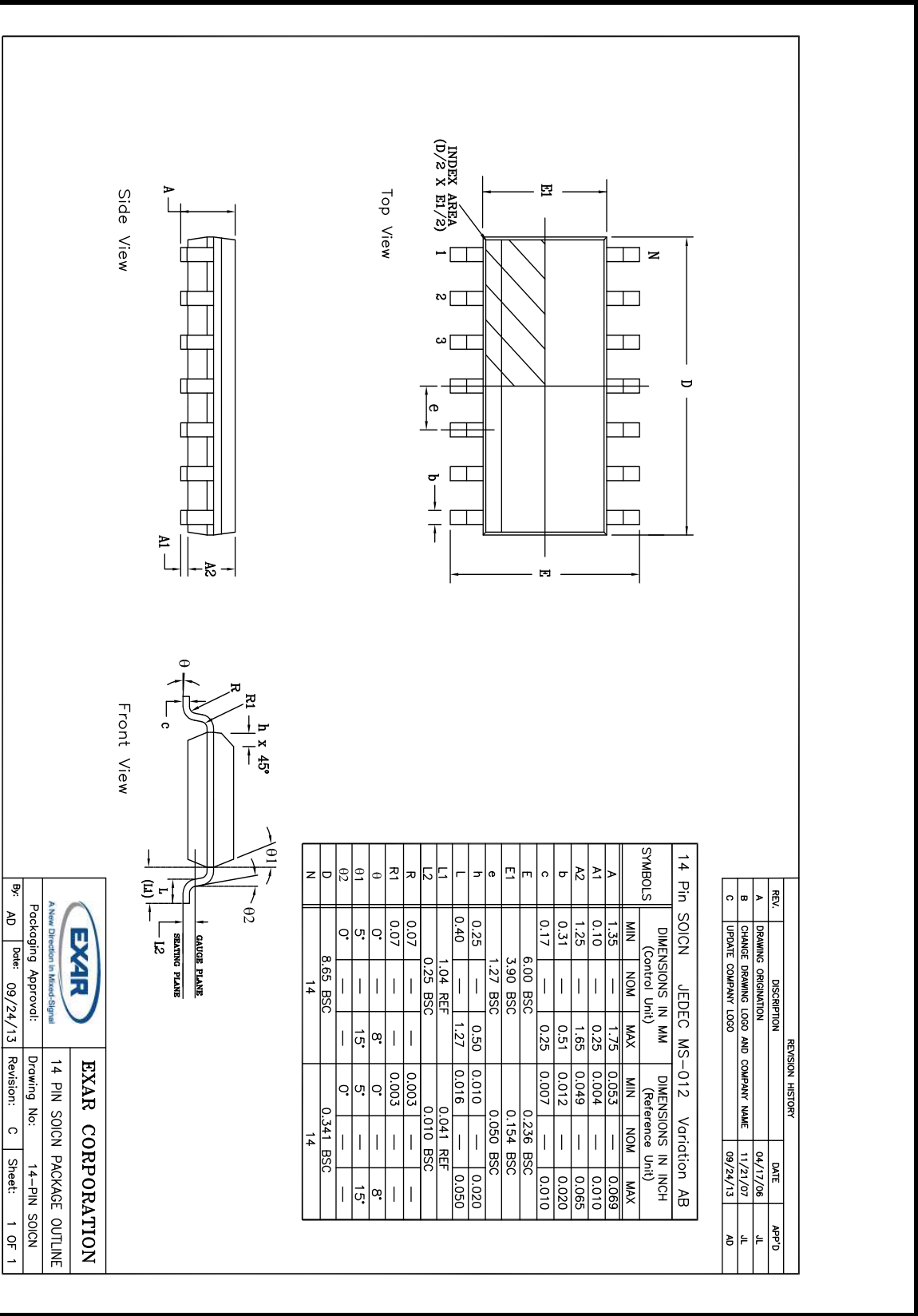


FIGURE 11. 14 NSOIC



REVISION HISTORY

| DATE | REVISION | DESCRIPTION |
|------------|----------|-------------------------|
| April 2013 | 1.0.0 | Production Release |
| Sept 2013 | 1.0.1 | Type formatting changes |

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