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1 Block diagram and pin description

Figure 1: Block diagram

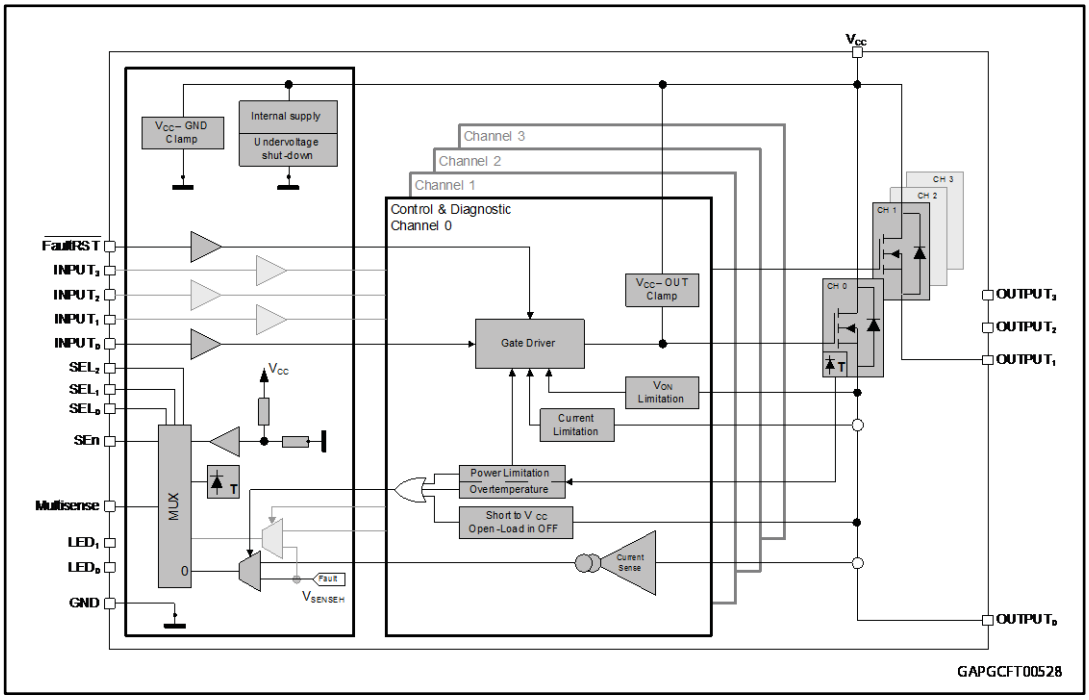


Table 1: Pin functions

Name	Function
V_{CC}	Battery connection.
$OUTPUT_{0,1,2,3}$	Power output.
GND	Ground connection.
$INPUT_{0,1,2,3}$	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. They control output switch state.
MultiSense	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the MultiSense diagnostic pin
$LED_{0,1}$	Active high compatible with 3 V and 5 V CMOS outputs pin; they enable the LED mode on logic high level (see *Table 15: "Truth table"*).
$SEL_{0,1,2}$	Active high compatible with 3 V and 5 V CMOS outputs pin; they address the MultiSense multiplexer (see *Table 15: "Truth table"*).
FaultRST	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode.

Figure 2: Configuration diagram (top view)

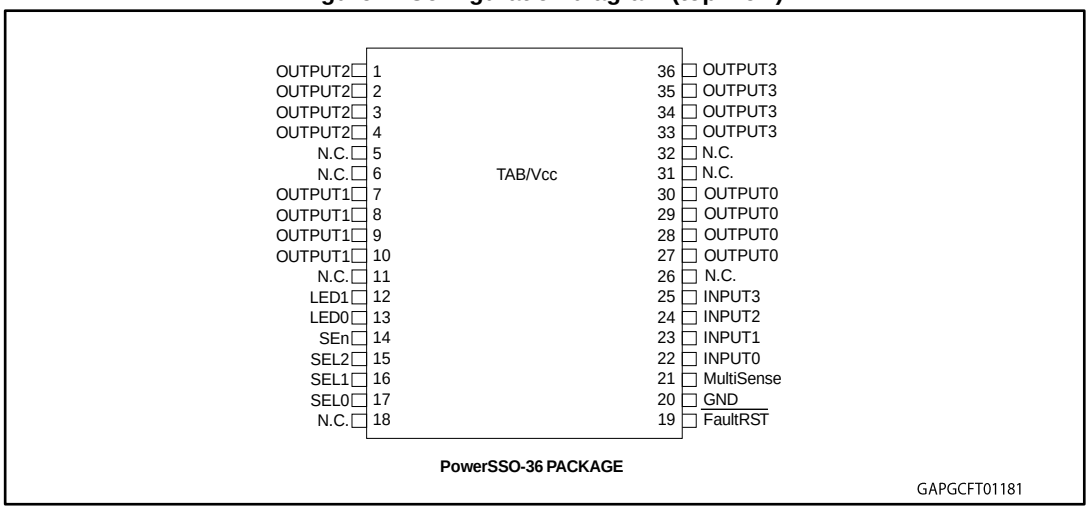


Table 2: Suggested connections for unused and not connected pins

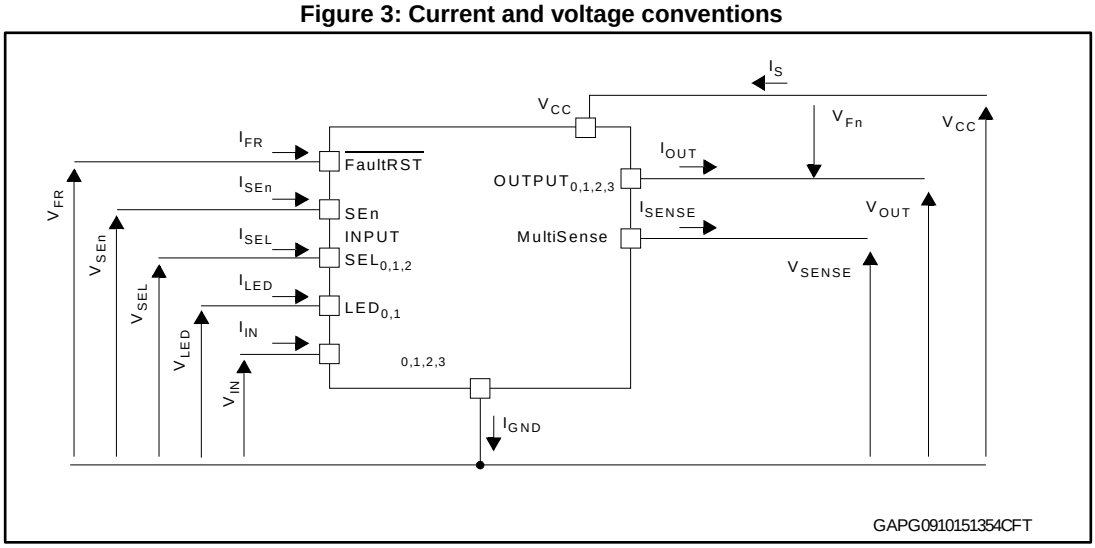
Connection / pin	MultiSense	N.C.	Output	Input	SEn, SELx, LEDx, FaultRST
Floating	Not allowed	X (1)	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

Notes:

(1)X: do not care.

2 Electrical specification

Figure 3: Current and voltage conventions



$V_{Fn} = V_{OUTn} - V_{CC}$

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3: "Absolute maximum ratings"* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the table below for extended periods may affect device reliability.

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	16	
V_{CCPK}	Maximum transient supply voltage (ISO7637-2:2004 Pulse 5b level IV clamped to 40 V; R_L = 4 Ω)	40	
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	$OUTPUT_{0,1,2,3}$ DC output current	Internally limited	A
$-I_{OUT\_0,1}$	$OUTPUT_{0,1}$ Reverse DC output current	10	
$-I_{OUT\_2,3}$	$OUTPUT_{2,3}$ Reverse DC output current	10	
I_{IN}	$INPUT_{0,1,2,3}$ DC input current	-1 to 10	mA
I_{LED}	$LED_{0,1}$ DC input current		
I_{SEn}	SEn DC input current		
I_{SEL}	$SEL_{0,1,2}$ DC input current		

Symbol	Parameter	Value	Unit
I_{FR}	FaultRST DC input current	-1 to 10	mA
V_{FR}	FaultRST DC input voltage	7.5	V
I_{SENSE}	MultiSense pin DC output current (V_{GND} = V_{CC} and V_{SENSE} < 0 V)	-10	mA
	MultiSense pin DC output current in reverse (V_{CC} < 0 V)	20	mA
E_{MAX}	Maximum switching energy (single pulse) (T_{DEMAG} = 0.4 ms; T_{jstart} = 150 °C)	36	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F) • $INPUT_{0,1,2,3}$ • MultiSense • $LED_{0,1}$, SEn, $SEL_{0,1,2}$, $\overline{FaultRST}$ • $OUTPUT_{0,1,2,3}$ • V_{CC}	 4000 2000 4000 4000 4000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4: Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj\text{-}board}$	Thermal resistance junction-board (JEDEC JESD 51-8) (1)(2)	4.9	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-2) (1)(3)	53	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-2) (1)(2)	18.5	

Notes:

(1)One channel ON.

(2)Device mounted on four-layers 2s2p PCB

(3)Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace

2.3 Electrical characteristics

7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

2.3.1 General electrical specification

Table 5: Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	
$V_{USDReset}$	Undervoltage shutdown reset				5	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		
V_{clamp}	Clamp voltage	I_S = 20 mA; 25 °C < T_j < 150 °C	41	46	52	V
		I_S = 20 mA; T_j = -40 °C	38			V
I_{STBY}	Supply current in standby at V_{CC} = 13 V (1)	V_{CC} = 13 V; V_{INx} = V_{OUTx} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1,2}$ = 0 V; $V_{LED0,1}$ = 0 V; T_j = 25 °C			0.5	µA
		V_{CC} = 13 V; V_{INx} = V_{OUTx} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1,2}$ = 0 V; $V_{LED0,1}$ = 0 V; T_j = 85 °C (2)			0.5	µA
		V_{CC} = 13 V; V_{INx} = V_{OUTx} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1,2}$ = 0 V; $V_{LED0,1}$ = 0 V; T_j = 125 °C			3	µA
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V; V_{INx} = V_{OUTx} = V_{FR} = 0 V; $V_{SEL0,1,2}$ = 0 V; $V_{LED0,1}$ = 0 V; V_{SEn} = 5 V to 0 V	60	300	550	µs
$I_{S(ON)}$	Supply current	V_{CC} = 13 V; V_{SEn} = V_{FR} = $V_{SEL0,1}$ = 0 V; V_{INx} = 5 V; $I_{OUT0,1,2,3}$ = 0 A		10	16	mA
$I_{GND(ON)}$	Control stage current consumption in ON state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; V_{FR} = $V_{SEL0,1}$ = 0 V; V_{INx} = 5 V; $I_{OUT0,1,2,3}$ = 2.5 A			18.5	mA
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V(1)	V_{INx} = V_{OUTx} = 0 V; V_{CC} = 13 V; T_j = 25 °C	0	0.01	0.5	µA
		V_{INx} = V_{OUTx} = 0 V; V_{CC} = 13 V; T_j = 125 °C	0		3	
V_F	Output - V_{CC} diode voltage (3)	I_{OUT} = -2.5 A; T_j = 150 °C			0.7	V

Notes:

(1)PowerMOS leakage included.

(2)Parameter specified by design; not subject to production test.

(3)For each channel.

Table 6: Logic Inputs

7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$INPUT_{0,1,2,3}$ characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
FaultRST characteristics						
V_{FRL}	Input low level voltage				0.9	V
I_{FRL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{FRH}	Input high level voltage		2.1			V
I_{FRH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{FR(hyst)}$	Input hysteresis voltage		0.2			V
V_{FRCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.7		
$SEL_{0,1,2}$ characteristics (7 V < V_{CC} < 18 V)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SELH}	Input high level voltage		2.1			V
I_{SELH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEL(hyst)}$	Input hysteresis voltage		0.2			V
V_{SELCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
$LED_{0,1}$ characteristics (7 V < V_{CC} < 18 V)						
V_{LEDL}	Input low level voltage				0.9	V
I_{LEDL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{LEDH}	Input high level voltage		2.1			V
I_{LEDH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{LED(hyst)}$	Input hysteresis voltage		0.2			V
V_{LEDCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA

7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		

Table 7: Protections

7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature *(1)*		T_{RS} + 1	T_{RS} + 5		
T_{RS}	Thermal reset of fault diagnostic indication	V_{FR} = 0 V; V_{SEn} =5 V	135			
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)*(1)*			5		
ΔT_{J_SD}	Dynamic temperature			60		K
t_{LATCH_RST}	Fault reset time for output unlatch*(1)*	V_{FR} = 5 V to 0 V; V_{SEn} = 5 V; V_{INx} = 5 V; $V_{SEL0,1,2}$ = 0 V	3	10	20	µs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT}= 2 A; L = 6 mH; T_j = -40 °C	V_{CC} - 38			V
		I_{OUT}= 2 A; L = 6 mH; T_j = 25 °C to 150 °C	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT}= 0.25 A		20		mV

Notes:

(1)Parameter guaranteed by design and characterization; not subject to production test.

Table 8: MultiSense

7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{SENSE_CL}	MultiSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		V
Current Sense characteristics						
I_{SENSE0}	MultiSense leakage current	MultiSense disabled: V_{SEn} = 0 V;	0		0.5	µA
		MultiSense disabled: (1) -1 V < V_{SENSE} < 5 V	-0.5		0.5	
		MultiSense enabled: V_{SEn} = 5 V All channels ON; I_{OUTX} = 0 A; Ch_X diagnostic selected; • E.g. Ch_0: V_{IN0} = 5 V; $V_{IN1,2,3}$ = 5 V; $V_{SEL0,1,2}$ = 0 V; I_{OUT0} = 0 A; $I_{OUT1,2,3}$ = 2.5 A	0		2	
		MultiSense enabled: V_{SEn} = 5 V Ch_X OFF; Ch_X diagnostic selected: • E.g. Ch_0: V_{IN0} = 0 V; $V_{IN1,2,3}$ = 5 V; $V_{SEL0,1,2}$ = 0 V; I_{OUT0} = 0 A; $I_{OUT1,2,3}$ = 2.5 A	0		2	
V_{OUT_MSD} (1)	Output Voltage for MultiSense shutdown	V_{SEn} = 5 V; R_{SENSE} = 2.7 kΩ • E.g. Ch_0: V_{IN0} = 5 V; $V_{SEL0,1,2}$ = 0 V; I_{OUT0} = 2.5 A		5		V
V_{SENSE_SAT}	Multisense saturation voltage	V_{CC} = 7 V; R_{SENSE} = 2.7 K; V_{SEn} = 5 V; V_{IN0} = 5 V; $V_{SEL0,1,2}$ = 0 V; I_{OUT0} = 4.5 A; T_j = 150°C	5			V
I_{SENSE_SAT} (1)	CS saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN0} = 5 V; V_{SEn} = 5 V; $V_{SEL0,1,2}$ = 0 V; T_j = 150°C	4			mA
$I_{OUT\_SAT\_BULB}$ (1)	Output saturation current in BULB mode	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN0} = 5 V; V_{SEn} = 5 V; $V_{SEL0,1,2}$ = 0 V; T_j = 150°C	8			A
$I_{OUT\_SAT\_LED}$ (1)	Output saturation current in LED mode	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN0} = 5 V; V_{SEn} = 5 V; $V_{SEL0,1,2}$ = 0 V; T_j = 150°C	2.3			A
OFF-state diagnostic						
V_{OL}	OFF state open load voltage detection threshold	V_{SEn} = 5V; Ch_X OFF; Ch_X diagnostic selected • E.g. Ch_0: V_{IN0} = 0 V; $V_{SEL0,1,2}$ = 0 V	2	3	4	V

7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$I_{L(off2)}$	OFF state output sink current	V_{IN} = 0 V; V_{OUT} = V_{OL}; T_j = -40°C to 125°C	-100		-15	µA
t_{DSTKON}	OFF state diagnostic delay time from falling edge of INPUT (see *Figure 4: "Switching times and Pulse skew"*)	V_{SEn} = 5 V; Ch_X ON to OFF transition; Ch_X diagnostic selected • E.g. Ch_0: V_{IN0} = 5 V to 0 V; $V_{SEL0,1,2}$ = 0 V; V_{OUT0} > 4 V	100	350	700	µs
$t_{D\_OL\_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V_{INx} = 0 V; V_{FR} = 0 V; $V_{SEL0,1,2}$ = 0 V; V_{OUT0} = 4 V; V_{SEn} = 0 V to 5 V			60	µs
t_{D_VOL}	OFF state diagnostic delay time from rising edge of V_{OUT}	V_{SEn} = 5V; Ch_X OFF; Ch_X diagnostic selected • E.g. Ch_0: V_{IN0} = 0 V; $V_{SEL0,1,2}$ = 0 V; V_{OUT0} = 0 V to 4 V		5	30	µs
Chip temperature analog feedback						
V_{SENSE_TC}	MultiSense output voltage proportional to chip temperature	V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{SEL2} = 5 V; R_{SENSE} = 1 kΩ; V_{INx} = 0 V; T_j = -40°C	2.325	2.41	2.495	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{SEL2} = 5 V; R_{SENSE} = 1 kΩ; V_{INx} = 0 V; T_j = 25°C	1.985	2.07	2.155	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{SEL2} = 5 V; R_{SENSE} = 1 kΩ; V_{INx} = 0 V; T_j = 125°C	1.435	1.52	1.605	V
dV_{SENSE_TC}/dT *(2)*	Temperature coefficient	T_j = -40°C to 150°C		-5.5		mV/K
Transfer function		V_{SENSE_TC} (T) = V_{SENSE_TC} (T_0) + dV_{SENSE_TC}/dT * (T-T_0)				
V_{CC} supply voltage analog feedback						
V_{SENSE_VCC}	MultiSense output voltage proportional to V_{CC} supply voltage	V_{CC} = 13 V; V_{SEn} = 5 V; $V_{SEL0,1,2}$ = 5 V; V_{INx} = 0 V; R_{SENSE} = 1 kΩ	3.16	3.23	3.3	V
Transfer function *(2)*		V_{SENSE_VCC} = V_{CC} / 4				
Fault diagnostic feedback (see *Table 15: "Truth table"*)						
V_{SENSEH}	MultiSense output voltage in fault condition	V_{CC} = 13 V; R_{SENSE} = 1 kΩ	5		6.6	V

7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{SENSEH}	MultiSense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V	7	20	30	mA
MultiSense timings (Chip Temperature Sense mode - see *Figure 6: "Multisense timings (chip temperature and VCC sense mode)"*)						
$t_{DSENSE3H}$	V_{SENSE_TC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = V_{SEL1} = 0 V; V_{SEL2} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE3L}$	V_{SENSE_TC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = V_{SEL1} = 0 V; V_{SEL2} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (V_{CC} Voltage Sense mode - see *Figure 6: "Multisense timings (chip temperature and VCC sense mode)"*)						
$t_{DSENSE4H}$	V_{SENSE_VCC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = V_{SEL1} = V_{SEL2} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE4L}$	V_{SENSE_VCC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = V_{SEL1} = V_{SEL2} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense Timings (Multiplexer transition times) *(3)*						
t_{D_XtoY}	MultiSense transition delay from Ch_X to Ch_Y	V_{IN2} = 5 V; V_{IN3} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V to 5 V; V_{SEL1} = 5 V; V_{SEL2} = 0 V; I_{OUT2} = 0 A; I_{OUT3} = 2.5 A; R_{SENSE} = 1 kΩ			20	µs
t_{D_CStoTC}	MultiSense transition delay from current sense to T_C sense	V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = V_{SEL2} = 0 V to 5 V; I_{OUT0} = 1.25 A; R_{SENSE} = 1 kΩ			60	µs
t_{D_TCtoCS}	MultiSense transition delay fromT_C sense to current sense	V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = V_{SEL2} = 5 V to 0 V; I_{OUT0} = 1.25 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_CStoVCC}$	MultiSense transition delay from current sense to V_{CC} sense	V_{IN2} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; V_{SEL2} = 0 V to 5 V; I_{OUT2} = 1.25 A; R_{SENSE} = 1 kΩ			60	µs
$t_{D\_VCCtoCS}$	MultiSense transition delay from V_{CC} sense to current sense	V_{IN2} = 5 V; V_{SEn} = 5 V; V_{SEL1} = 5 V; V_{SEL0} = V_{SEL2} = 5 V to 0 V; I_{OUT2} = 1.25 A; R_{SENSE} = 1 kΩ			20	µs

7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$t_{D\_TCtoVCC}$	MultiSense transition delay from T_C sense to V_{CC} sense	V_{SEn} = 5 V; $V_{SEL1,2}$ = 5 V; V_{SEL0} = 0 V to 5 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_VCCtoTC}$	MultiSense transition delay from V_{CC} sense to T_C sense	V_{SEn} = 5 V; $V_{SEL1,2}$ = 5 V; V_{SEL0} = 5 V to 0 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_CStoVSENSEH}$	MultiSense transition delay from stable current sense on Ch_X to V_{SENSEH} on Ch_Y	V_{IN0} = 5 V; V_{IN1} = 0 V; V_{OUT1} > 4 V; V_{SEn} = 5 V; V_{SEL2} = 0 V; V_{SEL1} = 0 V; V_{SEL0} = 0 V to 5 V; I_{OUT0} = 2.5 A; R_{SENSE} = 1 kΩ			60	µs

Notes:

(1)Parameter guaranteed by design and characterization; not subject to production test.

(2)V_{CC} sensing and T_C sensing are referred to GND potential.

(3)Transition delay is measured up to +/- 10% of final conditions.

Figure 4: Switching times and Pulse skew

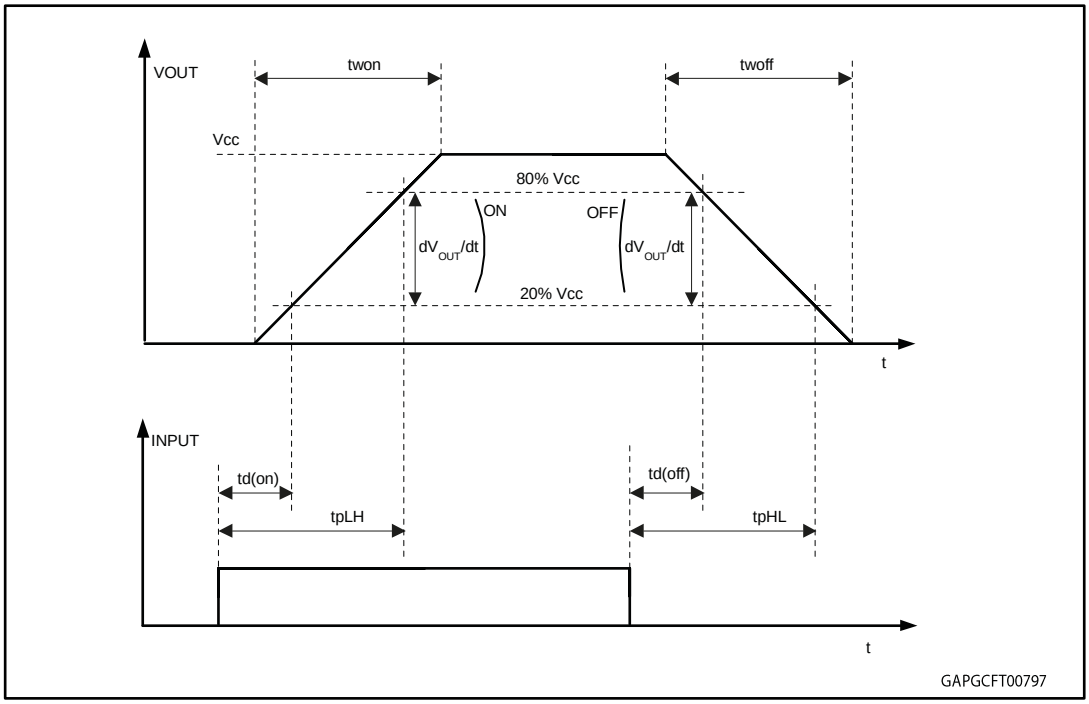


Figure 5: MultiSense timings (current sense mode)

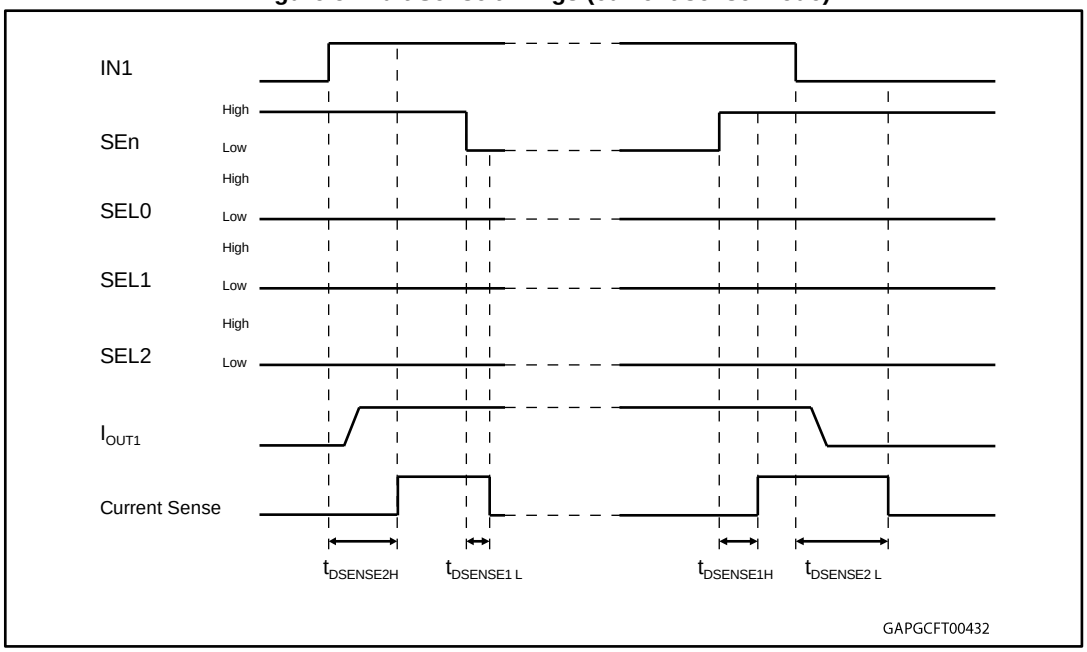


Figure 6: Multisense timings (chip temperature and VCC sense mode)

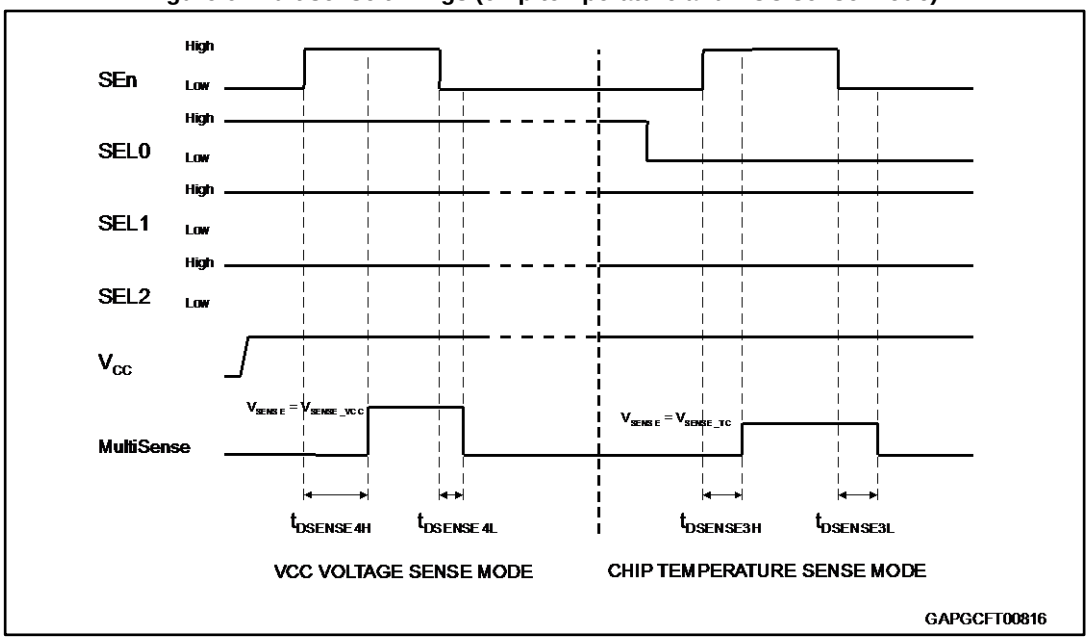
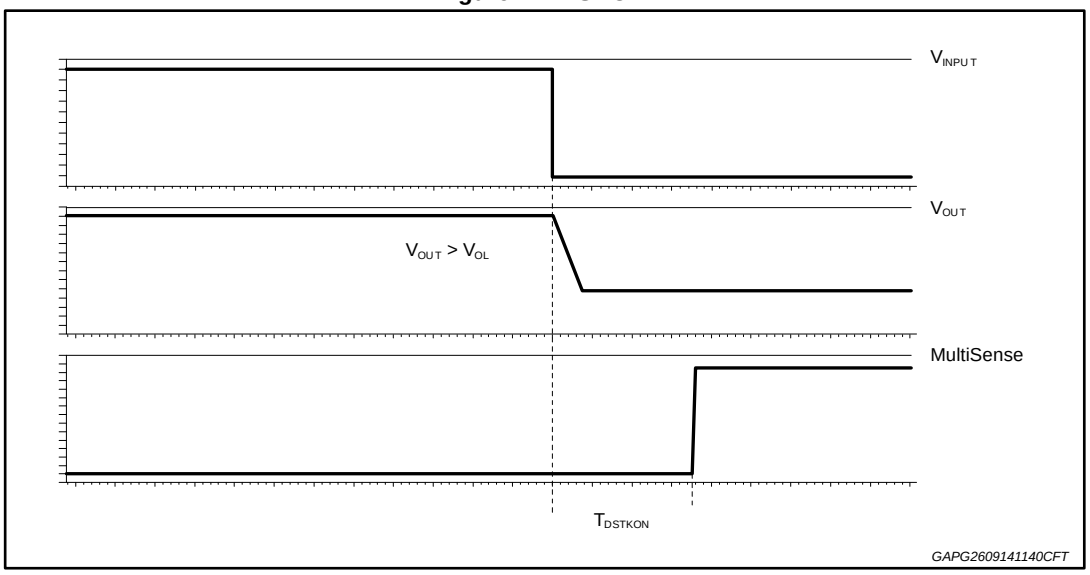


Figure 7: TDSKON



2.3.2 Bulb mode (default)

Table 9: Power section in Bulb Mode

7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$R_{ON\_0,1,2,3\_BULB}$	On-state resistance in Bulb Mode Ch0, Ch1, Ch2 and Ch3	I_{OUT} = 2.5 A; T_j = 25°C		40		mΩ
		I_{OUT} = 2.5 A; T_j = 150°C			80	
		I_{OUT} = 2.5 A; V_{CC} = 4 V; T_j = 25°C			60	
$R_{ON\_REV\_0,1,2,3}$	On-state resistance in Reverse Battery Ch0, Ch1, Ch2 and Ch3	V_{CC} = -13V; I_{OUT} = -2.5A; T_j = 25°C		40		mΩ
$I_{LIMH\_0,1,2,3\_BULB}$ (1)	DC short circuit current in Bulb Mode Ch0, Ch1, Ch2 and Ch3	V_{CC} = 13 V	24	34	48	A
		4 V < V_{CC} < 18 V (2)			48	
$I_{LIML\_0,1,2,3\_BULB}$	Short circuit current during thermal cycling in Bulb Mode Ch0, Ch1, Ch2 and Ch3	V_{CC} = 13 V; T_R < T_j < T_{TSD}		9		
$V_{ON\_0,1,2,3\_BULB}$	Output voltage drop limitation in Bulb Mode Ch0, Ch1, Ch2 and Ch3	I_{OUT} = 0.25 A		20		mV

Notes:

(1)Parameter guaranteed by an indirect test sequence.

(2)Parameter guaranteed by design and characterization; not subject to production test.

Table 10: Switching in Bulb Mode

V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Channel 0, 1, 2 and 3						
$t_{d(on)\_0,1,2,3}$ (1)	Turn-on delay time at T_j = 25 °C	R_L = 5.2 Ω	10	60	145	µs
$t_{d(off)\_0,1,2,3}$ (1)	Turn-off delay time at T_j = 25 °C	R_L = 5.2 Ω	10	50	100	
$(dV_{OUT}/dt)_{on\_0,1,2,3}$ (1)	Turn-on voltage slope at T_j = 25 °C	R_L = 5.2 Ω	0.1	0.5	0.7	V/µs
$(dV_{OUT}/dt)_{off\_0,1,2,3}$ (1)	Turn-off voltage slope at T_j = 25 °C	R_L = 5.2 Ω	0.1	0.5	0.7	
$W_{ON\_0,1,2,3}$	Switching energy losses at turn-on (t_{won})	R_L = 5.2 Ω	—	0.2	0.52 (2)	mJ
$W_{OFF\_0,1,2,3}$	Switching energy losses at turn-off (t_{woff})	R_L = 5.2 Ω	—	0.2	0.5 (2)	mJ
$t_{SKEW\_0,1,2,3}$ (1)	Differential pulse skew (t_{PHL} - t_{PLH})	R_L = 5.2 Ω	-100	-15	35	µs

Notes:

(1)See *Figure 4: "Switching times and Pulse skew"*.

(2)Parameter guaranteed by design and characterization, not subject to production test.

Table 11: MultiSense in Bulb Mode

7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Current sense characteristics						
Channel 0, 1, 2 and 3						
$K_{OL\_CH0,1\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 10 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	430			
$K_{OL\_CH2,3\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 10 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	430			
dK_{cal}/K_{cal} (1)(2)	Current sense ratio drift at calibration point	I_{CAL} = 30 mA; I_{OUT} = 10 mA to 50 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-35		35	%
$K_{LED\_CH0,1\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.05 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	720	1440	2160	
$K_{LED\_CH2,3\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.05 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	720	1440	2160	

7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$K_{0\_CH0,1\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.25 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	930	1550	2170	
$K_{0\_CH2,3\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.25 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	930	1550	2170	
dK_0/K_0 (1)(2)	Current sense ratio drift	I_{OUT} = 0.25 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-20		20	%
$K_{1\_CH0,1\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	1110	1590	2070	
$K_{1\_CH2,3\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	1085	1550	2015	
dK_1/K_1 (1)(2)	Current sense ratio drift	I_{OUT} = 0.5 A; V_{SENSE} = 4V; V_{SEn} = 5 V	-15		15	%
$K_{2\_CH0,1\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 2 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	1160	1450	1740	
$K_{2\_CH2,3\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 2 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	1130	1410	1690	
dK_2/K_2 (1)(2)	Current sense ratio drift	I_{OUT} = 2 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-10		10	%
$K_{3\_CH0,1\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 6 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	1295	1440	1585	
$K_{3\_CH2,3\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 6 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	1260	1400	1540	
dK_3/K_3 (1)(2)	Current sense ratio drift	I_{OUT} = 6 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-5		5	%
MultiSense timings (Current Sense mode see *Figure 5: "MultiSense timings (current sense mode)"*)						
Channel 0, 1, 2 and 3						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 5.2 Ω			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 5.2 Ω		5	20	µs

7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 5.2 Ω		100	250	µs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 5.2 Ω			100	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 5.2 Ω		50	250	µs

Notes:

(1)Parameter specified by design; not subject to production test.

(2)All values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

Figure 8: Bulb Mode - IOUT/ISENSE versus IOUT

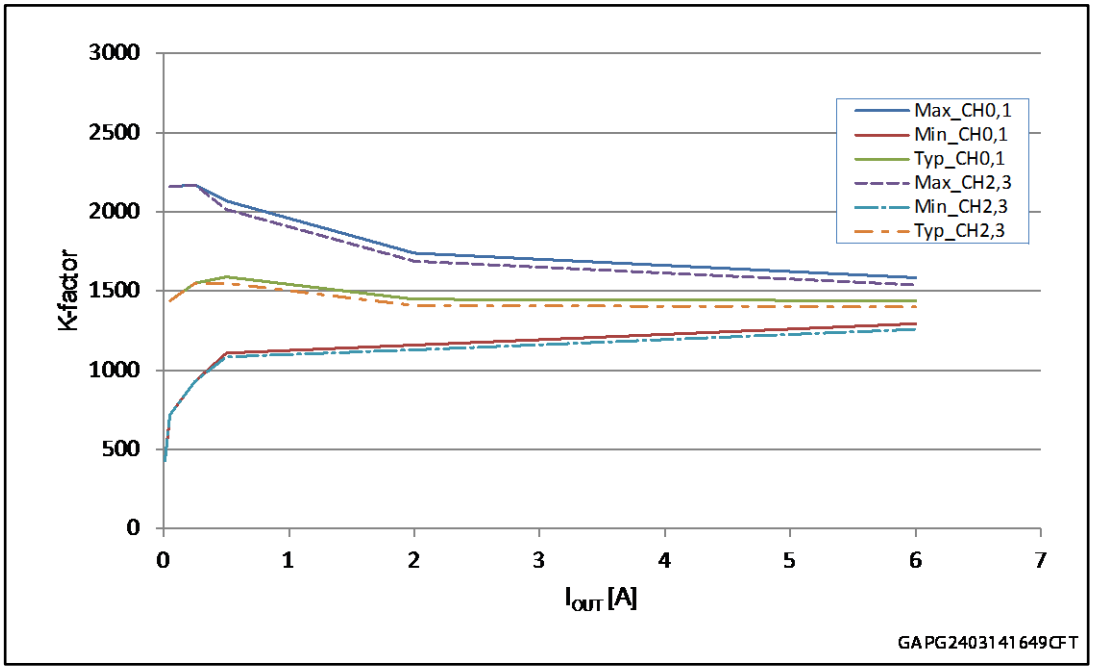
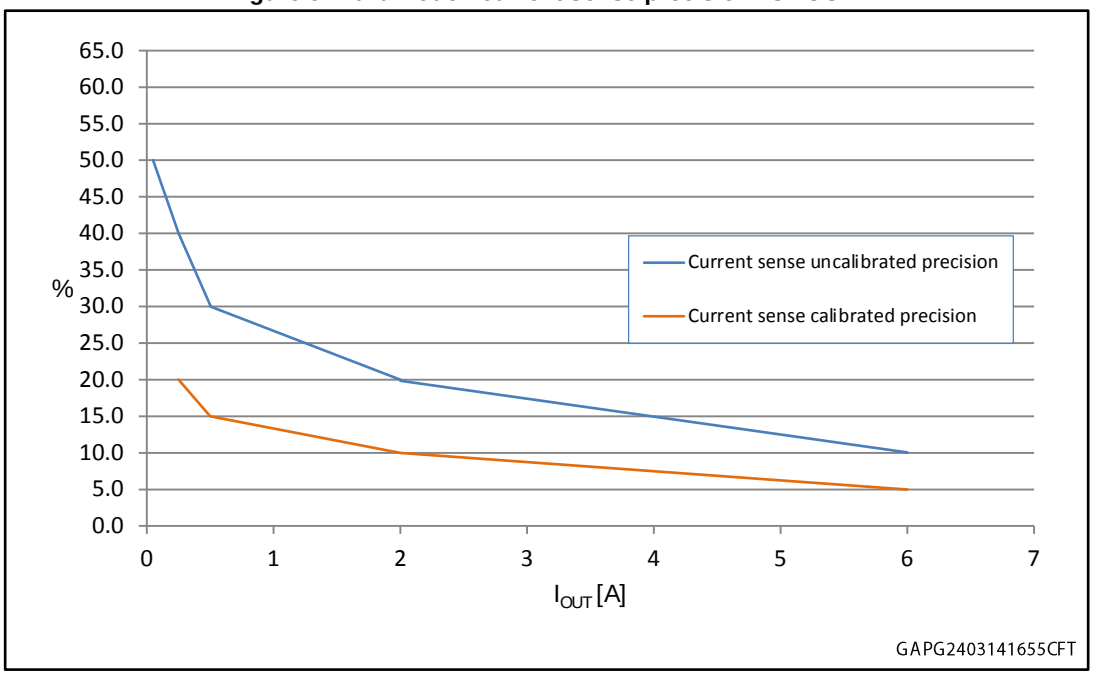


Figure 9: Bulb Mode - current sense precision vs. IOUT



2.3.3 Electrical characteristics curves - Bulb Mode

Figure 10: OFF-state output current

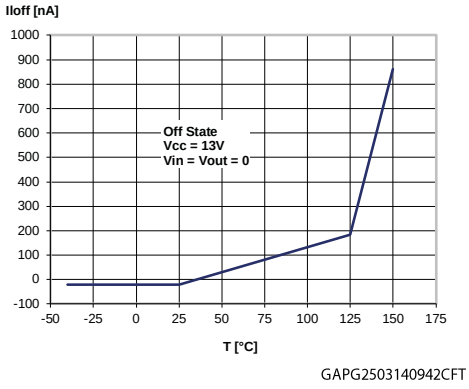


Figure 11: Standby current

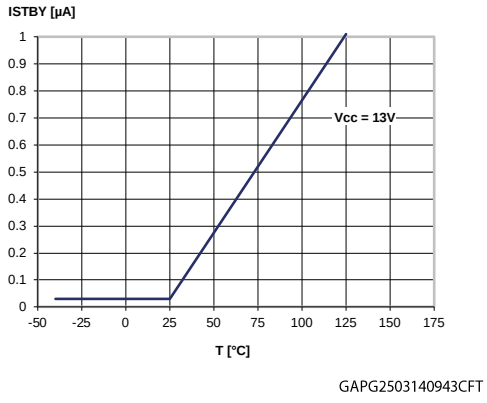


Figure 12: IGND(ON) vs. Iout

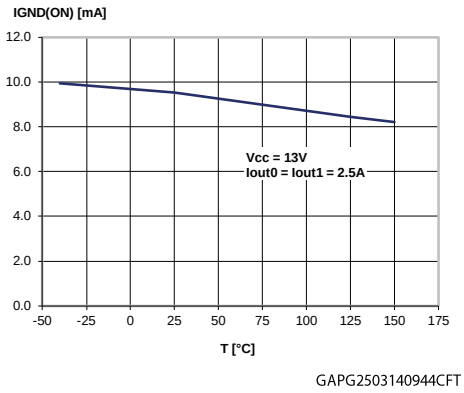


Figure 13: Logic Input high level voltage

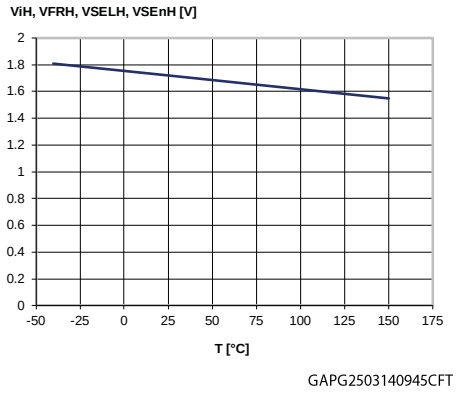


Figure 14: Logic Input low level voltage

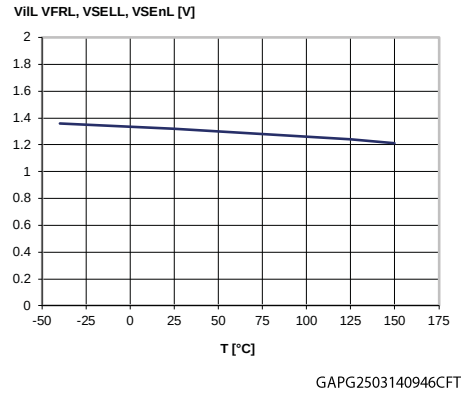


Figure 15: High level logic input current

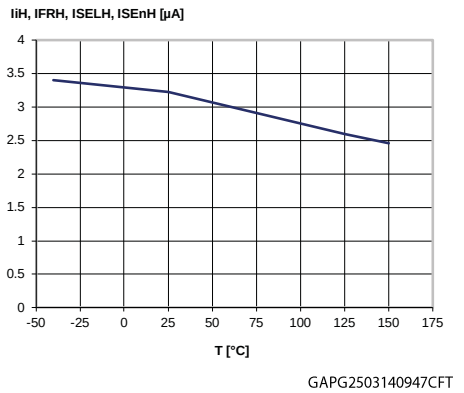


Figure 16: Low level logic input current

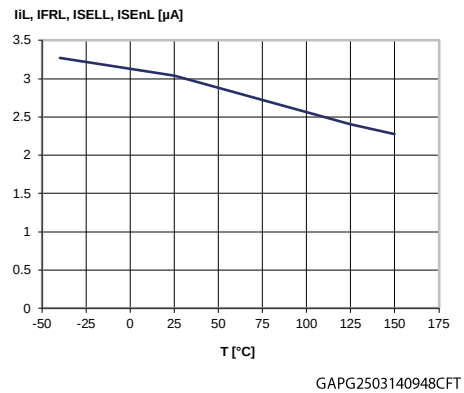


Figure 17: Logic Input hysteresis voltage

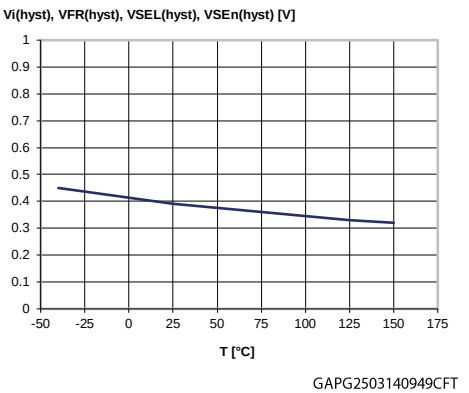


Figure 18: FaultRST Input clamp voltage

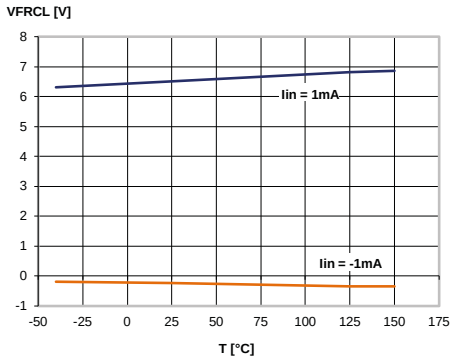


Figure 19: Undervoltage shutdown

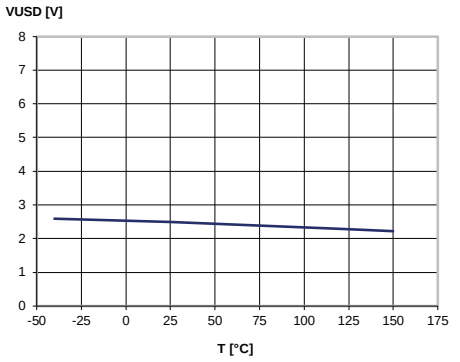


Figure 20: On-state resistance vs. Tcase

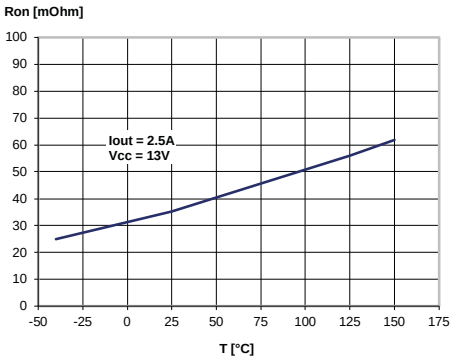


Figure 21: On-state resistance vs. VCC

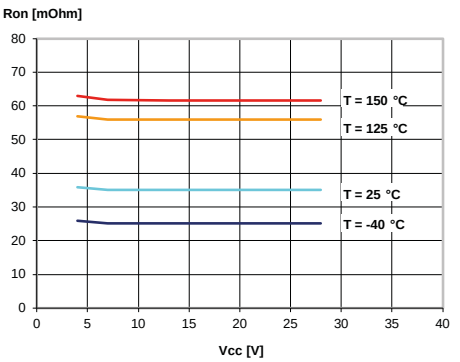


Figure 22: Turn-on voltage slope

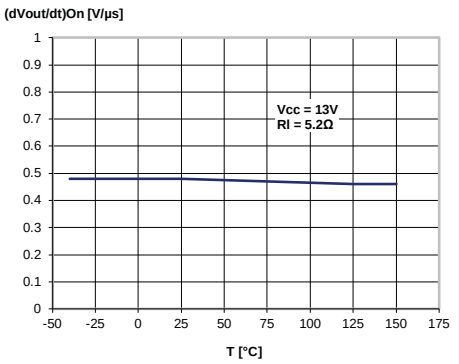


Figure 23: Turn-off voltage slope

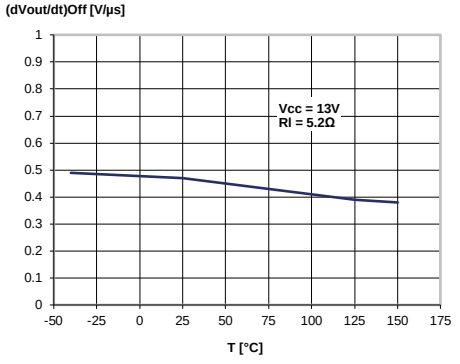
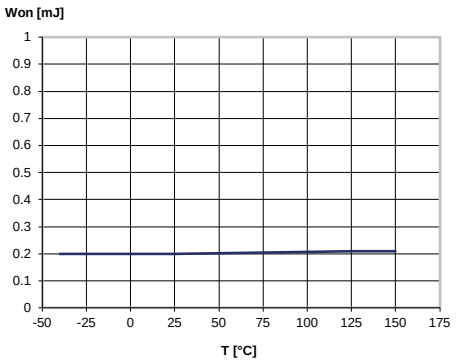
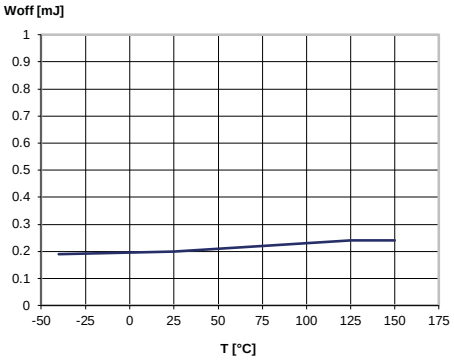


Figure 24: Won vs. Tcase



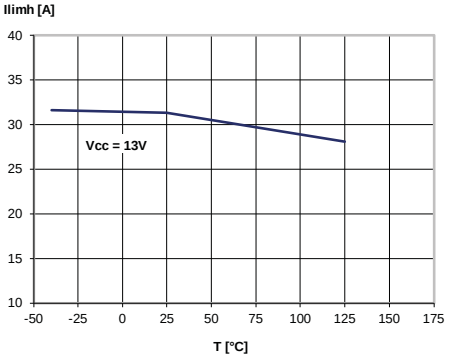
GAPG2503141122CFT

Figure 25: Woff vs. Tcase



GAPG2503141123CFT

Figure 26: ILIMH vs. Tcase



GAPG2503141124CFT

Figure 27: OFF-state open-load voltage detection threshold

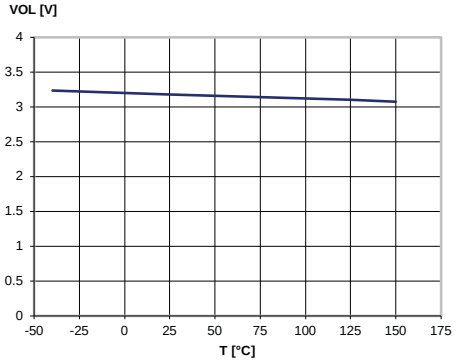


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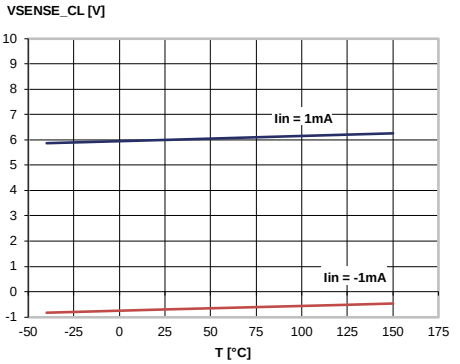
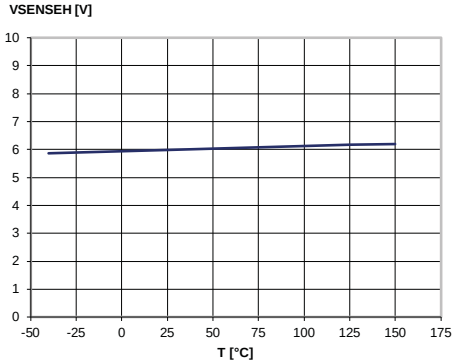
Figure 28: Vsense clamp vs. Tcase



GAPG2503141126CFT

Figure 29: Vsenseh vs. Tcase



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2.3.4 LED Mode (Channel 0 and 1)

Table 12: Switching in LED Mode

V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$t_{d(on)\_0,1\_LED}$ (1)	Turn-on delay time at T_j = 25 °C	R_L = 22.8 Ω	10	65	145	µs
$t_{d(off)\_0,1\_LED}$ (1)	Turn-off delay time at T_j = 25 °C	R_L = 22.8 Ω	10	40	100	
$(dV_{OUT}/dt)_{on\_0,1\_LED}$ (1)	Turn-on voltage slope at T_j = 25 °C	R_L = 22.8 Ω	0.2	0.5	0.8	V/µs
$(dV_{OUT}/dt)_{off\_0,1\_LED}$ (1)	Turn-off voltage slope at T_j = 25 °C	R_L = 22.8 Ω	0.1	0.5	0.7	
$W_{ON\_0,1\_LED}$	Switching energy losses at turn-on (t_{won})	R_L = 22.8 Ω	—	0.04	0.1 (2)	mJ
$W_{OFF\_0,1\_LED}$	Switching energy losses at turn-off (t_{woff})	R_L = 22.8 Ω	—	0.045	0.11 (2)	mJ
$t_{SKEW\_0,1\_LED}$ (1)	Differential Pulse skew (t_{PHL} - t_{PLH})	R_L = 22.8 Ω	-100	-25	25	µs

Notes:

(1)See *Figure 4: "Switching times and Pulse skew"*.

(2)Parameter guaranteed by design and characterization, not subject to production test.

Table 13: Power section in LED Mode

7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$R_{ON\_0,1\_LED}$	On-state resistance in LED Mode Ch0 and Ch1	I_{OUT} = 0.57 A; T_j = 25°C		140		mΩ
		I_{OUT} = 0.57 A; T_j = 150°C			280	
		I_{OUT} = 0.57 A; V_{CC} = 5 V; T_j = 25°C			210	
$I_{LIMH\_0,1\_LED}$ (1)	DC short circuit current in Bulb Mode Ch0 and Ch1	V_{CC} = 13 V	5.5	8	11	A
		4 V < V_{CC} < 18 V (2)				
$I_{LIML\_0,1\_LED}$	Short circuit current during thermal cycling in Bulb Mode Ch0 and Ch1	V_{CC} = 13 V; T_R < T_j < T_{TSD}		2		
$V_{ON\_0,1\_LED}$	Output voltage drop limitation in LED Mode Ch0 and Ch1	I_{OUT} = 0.07 A		20		mV

Notes:

(1)Parameter guaranteed by an indirect test sequence.

(2)Parameter guaranteed by design and characterization; not subject to production test.

Table 14: MultiSense in LED Mode

7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
K_{OL}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.01 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	120			
dK_{cal}/K_{cal} (1)(2)	Current sense ratio drift at calibration point	I_{cal} = 17.5 mA; I_{OUT} = 10 mA to 25 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-30		30	%
K_{LED}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.025 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	150	380	610	
dK_{LED}/K_{LED} (1)(2)	Current sense ratio drift	I_{OUT} = 0.025 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-25		25	%
$K_{0\_CH0,1\_L}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.15 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	240	405	570	
dK_0/K_0 (1)(2)	Current sense ratio drift	I_{OUT} = 0.15 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-15		15	%
$K_{1\_CH0,1\_L}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.7 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	300	380	460	
dK_1/K_1 (1)(2)	Current sense ratio drift	I_{OUT} = 0.7 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-8		8	%
MultiSense timings (Current Sense mode - see *Figure 5: "MultiSense timings (current sense mode)"*)						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 22.8 Ω			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 22.8 Ω		5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 22.8 Ω			250	µs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 22.8 Ω			100	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 22.8 Ω		50	250	µs

Notes:

(1)Parameter specified by design; not subject to production test.

(2)All values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

Figure 30: LED Mode - IOUT/ISENSE versus IOUT

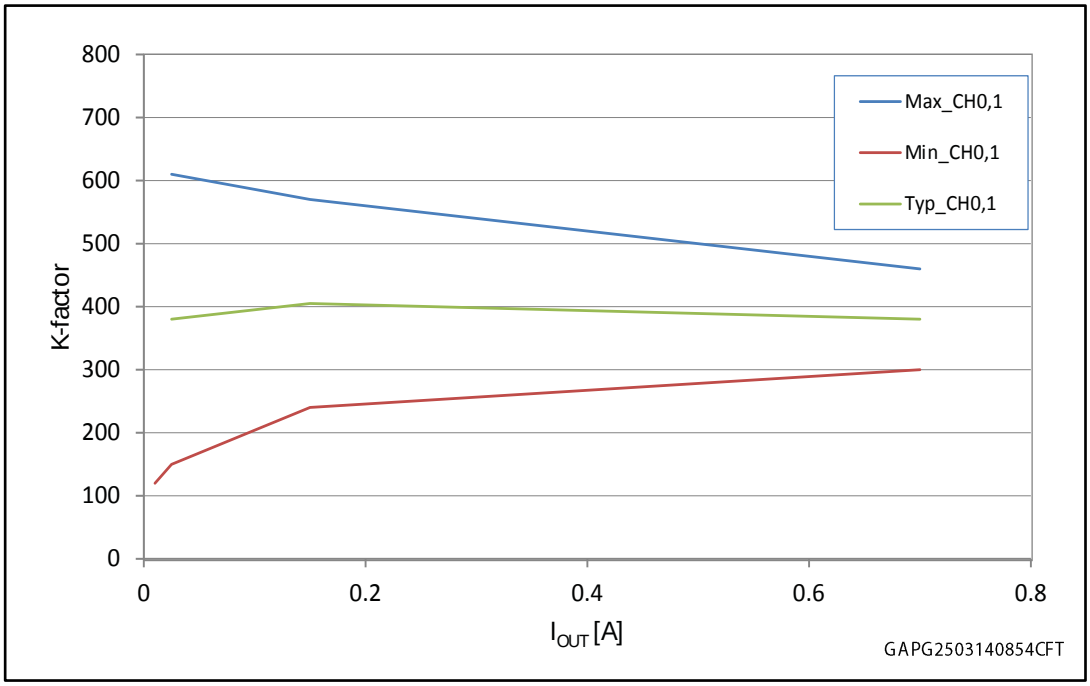
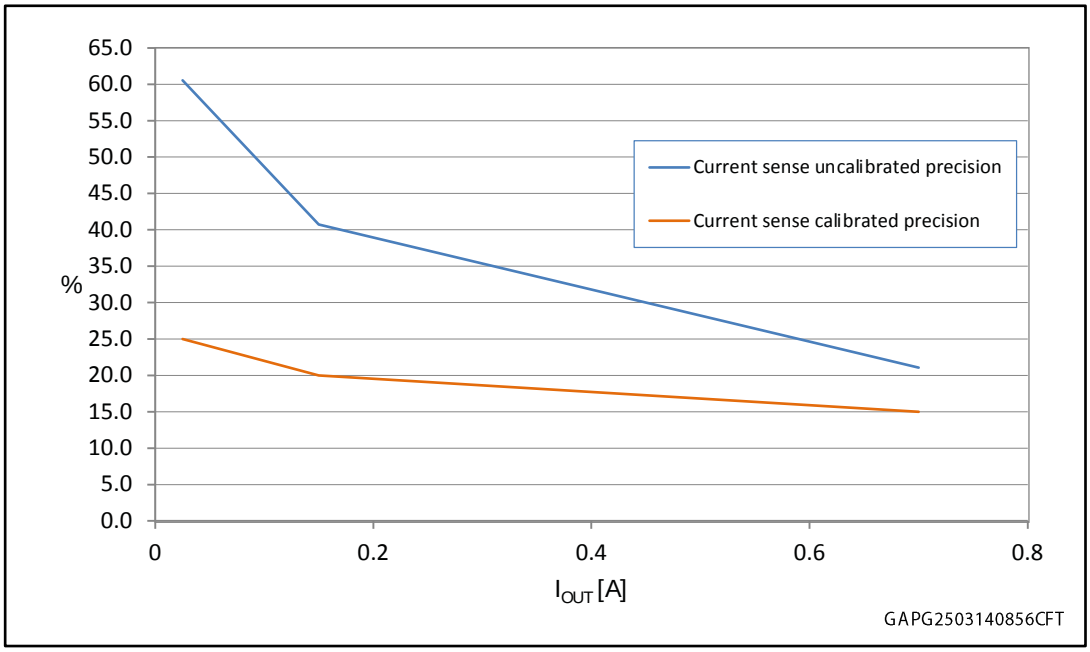


Figure 31: LED Mode - current sense precision vs. IOUT



2.3.5 Electrical characteristics curves - LED mode

Figure 32: On-state resistance vs. Tcase

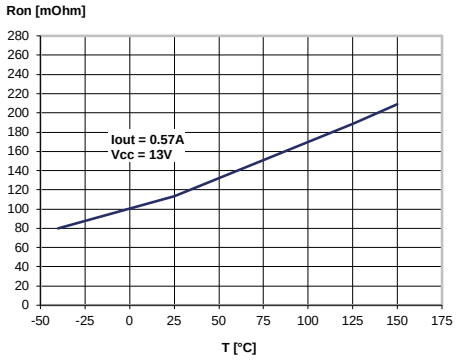


Figure 33: On-state resistance vs. VCC

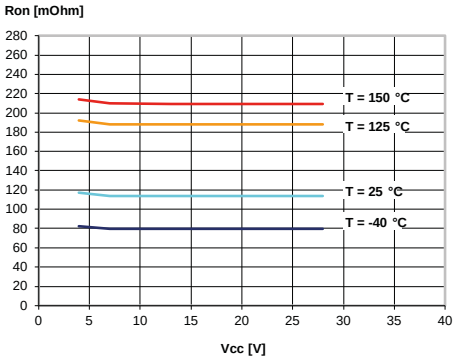


Figure 34: Turn-on voltage slope

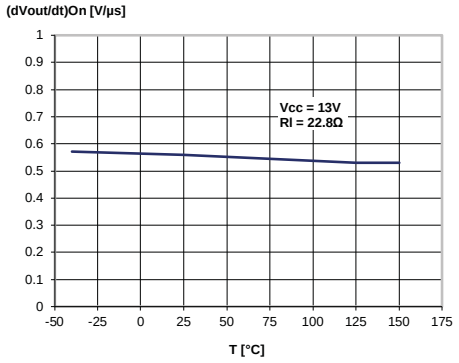


Figure 35: Turn-off voltage slope

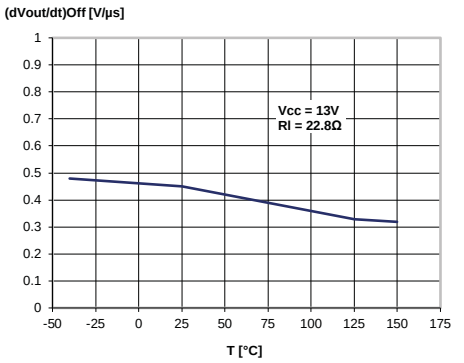


Figure 36: Won vs. Tcase

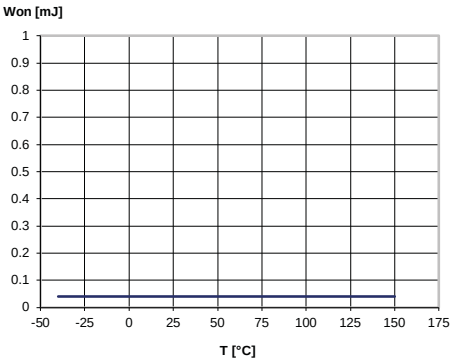


Figure 37: Woff vs. Tcase

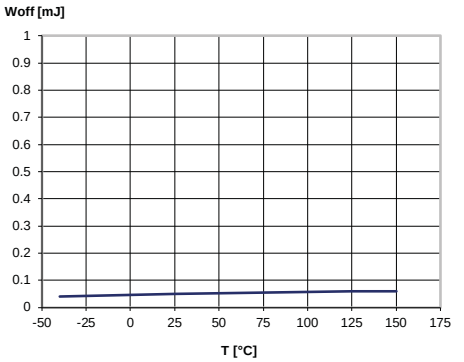
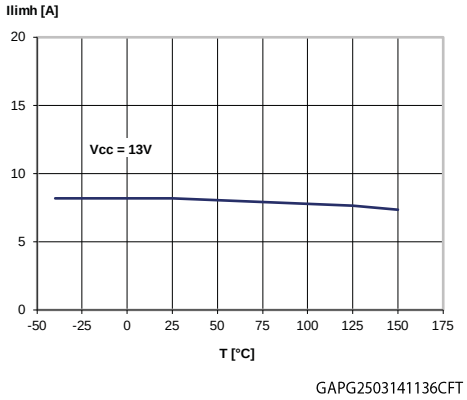


Figure 38: ILIMH vs. Tcase



2.3.6 Truth tables

Table 15: Truth table

Mode	Conditions	IN_X	FR	SEn	SEL_X	OUT_X	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T_j < 150°C	L	X	See (1)		L	See (1)	
		H	L			H	See (1)	Outputs configured for auto-restart
		H	H			H	See (1)	Outputs configured for Latch-off
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j\_SD}$	L	X	See (1)		L	See (1)	
		H	L			H	See (1)	Output cycles with temperature hysteresis
		H	H			L	See (1)	Output latches-off
Under-voltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	X	See (1)		H	See (1)	
	Open load	L	X			H	See (1)	External pull-up
Negative output voltage	Inductive loads turn off	L	X	See (1)		< 0V	See (1)	

Notes:

(1)Refer to *Table 16: "MultiSense multiplexer addressing"*

Table 16: MultiSense multiplexer addressing

SEn	SEL_2	SEL_1	SEL_0	MUX channel	MultiSense output			
					Normal mode	Overload	OFF-state diag. (1)	Negative output
L	X	X	X		Hi-Z			
H	L	L	L	Channel 0 diagnostic	I_{SENSE} = 1/K * I_{OUT0}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	L	L	H	Channel 1 diagnostic	I_{SENSE} = 1/K * I_{OUT1}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	L	H	L	Channel 2 diagnostic	I_{SENSE} = 1/K * I_{OUT2}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	L	H	H	Channel 3 diagnostic	I_{SENSE} = 1/K * I_{OUT3}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	H	L	L	T_{CHIP} Sense	V_{SENSE} = V_{SENSE_TC}			
H	H	L	H	V_{CC} Sense	V_{SENSE} = V_{SENSE_VCC}			
H	H	H	L	T_{CHIP} Sense	V_{SENSE} = V_{SENSE_TC}			
H	H	H	H	V_{CC} Sense	V_{SENSE} = V_{SENSE_VCC}			

Notes:

(1)In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic. Example 1: FR = 1; IN_0 = 0; OUT_0 = L (latched); MUX channel = channel 0 diagnostic; Mutisense = 0. Example 2: FR = 1; IN_0 = 0; OUT_0 = latched, V_{OUT0} > V_{OL}; MUX channel = channel 0 diagnostic; Mutisense = V_{SENSEH}

Table 17: Bulb/LED Mode Configuration

LED_1	LED_0	Configuration	
		Channel 1	Channel 0
L	L	Bulb	Bulb
L	H	Bulb	LED
H	L	LED	Bulb
H	H	LED	LED

3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD}. According to the voltage level on the FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FaultRST = Low) or remains off (FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FaultRST pin, the device switches on again as soon as its junction temperature drops to T_R (FaultRST = Low) or remains off (FaultRST = High).

3.3 Current limitation

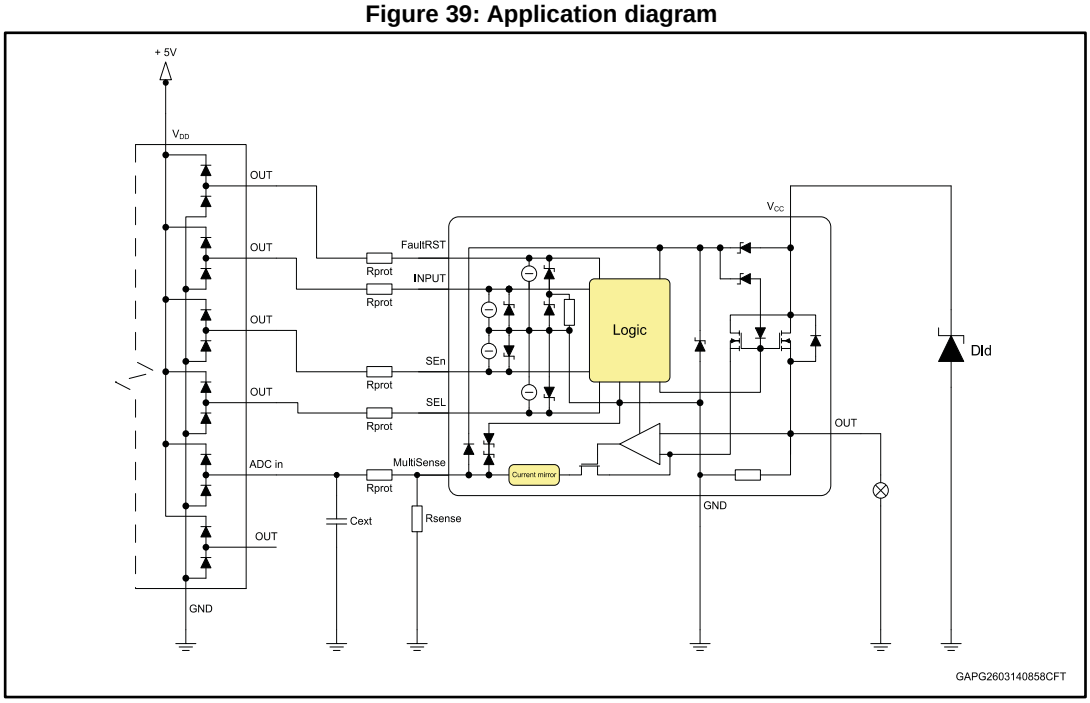
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG}, allowing the inductor energy to be dissipated without damaging the device.

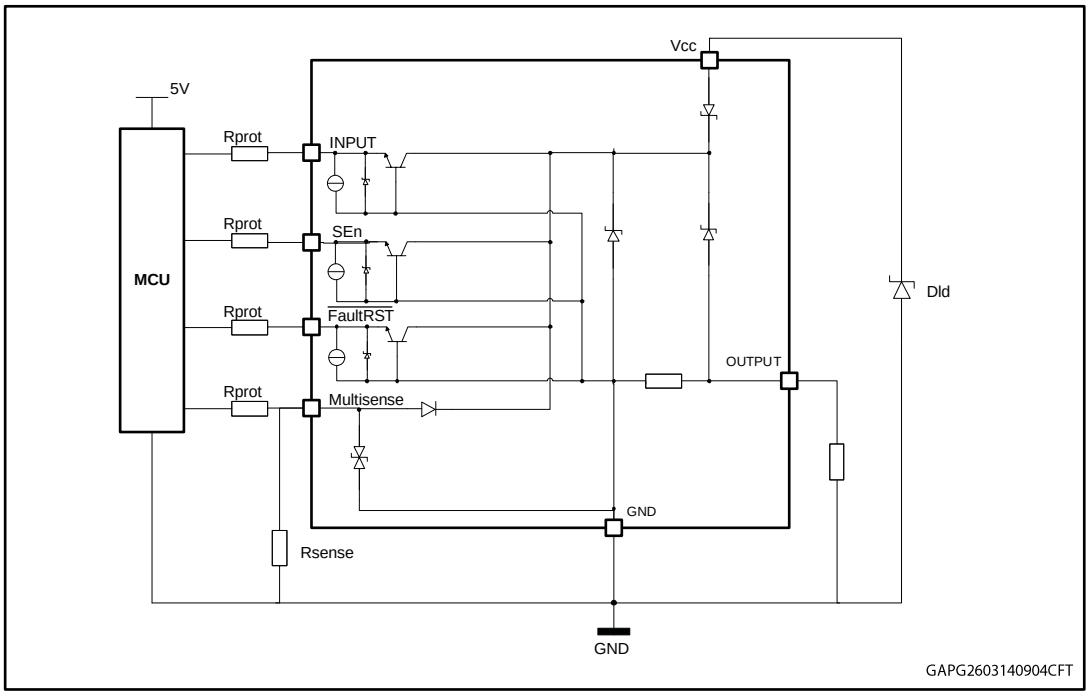
4 Application information

Figure 39: Application diagram



4.1 GND protection network against reverse battery

Figure 40: Simplified internal structure



The device does not need any external components to protect the internal logic in case of a reverse battery condition. The protection is provided by internal structures.

In addition, due to the fact that the output MOSFET turns on even in reverse battery mode, thus providing the same low ohmic path as in regular operating conditions, no additional power dissipation has to be considered.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in *Table 18: "ISO 7637-2 - electrical transient conduction along supply line"*.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

Table 18: ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S (1)		min	max	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a (3)	III	+55 V	500 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4 (2)	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B (3)		40 V	5 pulse	1 min		400 ms, 2 Ω

Notes:

(1) U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

(2) Test pulse from ISO 7637-2:2004(E).

(3) With 40 V external suppressor referred to ground (-40°C < T_j < 150 °C).

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latching-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation

$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak} = -150 V; $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

7.5 kΩ ≤ R_{prot} ≤ 140 kΩ.

Recommended values: R_{prot} = 15 kΩ

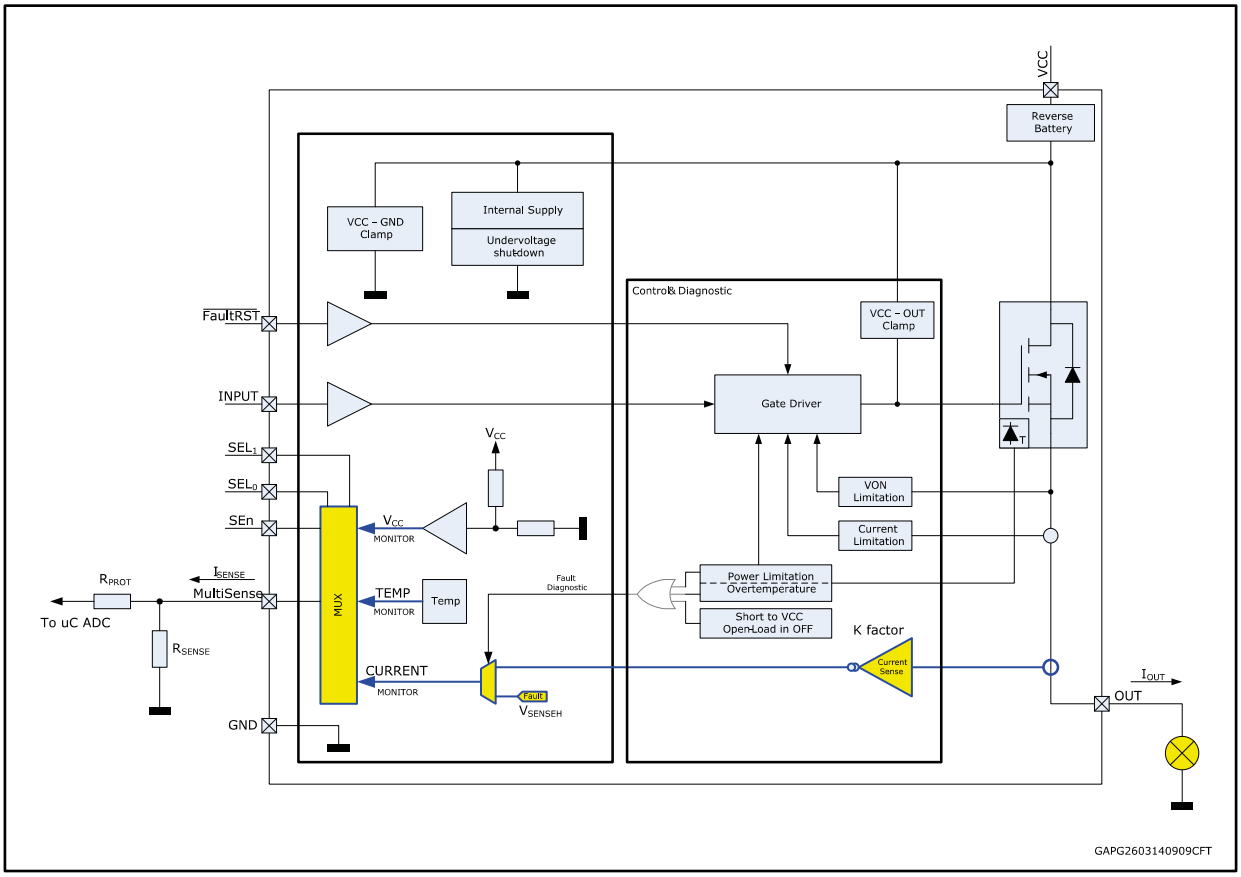
4.4 Multisense - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (MultiSense) delivering the following signals:

- Current monitor: current mirror of channel output current
- V_{CC} monitor: voltage propotional to V_{CC}
- T_{CASE}: voltage propotional to chip temperature

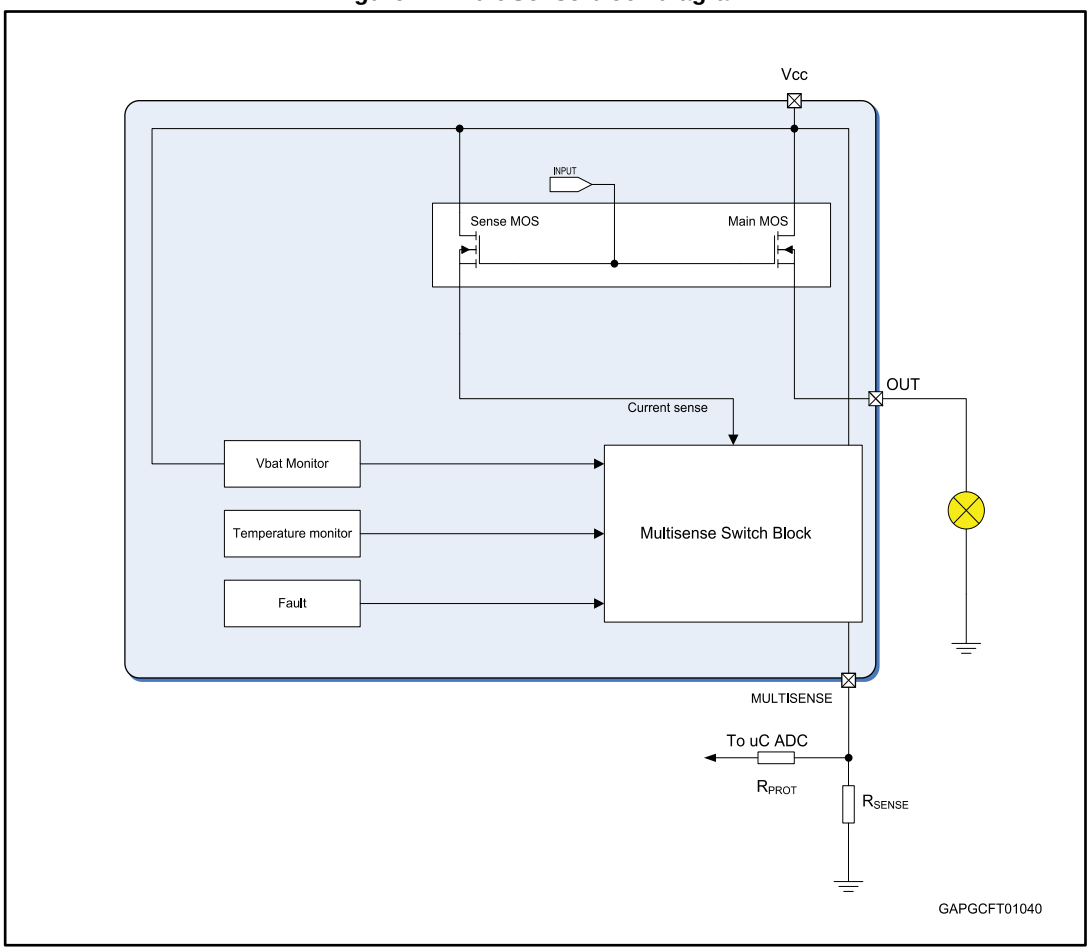
Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in *MultiSense multiplexer addressing Table*.

Figure 41: MultiSense and diagnostic – block diagram



4.4.1 Principle of Multisense signal generation

Figure 42: MultiSense block diagram



Current monitor

When current mode is selected via MultiSense, this output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to a known ratio named **K**
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by MultiSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- V_{SENSE} is the voltage measurable on R_{SENSE} resistor
- I_{SENSE} is the current provided from MultiSense pin in current output mode

- I_{OUT} is the current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying the ratio between I_{OUT} and I_{SENSE}.

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the MultiSense pin which is switched to a “current limited” voltage source, V_{SENSEH}.

In any case, the current sourced by the MultiSense in this condition is limited to I_{SENSEH}.

The typical behavior in case of overload or hard short circuit is shown in *Waveforms section*.

Figure 43: Analogue HSD – open-load detection in off-state

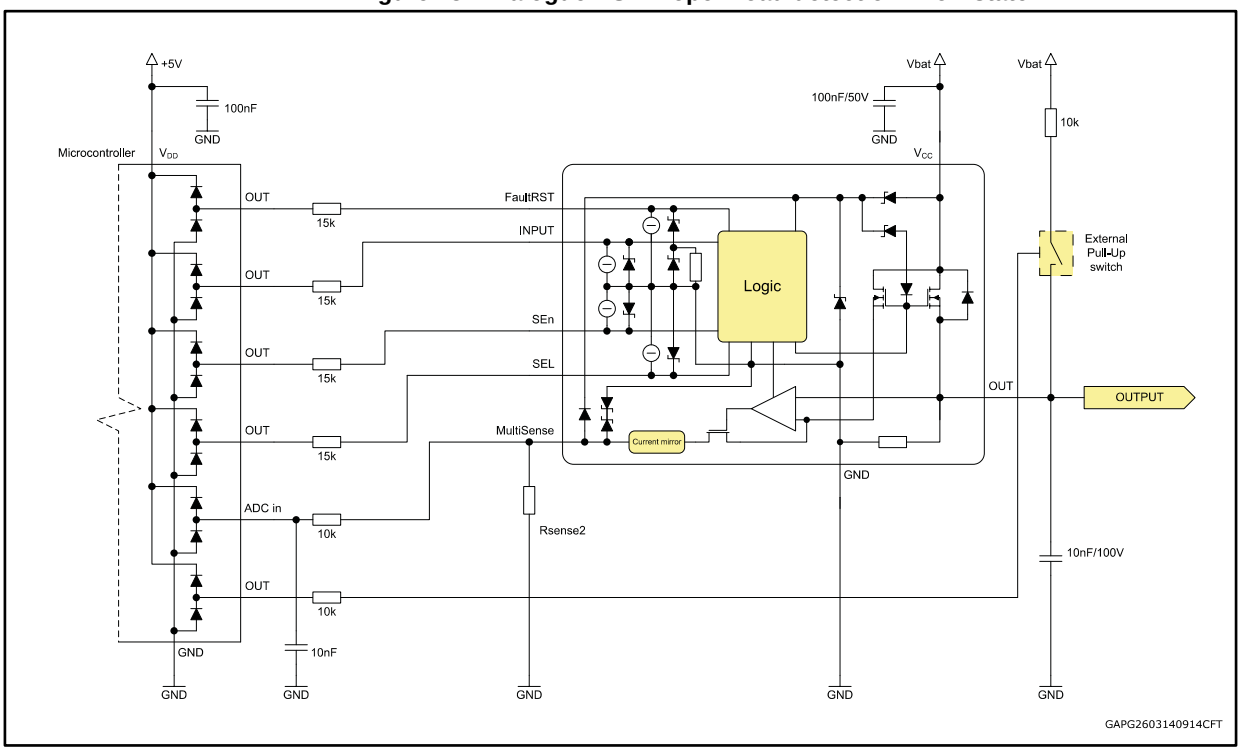


Figure 44: Open-load / short to VCC condition

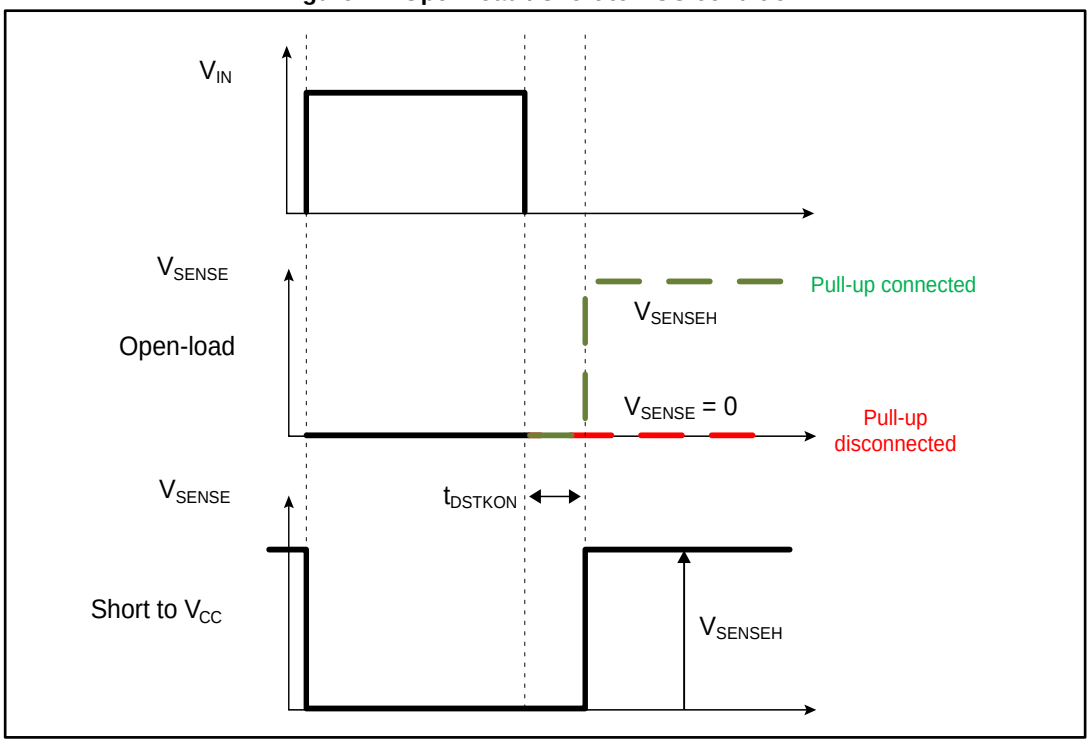


Table 19: MultiSense pin levels in off-state

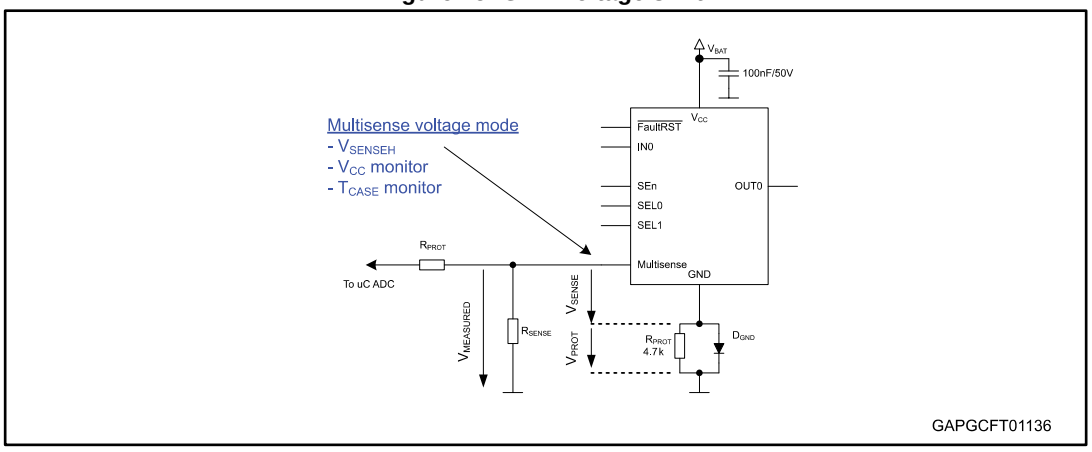
Condition	Output	MultiSense	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 TCASE and VCC monitor

In this case, MultiSense output operates in voltage mode and output level is referred to device GND. Care must be taken in case a GND network protection is used, because a voltage shift is generated between the device GND and the microcontroller input GND reference.

Figure 45: "GND voltage shift" shows the link between $V_{MEASURED}$ and the real V_{SENSE} signal.

Figure 45: GND voltage shift



V_{CC} monitor

Battery monitoring channel provides $V_{SENSE} = V_{CC} / 8$.

Case temperature monitor

Case temperature monitor is capable of providing information about the actual device temperature. Since a diode is used for temperature sensing, the following equation describes the link between temperature and output V_{SENSE} level:

$V_{SENSE\_TC}(T) = V_{SENSE\_TC}(T_0) + dV_{SENSE\_TC} / dT * (T - T_0)$

where dV_{SENSE_TC} / dT ~ typically -5.5 mV/K (for temperature range (-40 °C to 150 °C)).

4.4.3 Short to VCC and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable that V_{PU} is switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

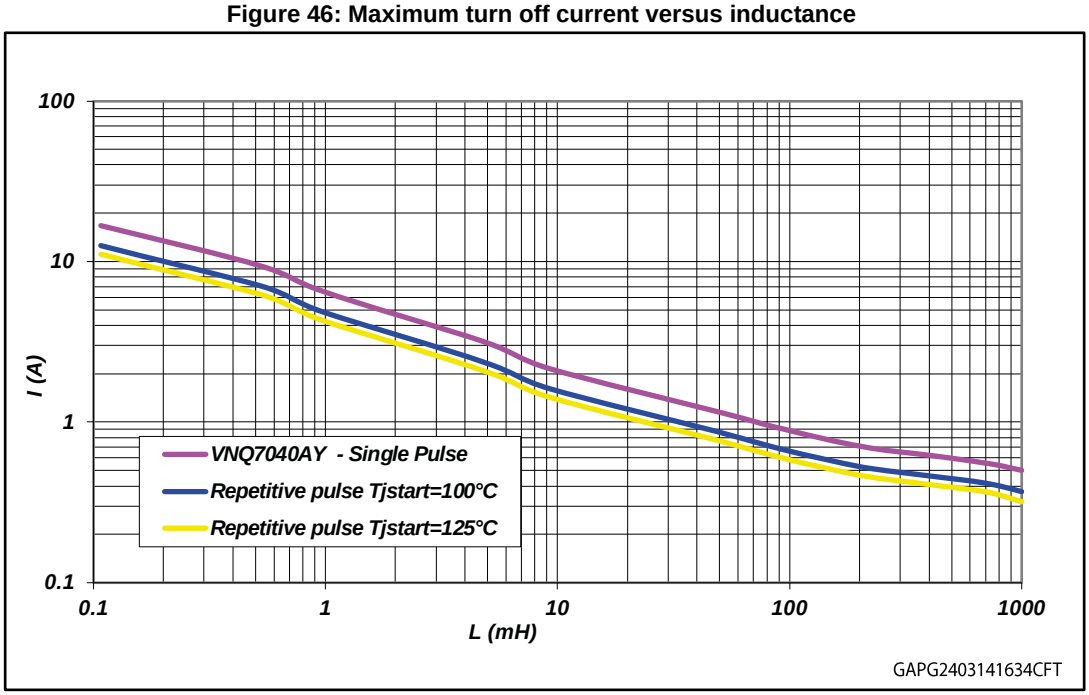
R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

Equation

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min\ @\ 4V}}$$

5 Maximum demagnetization energy (VCC = 16 V)

Figure 46: Maximum turn off current versus inductance



6 Package and PCB thermal data

6.1 PowerSSO-36 thermal data

Figure 47: PowerSSO-36 PC board

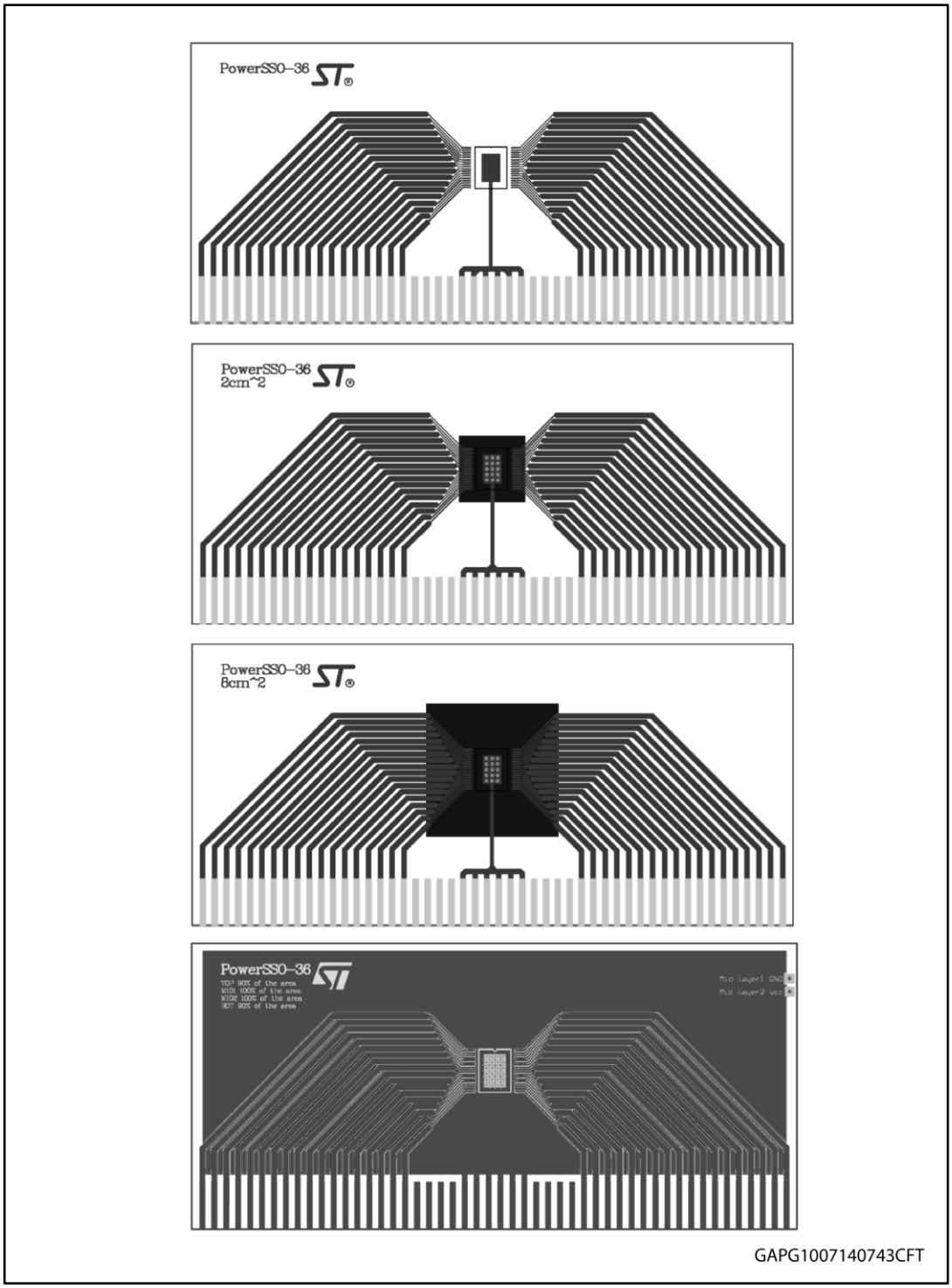


Table 20: PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	129 mm x 60 mm
Board Material	FR4
Cu thickness (outer layers)	0.070 mm
Cu thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Cu thickness on vias	0.025 mm
Footprint dimension	4.1 mm x 6.5 mm

Figure 48: Rthj-amb vs PCB copper area in open box free air condition

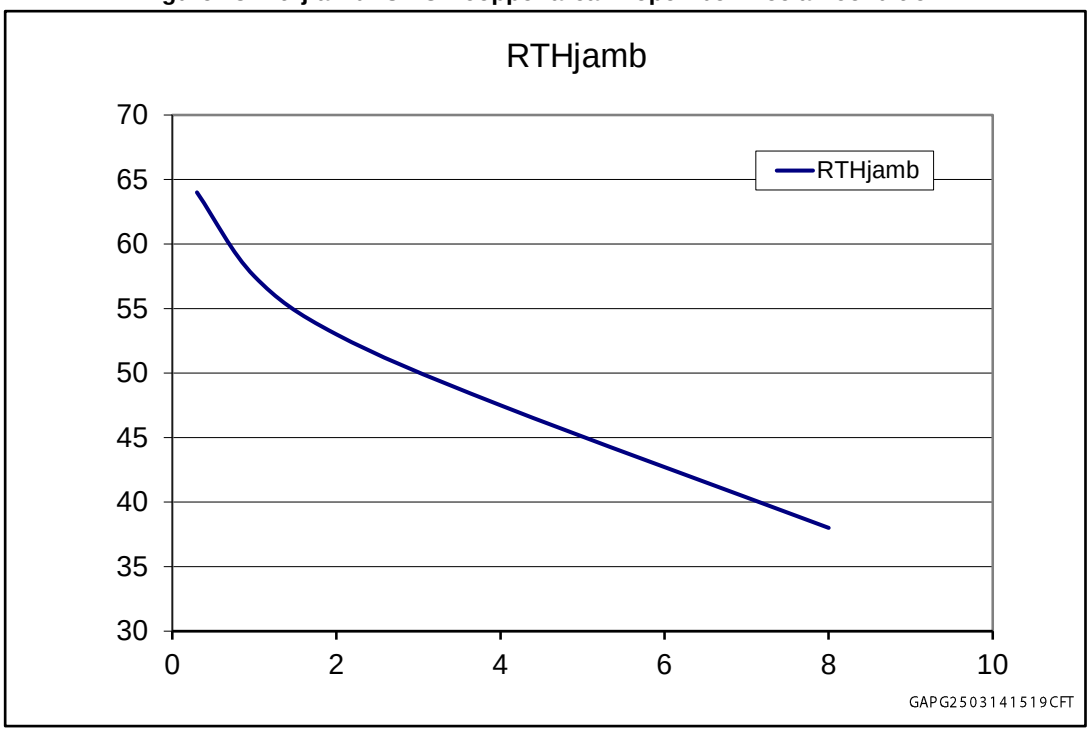


Figure 49: PowerSSO-36 thermal impedance junction ambient

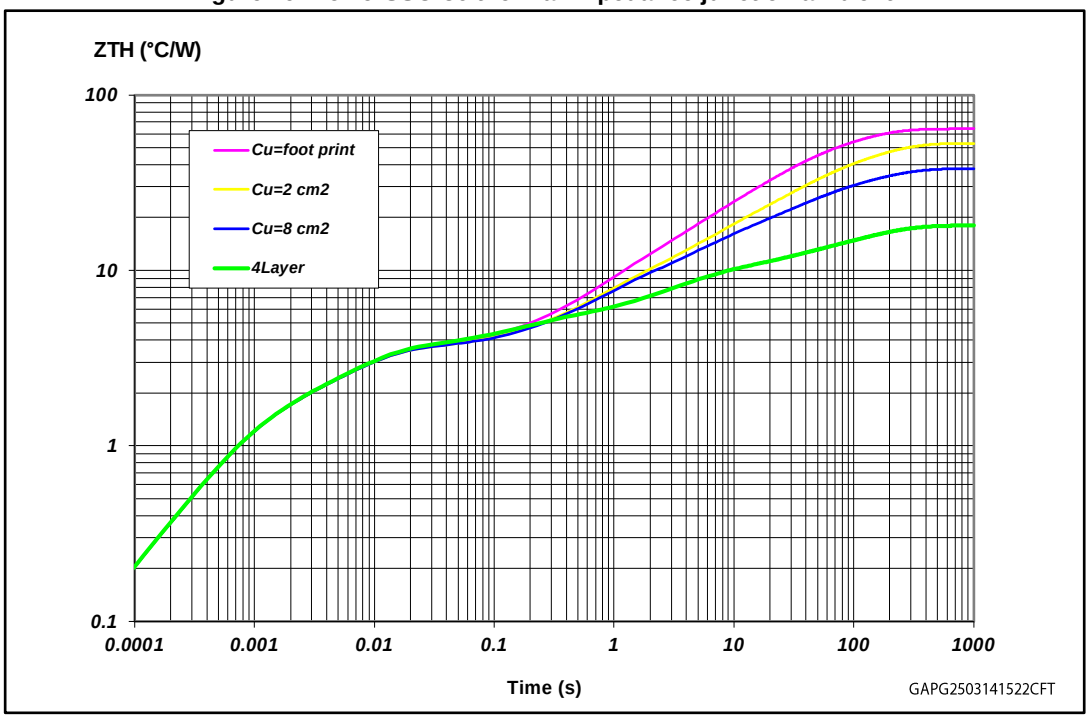


Figure 50: Thermal fitting model of a HSD in PowerSSO-36

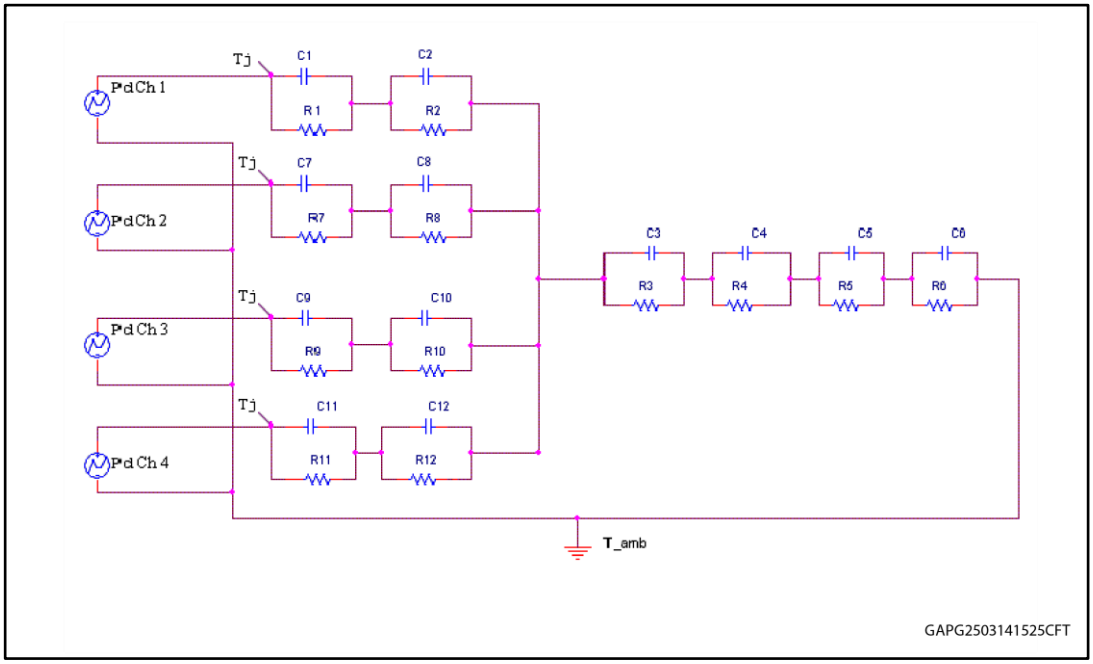


Table 21: Thermal parameters

Area/island (cm^2)	FP	2	8	4L
R1 = R7 = R9 = R11 (°C/W)	1.8			
R2 = R8 = R10 = R12 (°C/W)	1.7			
R3 (°C/W)	3.5	3.5	3.5	2
R4 (°C/W)	8	6	6	4
R5 (°C/W)	20	14	10	2
R6 (°C/W)	30	26	15	7
C1 = C7 = C9 = C11 (W·s/°C)	0.0005			
C2 = C8 = C10 = C12 (W·s/°C)	0.01			
C3 (W·s/°C)	0.1	0.1	0.1	0.1
C4 (W·s/°C)	0.5	0.8	0.8	0.8
C5 (W·s/°C)	1	2	3	10
C6 (W·s/°C)	3	5	9	18

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

7.1 PowerSSO-36 package information

Figure 51: PowerSSO-36 package outline

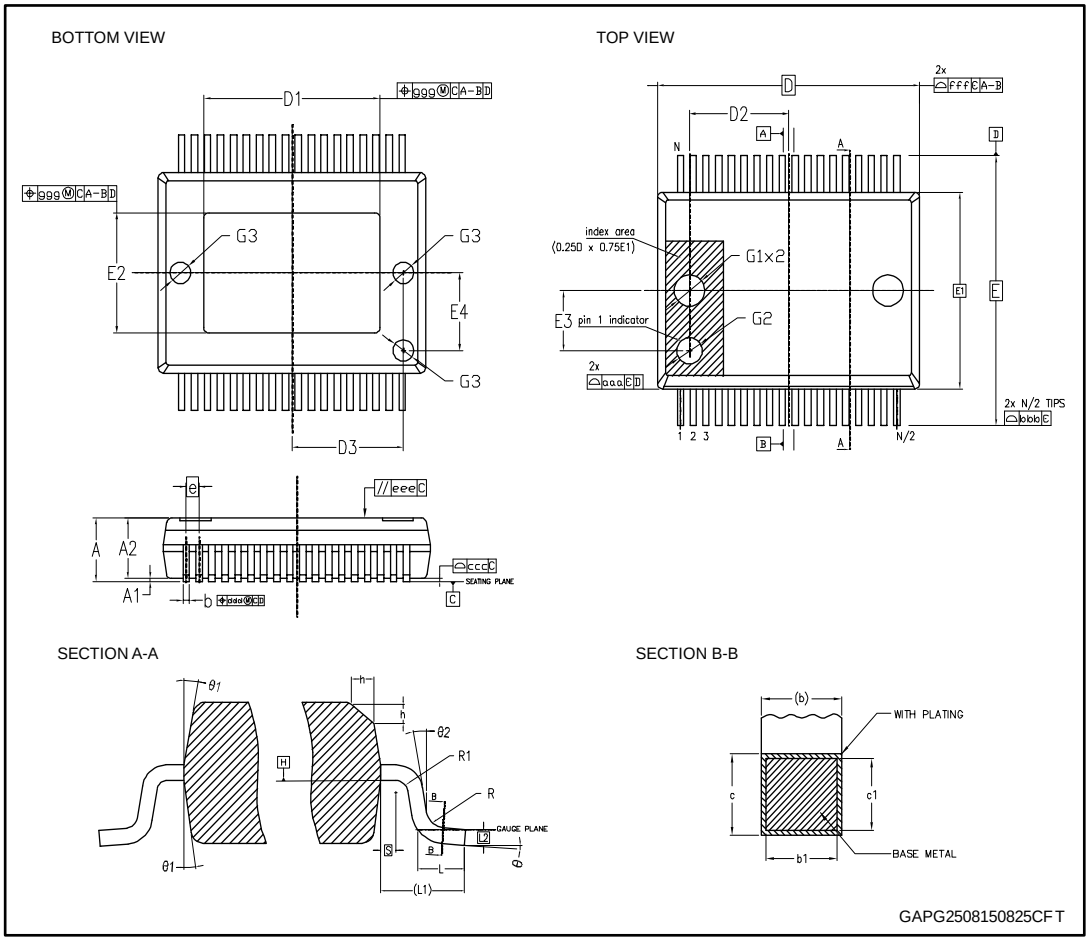


Table 22: PowerSSO-36 mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
Θ1	5°		10°
Θ2	0°		
A	2.15		2.45
A1	0.00		0.10

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A2	2.15		2.35
b	0.18		0.32
b1	0.13	0.25	0.30
c	0.23		0.32
c1	0.20	0.20	0.30
D	10.30 BSC		
D1	6.90		7.50
D2		3.65	
D3		4.30	
e	0.50 BSC		
E	10.30 BSC		
E1	7.50 BSC		
E2	4.30		5.20
E3		2.30	
E4		2.90	
G1		1.20	
G2		1.00	
G3		0.80	
h	0.30		0.40
L	0.55	0.70	0.85
L1	1.40 REF		
L2	0.25 BSC		
N	36		
R	0.30		
R1	0.20		
S	0.25		
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
eee	0.10		
fff	0.20		
ggg	0.15		

7.2 PowerSSO-36 packing information

Figure 52: PowerSSO-36 reel 13"

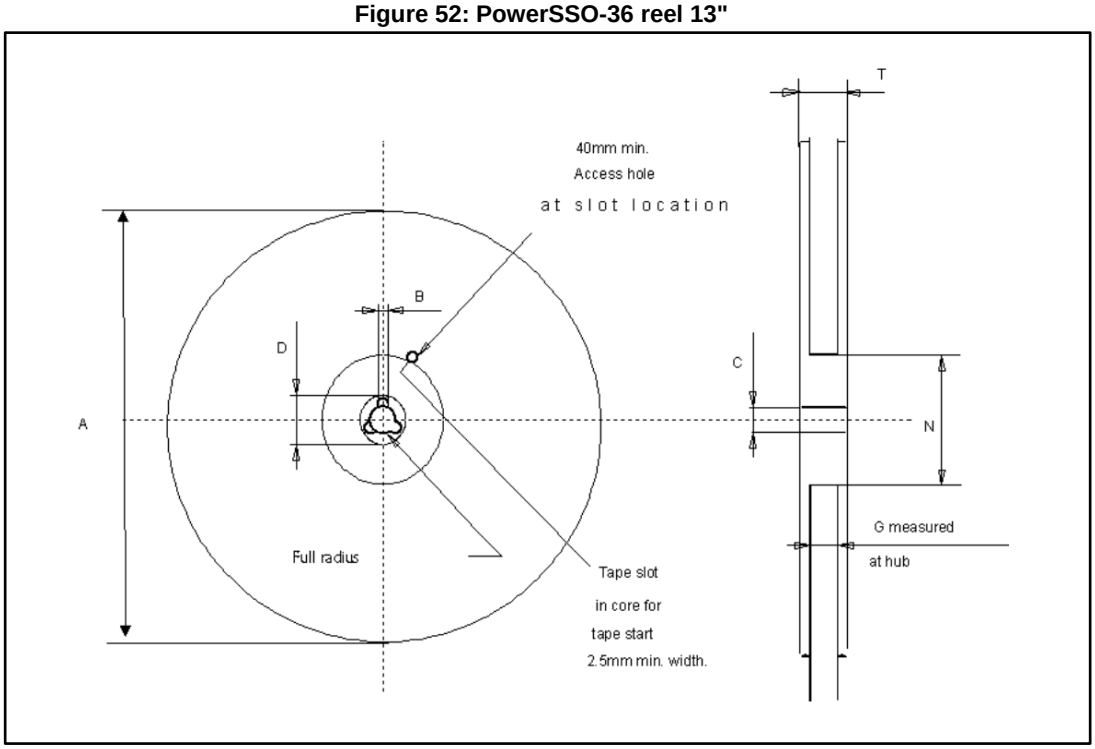


Table 23: Reel dimensions

Description	Value[(1)]
Base quantity	1000
Bulk quantity	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

Notes:

(1)All dimensions are in mm.

Figure 53: PowerSSO-36 carrier tape

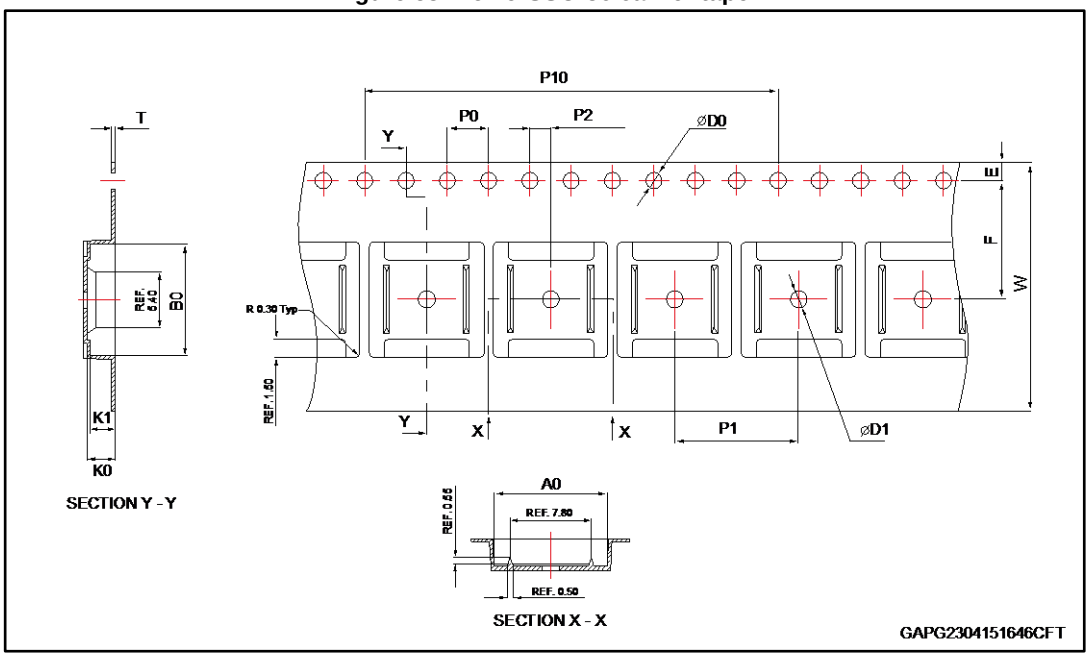


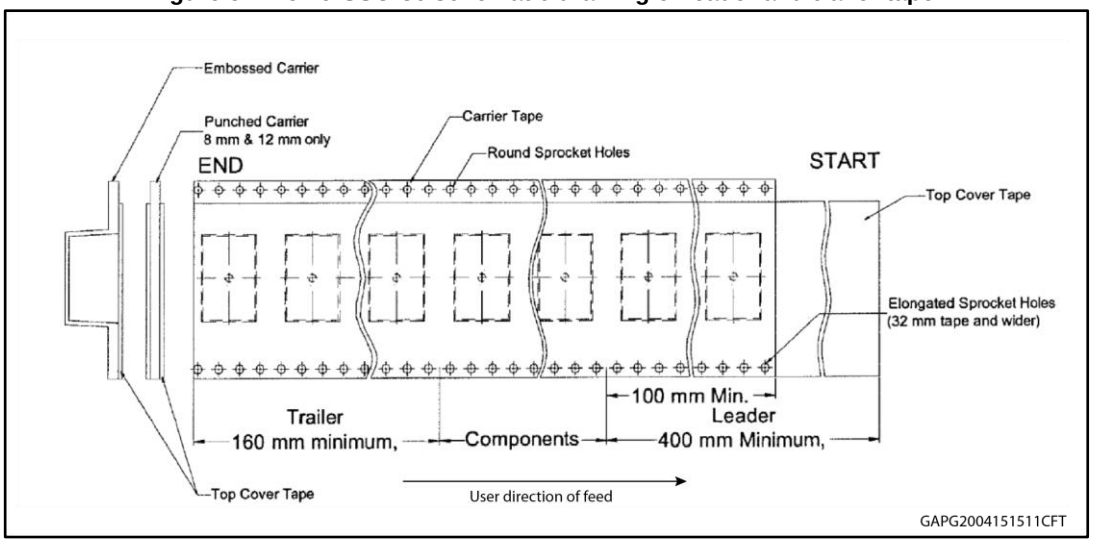
Table 24: PowerSSO-36 carrier tape dimensions

Description	Value[(1)]
A_0	10.90 ± 0.10
B_0	10.80 ± 0.10
K_0	2.75 ± 0.10
K_1	2.45 ± 0.10
D_0	1.50 (+0.10 / -0)
D_1	1.60 ± 0.10
P_0	4.00 ± 0.10
P_1	12.00 ± 0.10
P_2	2.00 ± 0.10
P_{10}	40.00 ± 0.20
E	1.75 ± 0.10
F	11.50 ± 0.10
W	24.00 ± 0.30
T	0.30 ± 0.05

Notes:

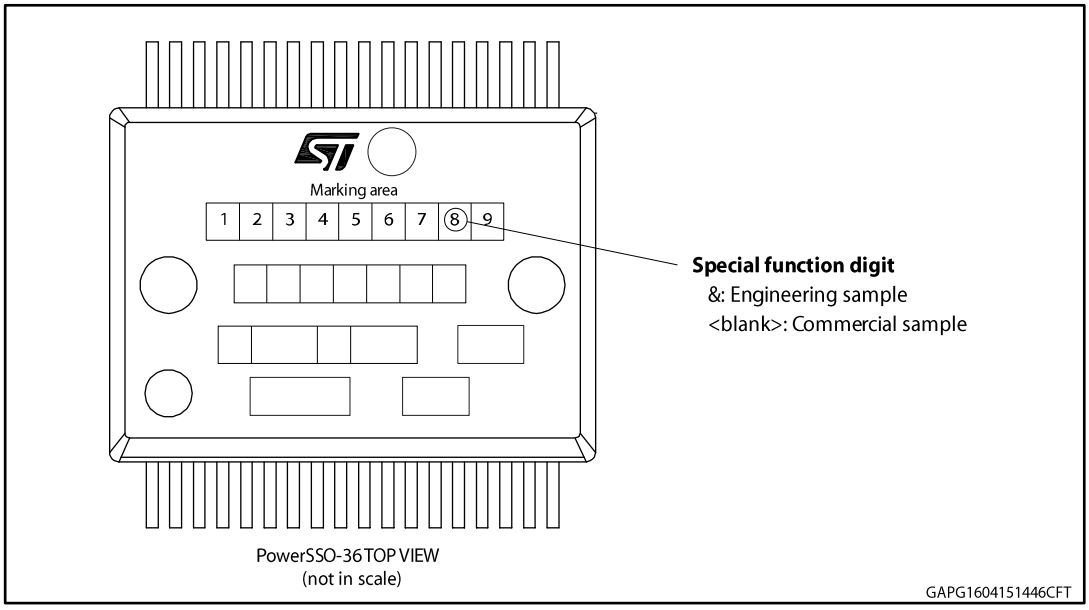
(1)All dimensions are in mm.

Figure 54: PowerSSO-36 schematic drawing of leader and trailer tape



7.3 PowerSSO-36 marking information

Figure 55: PowerSSO-36 marking information



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8 Order codes

Table 25: Device summary

Package	Order codes
	Tape and reel
PowerSSO-36	VNQ7040AYTR

9 Revision history

Table 26: Document revision history

Date	Revision	Changes
21-Oct-2015	1	Initial release.
02-May-2016	2	Added “AEC-Q100 qualified” in Features Upated Table 4: "Thermal data" Upated Table 8: "MultiSense" Updated Section 6: "Package and PCB thermal data"
15-Jul-2016	3	Updated Figure 52: "PowerSSO-36 reel 13""and Table 23: "Reel dimensions"
21-Dec-2017	4	Updated *Table 10: "Switching in Bulb Mode"* and *Table 12: "Switching in LED Mode"*

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