Contents

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1 Pin connection

Figure 2. Pin connection (top view)

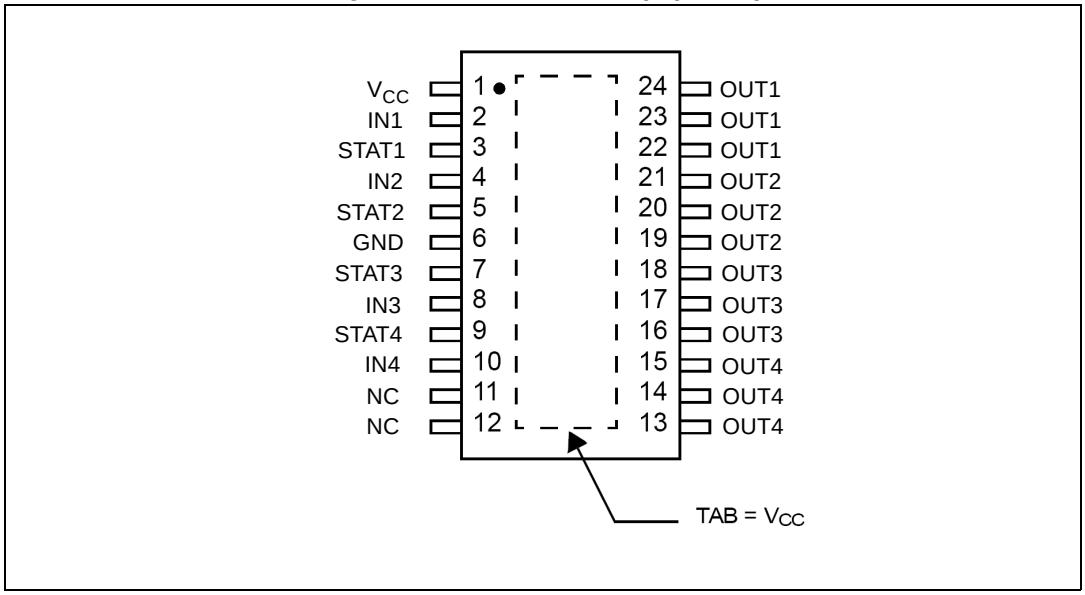

Table 1. Pin description

Pin	Name	Description
Tab	TAB	Exposed tab internally connected to V_{cc}
1	V_{CC}	Supply voltage
2	IN1	Channel 1 input 3.3 V CMOS/TTL compatible
3	STAT1	Channel 1 status in open drain configuration
4	IN2	Channel 2 input 3.3 V CMOS/TTL compatible
5	STA2	Channel 2 status in open drain configuration
6	GND	Device ground connection
7	STAT3	Channel 3 status in open drain configuration
8	IN3	Channel 3 input 3.3 V CMOS/TTL compatible
9	STAT4	Channel 4 status in open drain configuration
10	IN4	Channel 4 input 3.3 V CMOS/TTL compatible
11	NC	
12	NC	
13	OUT4	Channel 4 power stage output, internally protected
14	OUT4	Channel 4 power stage output, internally protected
15	OUT4	Channel 4 power stage output, internally protected
16	OUT3	Channel 3 power stage output, internally protected
17	OUT3	Channel 3 power stage output, internally protected

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Table 1. Pin description (continued)

Pin	Name	Description
18	OUT3	Channel 3 power stage output, internally protected
19	OUT2	Channel 2 power stage output, internally protected
20	OUT2	Channel 2 power stage output, internally protected
21	OUT2	Channel 2 power stage output, internally protected
22	OUT1	Channel 1 power stage output, internally protected
23	OUT1	Channel 1 power stage output, internally protected
24	OUT1	Channel 1 power stage output, internally protected

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2 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	41	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
I_{GND}	DC ground reverse current	-250	mA
I_{OUT}	Output current (continuous)	Internally limited	A
I_R	Reverse output current (per channel)	-5	A
I_{IN}	Input current (per channel)	± 10	mA
V_{IN}	Input voltage	$+V_{CC}$	V
V_{STAT}	Status pin voltage	$+V_{CC}$	V
I_{STAT}	Status pin current	± 10	mA
V_{ESD}	Electrostatic discharge (R = 1.5 kΩ; C = 100 pF)	2000	V
E_{AS}	I_{OUT} = 500 mA T_{AMB} = 125 °C	5	J
P_{TOT}	Power dissipation at T_c = 25 °C	Internally limited	W
T_J	Junction operating temperature	Internally limited	°C
T_{STG}	Storage temperature	-55 to 150	°C

2.1 Thermal data

Table 3. Thermal data

Symbol	Parameter		Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case (1)	Max.	2	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient	Max.	see *Figure 11*	°C/W

1. Per channel.

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3 Electrical characteristics

10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified

Table 4. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{cc}	Supply voltage		10.5		36	V
$R_{DS(on)}$	On-state resistance	I_{OUT} = 0.5 A at T_J = 25 °C I_{OUT} = 0.5 A			0.080 0.140	Ω Ω
V_{clamp}		I_S = 20 mA	41	45	52	V
I_S	Supply current	All channels in OFF state ON state with V_{IN} = 5 V (T_J = 125 °C)		250 2.4	4	µA mA
I_{LGND}	Output current at turn-off	V_{CC} = V_{STAT} = V_{IN} = V_{GND} = 24 V, V_{OUT} = 0 V			1	mA
$V_{OUT(OFF)}$	Off state output voltage	V_{IN} = 0 V and I_{OUT} = 0 A			1	V
$I_{OUT(OFF)}$	Off state output current	V_{IN} = V_{OUT} = 0 V	0		5	µA
F_{CP}	Charge pump frequency	Channel in ON state (1)		1450		kHz

1. To cover EN55022 class A and class B normative.

V_{CC} = 24 V; -40 °C < T_J < 125 °C, R_L = 48 Ω, input rise time < 0.1 µs

Table 5. Switching

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{d(ON)}$	Turn on delay	-	20	-	µs
t_r	Rise time	-	10	-	µs
$t_{d(OFF)}$	Turn off	-	30	-	µs
t_f	Fall time	-	8	-	µs
$dV/dt_{(ON)}$	Turn on voltage slope	-	3	-	V/µs
$dV/dt_{(OFF)}$	Turn off voltage slope	-	4	-	V/µs

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Table 6. Logical input

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.8	V
V_{IH}	Input high level voltage		2.20			V
$V_{I(HYST)}$	Input hysteresis voltage			0.15		V
I_{IN}	Input current	V_{IN} = 15 V			10	µA
		V_{IN} = 36 V			210	

Table 7. Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status voltage output low	I_{STAT} = 1.6 mA			0.6	V
V_{USD}	Undervoltage protection		7		10.5	V
V_{USDHYS}	Undervoltage hysteresis		0.4	0.5		V
I_{LIM}	DC short-circuit current	V_{CC} = 24 V; R_{LOAD} < 10 mΩ	0.7	1	1.7	A
I_{PEAK}	Maximum DC output current	Dynamic load		1.3		A
HYST	Tracking limits			0.2		A
I_{LSTAT}	Status leakage current	V_{CC} = V_{STAT} = 36 V		30		µA
T_{TSD}	Junction shutdown temperature		150	170	190	°C
T_R	Junction reset temperature		135			°C
T_{HYST}	Junction thermal hysteresis		7	15		°C
T_{CSD}	Case shutdown temperature		125	130	135	°C
T_{CR}	Case reset temperature		110			°C
T_{CHYST}	Case thermal hysteresis		7	15		°C
V_{demag}	Output voltage at turn-off	I_{OUT} = 0.5 A; L_{LOAD} >= 1 mH	V_{CC}-41	V_{CC}-45	V_{CC}-52	V

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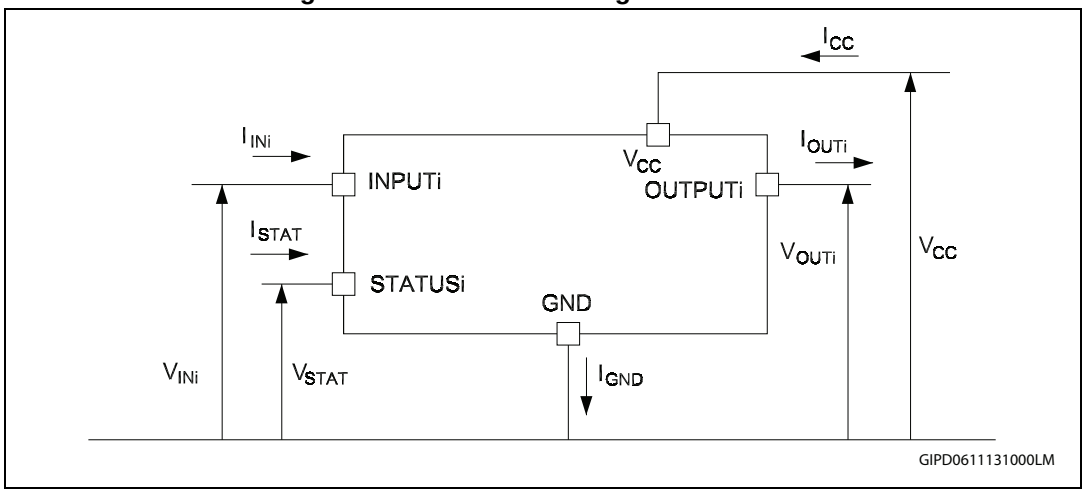
Figure 3. Current and voltage conventions



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4 Truth table

Table 8.Truth table

Condition	INPUTn	OUTPUTn	STATUSn
Normal operation	L H	L H	H H
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Shorted load (current limitation)	L H	L X	H H

5 Typical application circuit

Figure 4. Typical application circuit

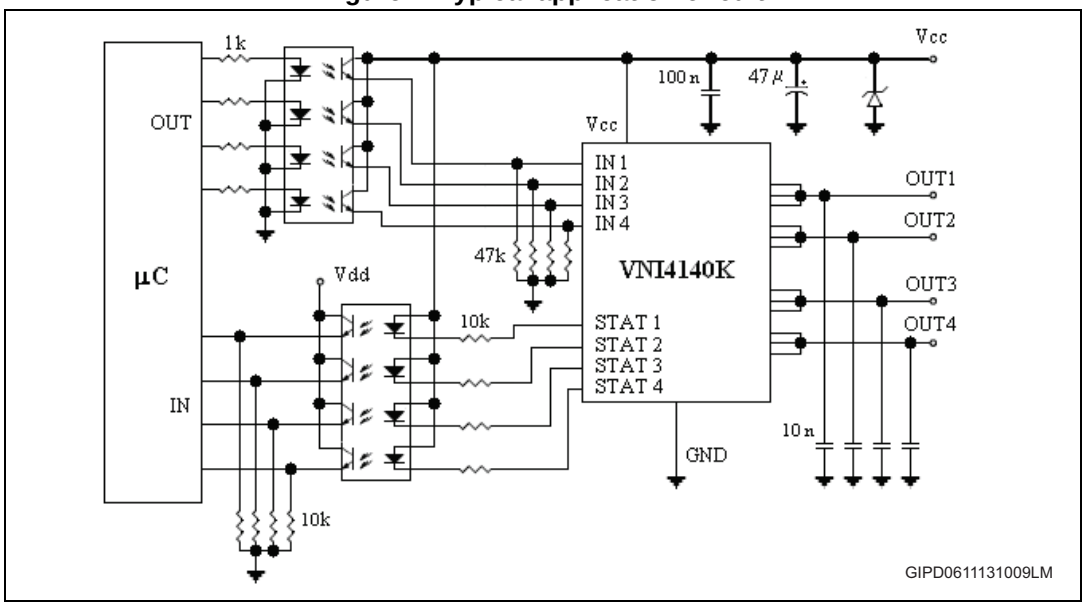

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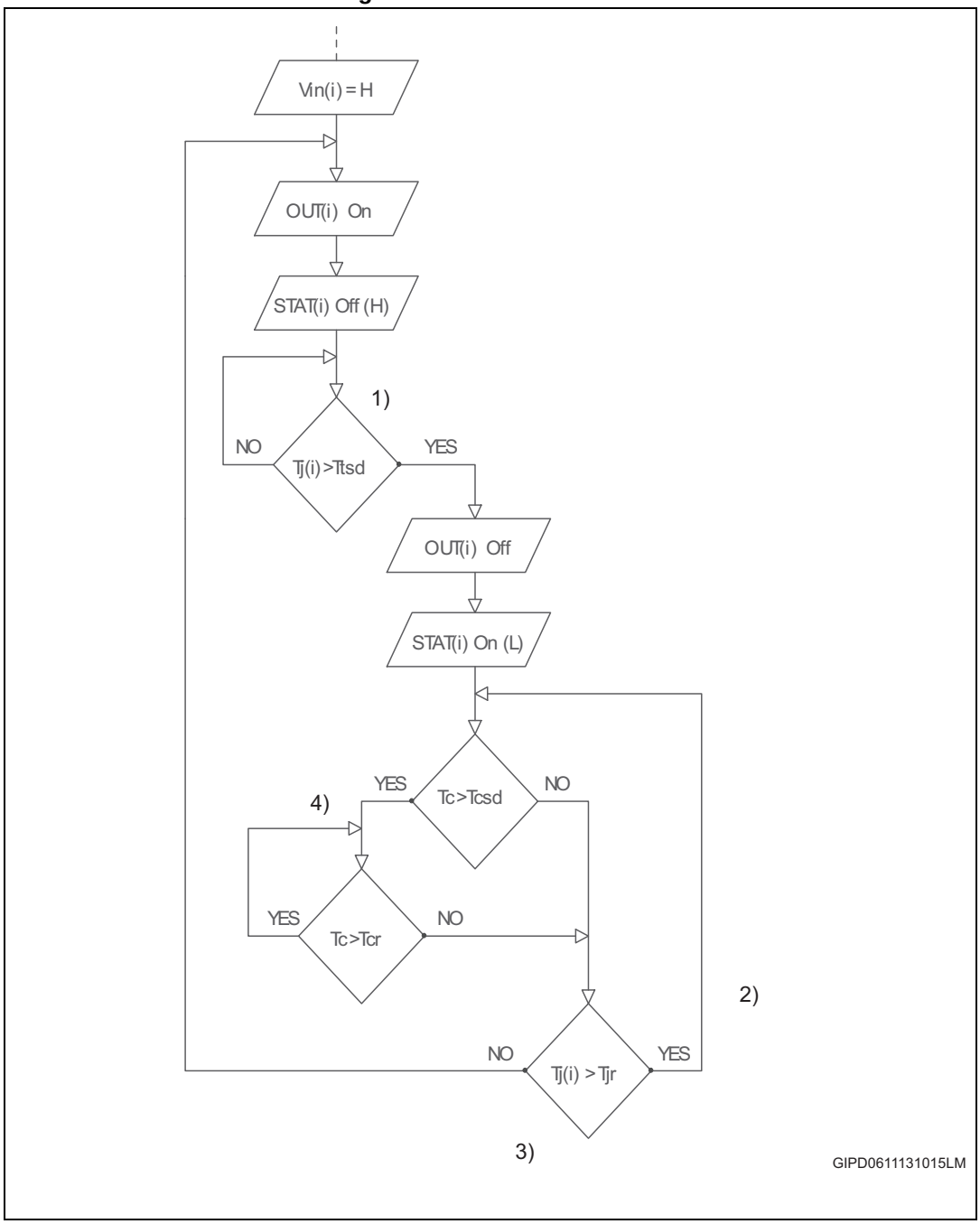
Figure 5. Thermal behavior



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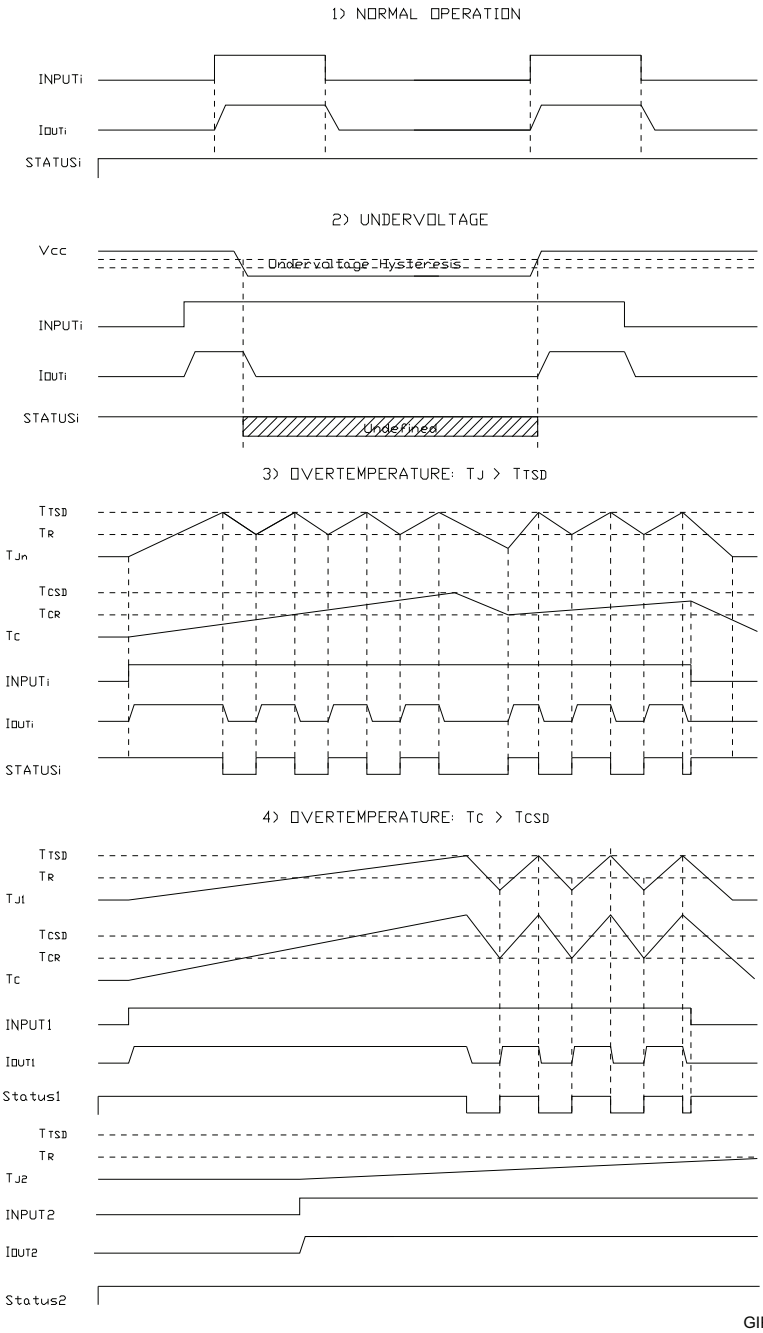
6 Switching waveforms

Figure 6. Switching waveforms



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7 Pin functions

Figure 7. Input circuit

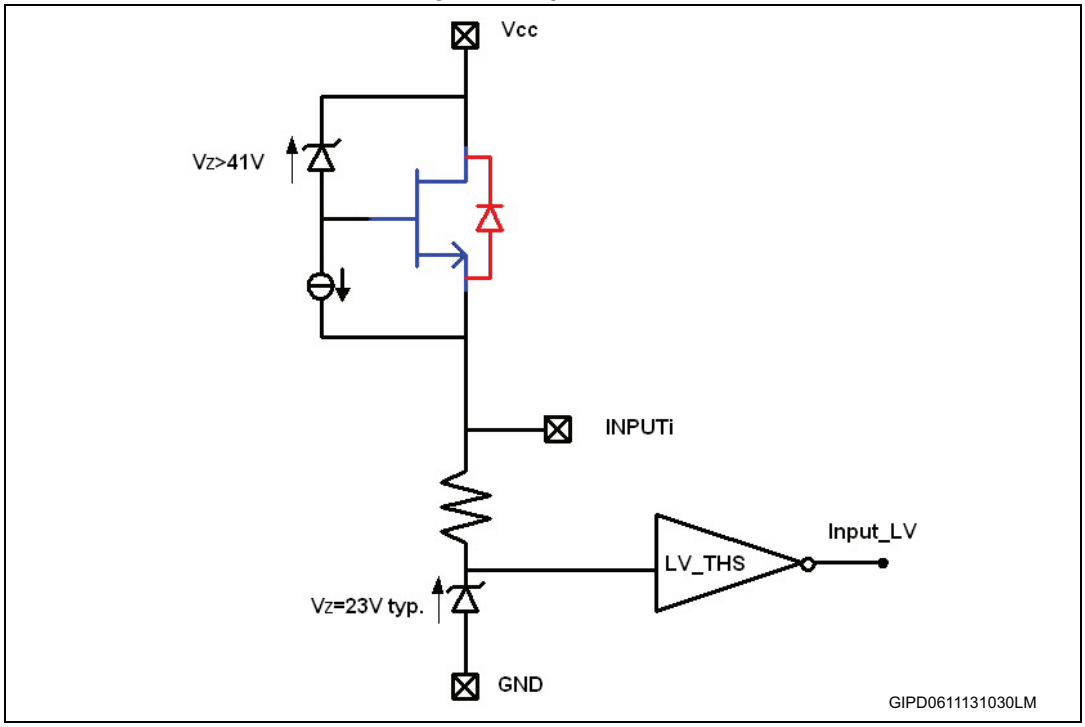

Figure 8. Status circuit

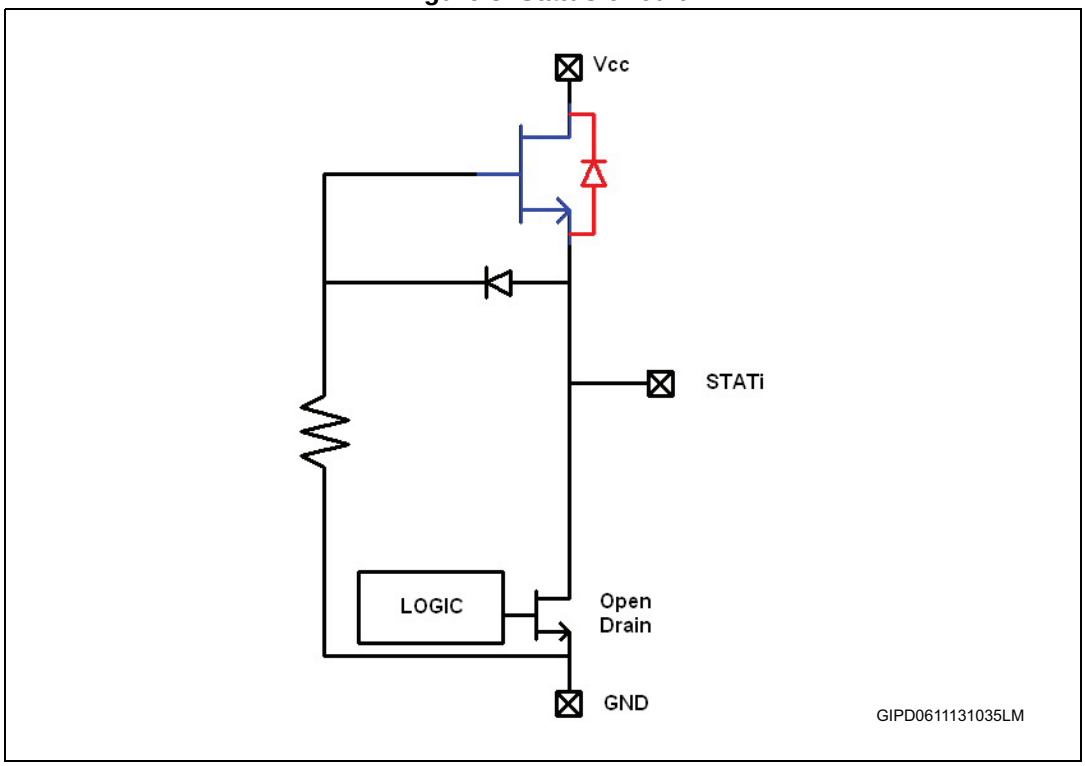

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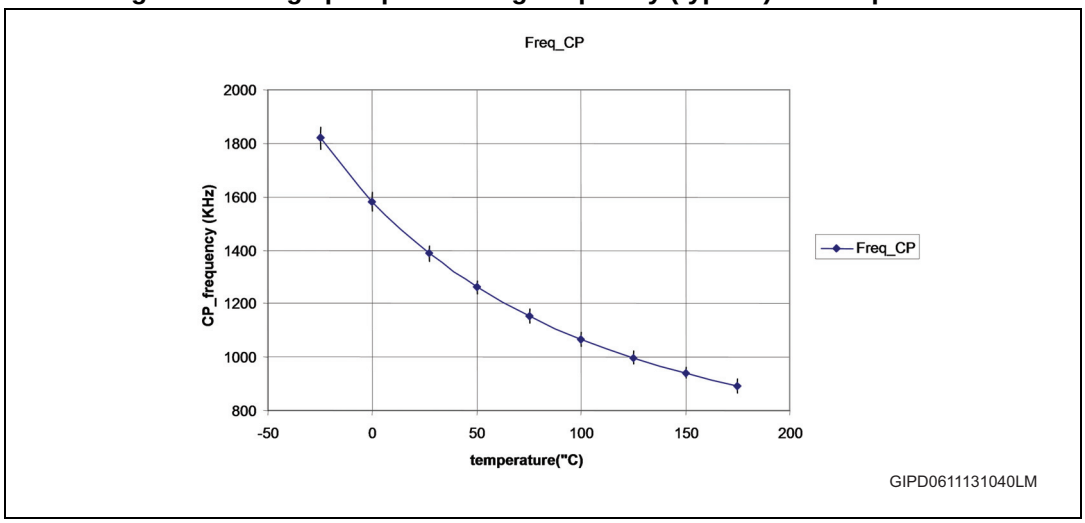
Figure 9. Charge pump switching frequency (typical) vs. temperature



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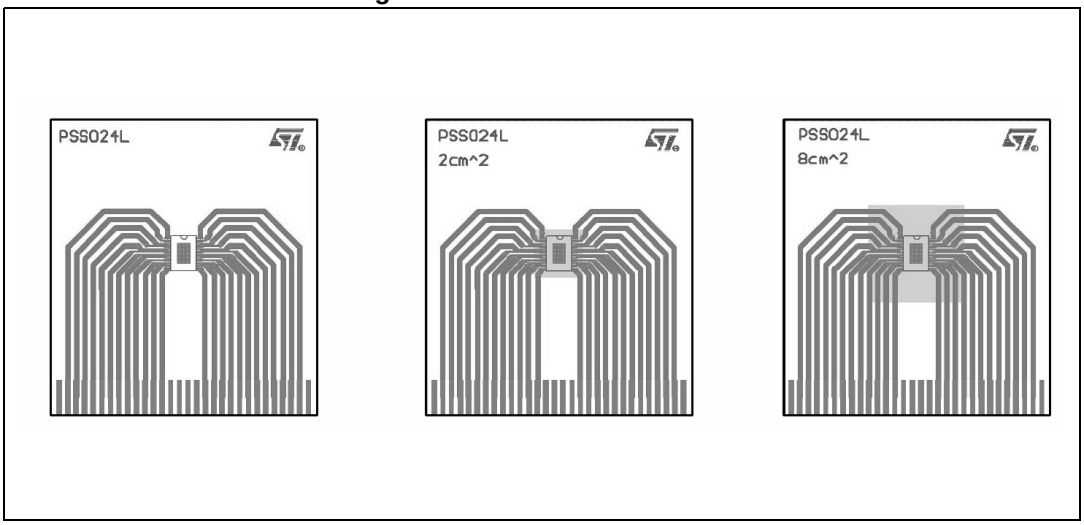
8 Package and PC board thermal data

8.1 VNI4140K thermal data

Figure 10. VNI4140K PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: double layer, thermal vias, FR4 area =77 mm x 86 mm, PCB thickness =1.6 mm, Cu thickness = 70 mm (front and back side), copper areas: from minimum pad layout to 8 cm^2).

Figure 11. $R_{th(JA)}$ vs. PCB copper area in open box free air condition (one channel ON)

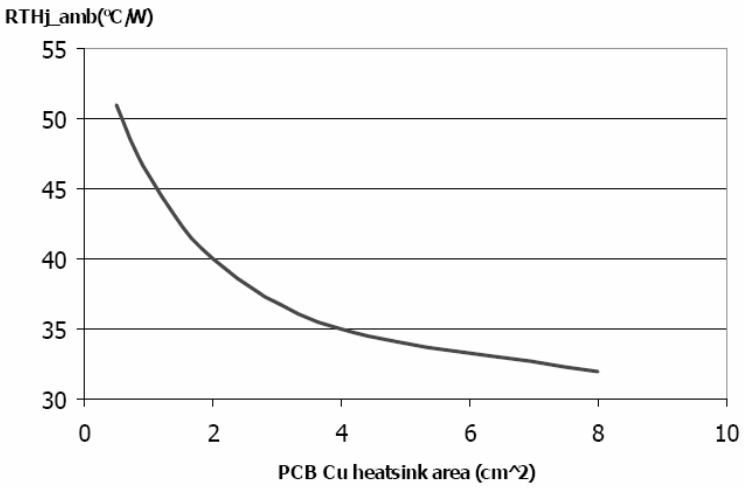


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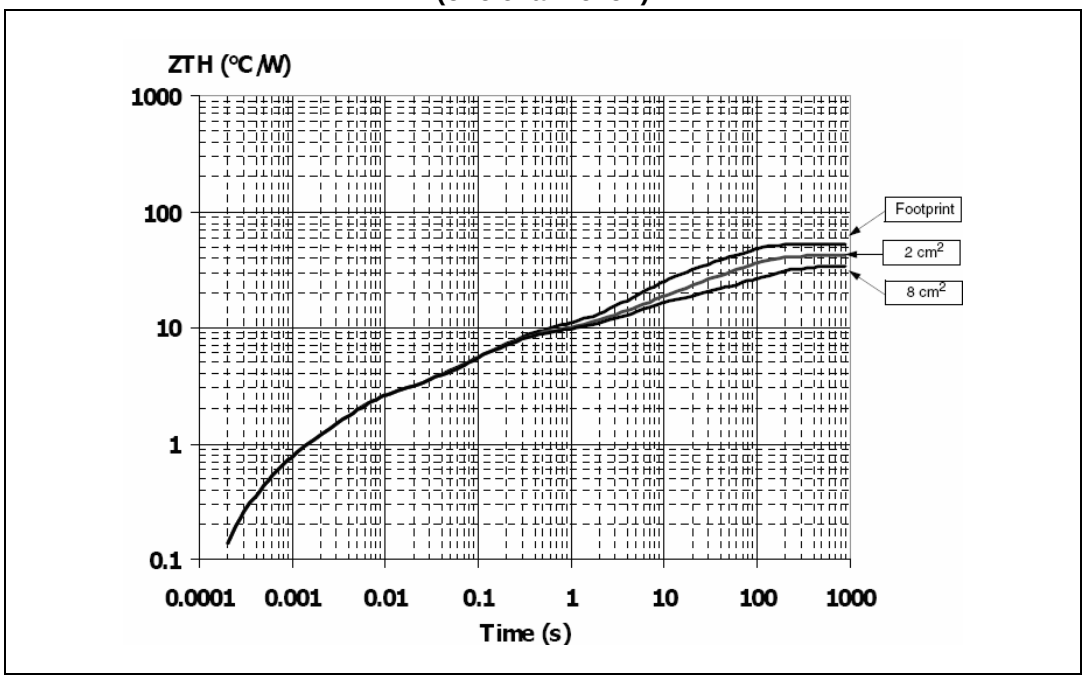
Figure 12. VNI4140K thermal impedance junction ambient single pulse (one channel on)



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9 Reverse polarity protection

Reverse polarity protection can be implemented on board using two different solutions:

1. Placing a resistor (R_{GND}) between IC GND pin and load GND
2. Placing a diode between IC GND pin and load GND

If option 1 is selected, the minimum resistance value has to be selected according to the following equation:

Equation 1

$R_{GND} \geq V_{CC}/I_{GND}$

where I_{GND} is the DC reverse ground pin current and can be found in *Section 2: Maximum ratings* of this datasheet.

Power dissipated by R_{GND} (when $V_{CC} < 0$: during reverse polarity situations) is:

Equation 2

$PD = (V_{CC})^2/R_{GND}$

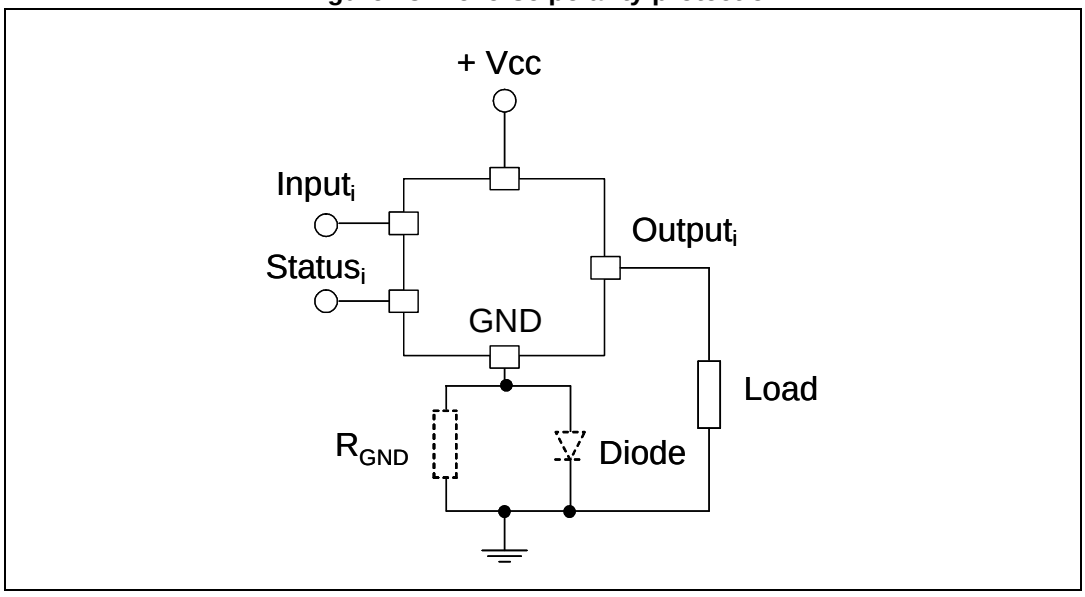
If option 2 is selected, the diode has to be chosen by taking into account VRRM >$|V_{cc}|$ and its power dissipation capability:

Equation 3

$P_D \geq I_S * V_f$

Note: In normal conditions (no reverse polarity) due to the diode, there is a voltage drop between GND of the device and GND of the system.

Figure 13. Reverse polarity protection



This schematic can be used with any type of load.

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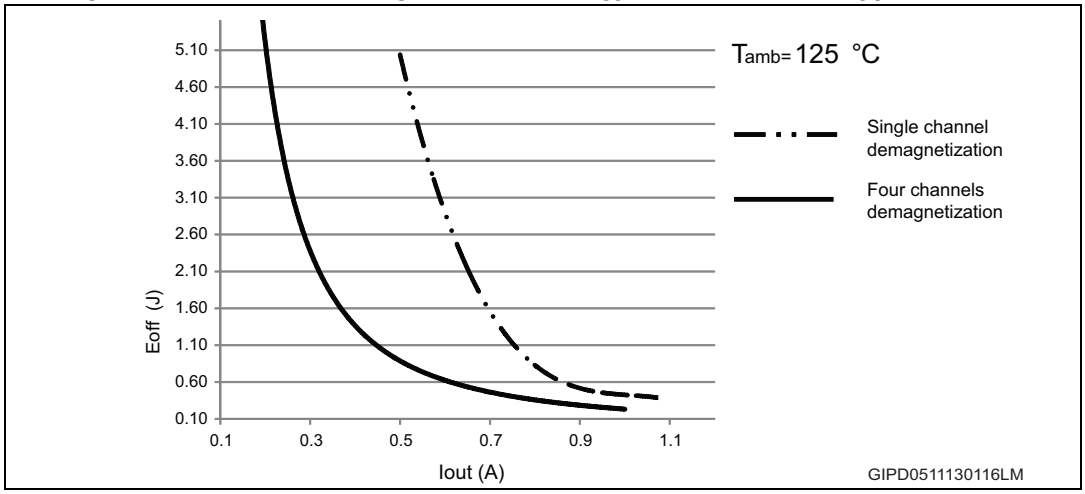
10 Demagnetization energy

Figure 14. Maximum demagnetization energy vs. load current, typical values



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11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. PowerSSO-24 mechanical data

Symbol	mm		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10deg
X	4.1		4.7
Y	6.5		7.1

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Figure 15. PowerSSO-24 package dimensions

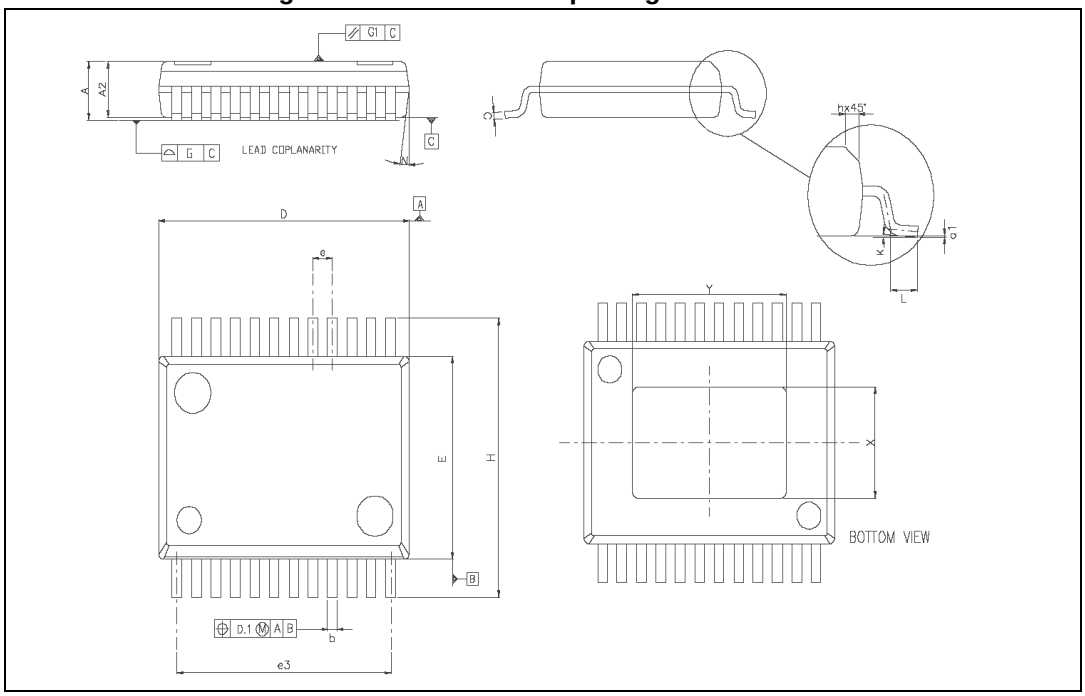

Figure 16. PowerSSO-24 tube shipment (no suffix)

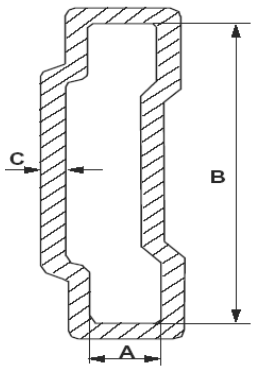

Table 10. PowerSSO-24 tube shipment

Base quantity	49
Bulk quantity	1225
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

Note: All dimensions are in mm.

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Figure 17. PowerSSO-24 reel shipment (suffix “TR”)

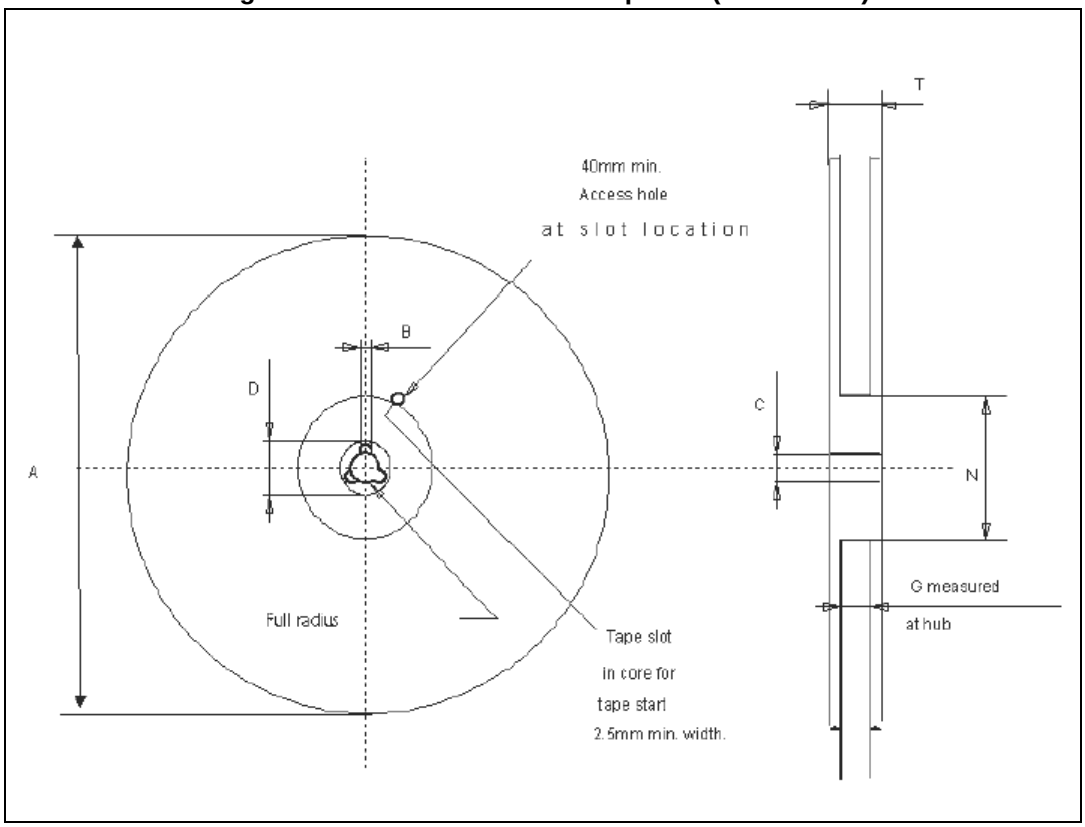

Table 11. PowerSSO-24 reel dimensions

Base quantity	1000
Bulk quantity	1000
A (max.)	330
B (min.)	1.5
C (± 0.2)	13
F	20.2
G (2 ± 0)	24.4
N (min.)	100
T (max.)	30.4

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Figure 18. PowerSSO-24™ tape dimensions

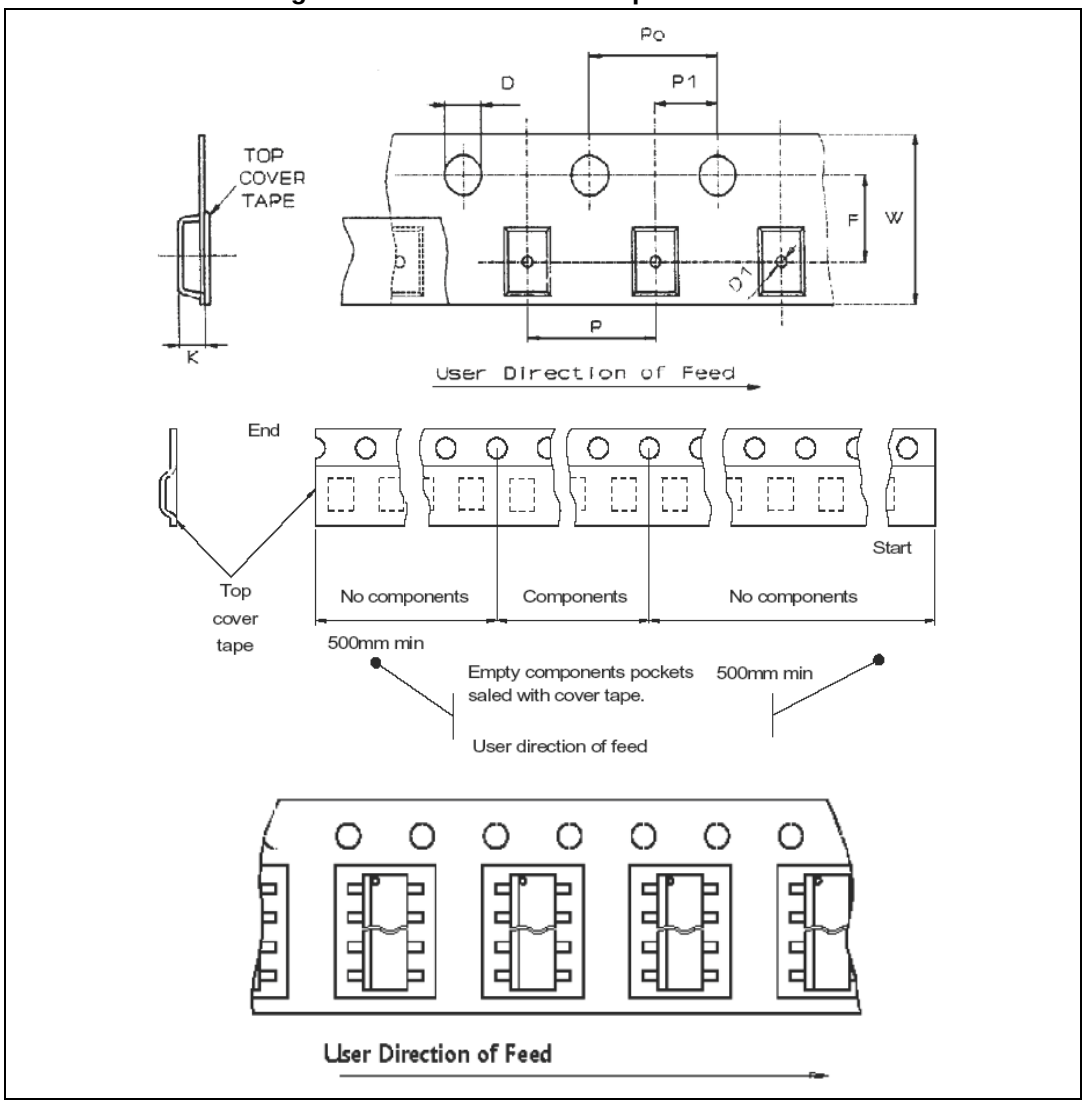

Table 12. PowerSSO-24™ tape dimensions

Tape width	W	24
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	12
Hole diameter	D (± 0.05)	1.55
Hole diameter	D1 (min.)	1.5
Hole position	F (± 0.1)	11.5
Compartment depth	K (max.)	2.85
Hole spacing	P1 (± 0.1)	2

Note: According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

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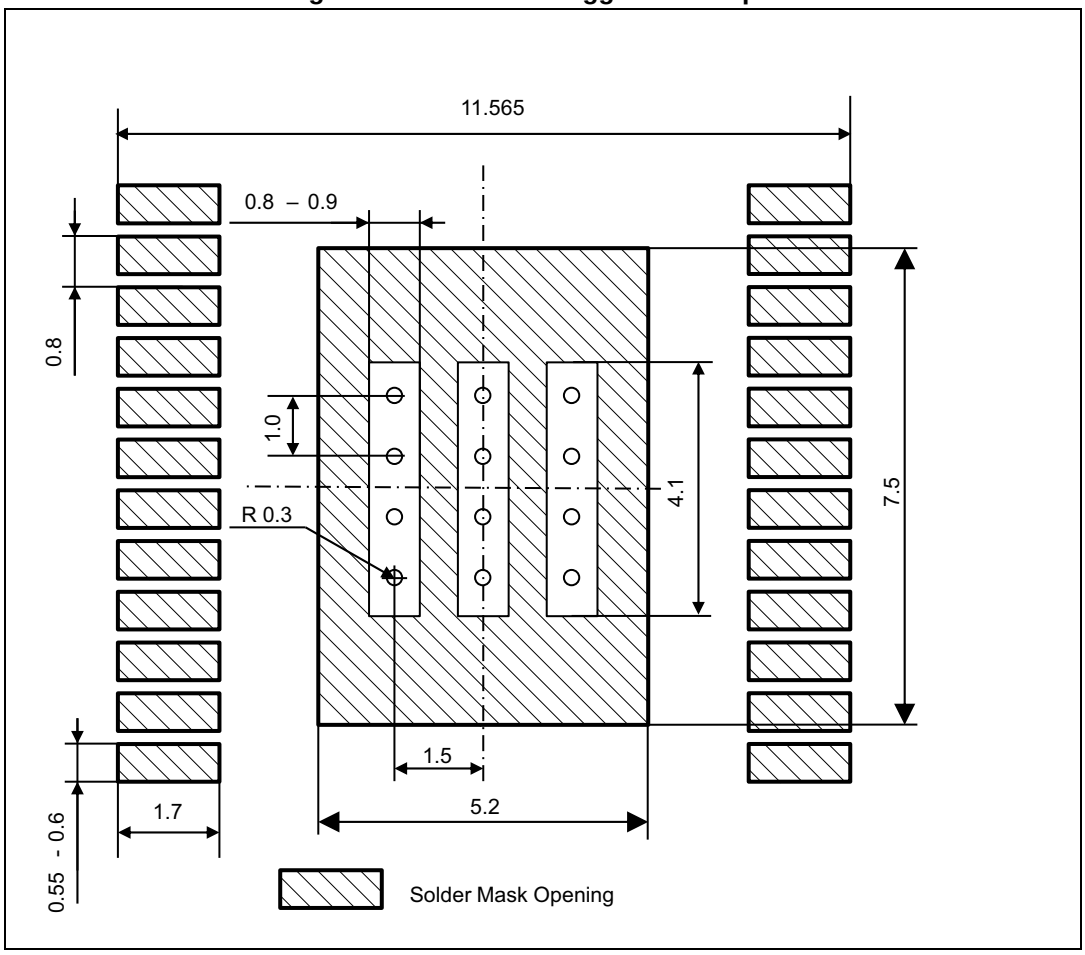
Figure 19. VN14140k suggested footprint



Note: STMicroelectronics is not responsible for any PCB related issues. The footprint shown in the above figure is a suggestion which might not be in line to the customer PCB supplier design rules.

All dimensions are in mm.

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12 Ordering information

Table 13. Order code

Order code	Package	Packaging
VNI4140K	PowerSSO-24	Tube
VNI4140KTR	PowerSSO-24	Tape and reel

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13 Revision history

Table 14. Document revision history

Date	Revision	Changes
16-Nov-2007	1	Initial release.
26-Nov-2007	2	Updated electrical parameters values.
08-Jul-2008	3	Inserted: *Figure 4 on page 9* and *Section 9: Reverse polarity protection on page 16*.
08-Apr-2008	4	Added I_{LGND} parameter in *Table 4 on page 6*.
27-Aug-2009	5	Updated *Section 9: Reverse polarity protection*.
09-Dec-2009	6	Added *Section 10: Conformity to IEC 61000-4-2 ESD immunity test.*
15-Apr-2010	7	Updated *Table 5 on page 6*.
06-Feb-2012	8	Inserted feature: conformity to IEC 61000-4-2 ESD immunity test in cover page. Removed chapter: conformity to IEC 61000-4-2 ESD immunity test.
05-Mar-2012	9	Suggested footprint inserted. In *Table 4* parameter I_{LGND} has been added.
19-Mar-2012	10	Minor text changes.
20-Dec-2012	11	Operating temperature range extended.
06-Nov-2013	12	Updated E_{AS} value in *Table 2: Absolute maximum ratings*. Added *Figure 14*.
11-Dec-2013	13	Updated *Section 9*.

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