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# 1 Block diagrams and pins configurations

Figure 1. VNL5090N3-E block diagram

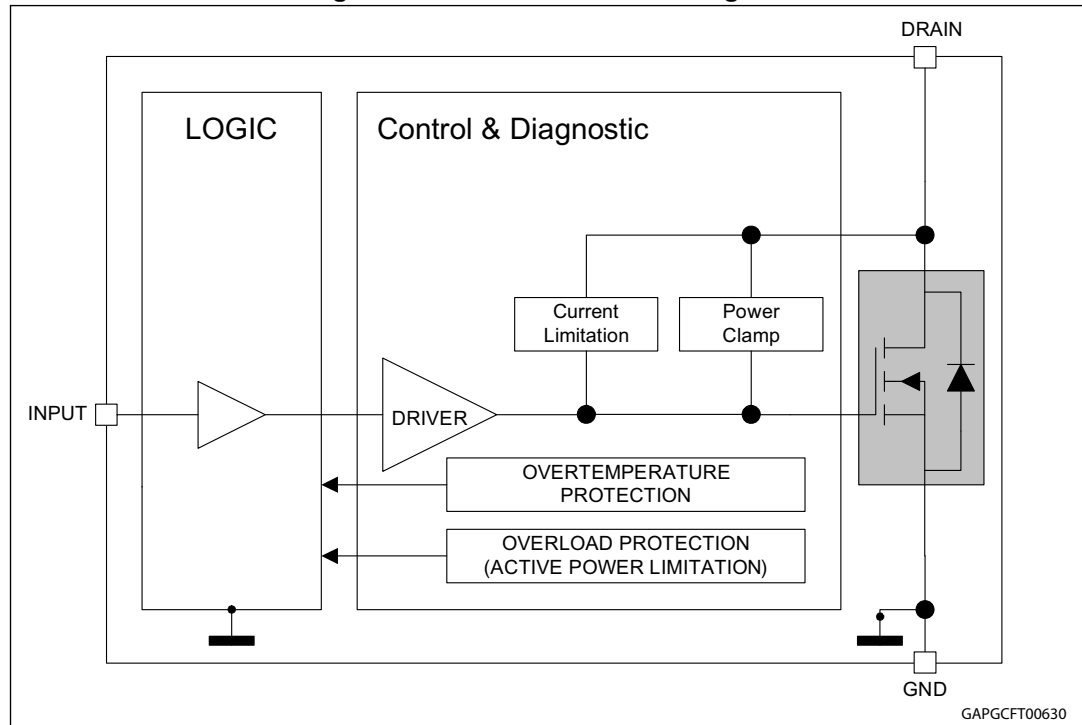


Figure 2. VNL5090S5-E block diagram

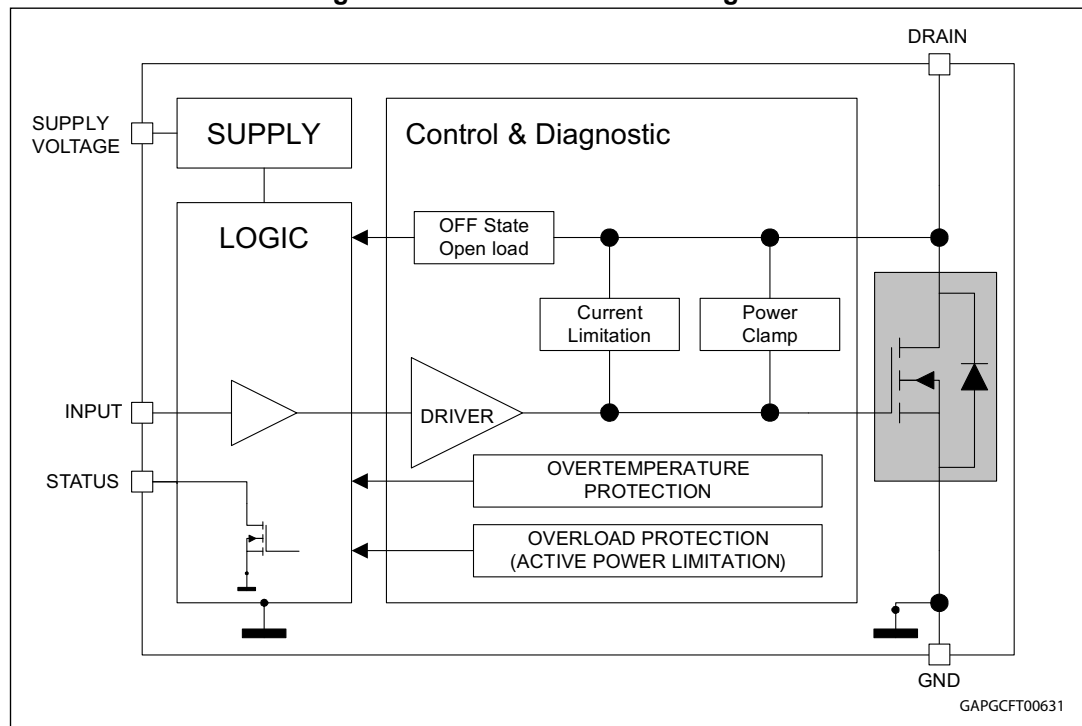


Table 2. Pin function

| Name           | Function                                                                                                      |
|----------------|---------------------------------------------------------------------------------------------------------------|
| INPUT          | Voltage controlled input pin with hysteresis, CMOS compatible; It controls output switch state <sup>(1)</sup> |
| DRAIN          | PowerMOS drain                                                                                                |
| SOURCE         | PowerMOS source and ground reference for the control section                                                  |
| SUPPLY VOLTAGE | Supply voltage connected to the signal part (5 V)                                                             |
| STATUS         | Open drain digital diagnostic pin <sup>(2)</sup>                                                              |

1. Internally connected to  $V_{supply}$  in the VNL5090N3-E  
2. Valid for VNL5090S5-E only.

Figure 3. VNL5090N3-E current and voltage conventions

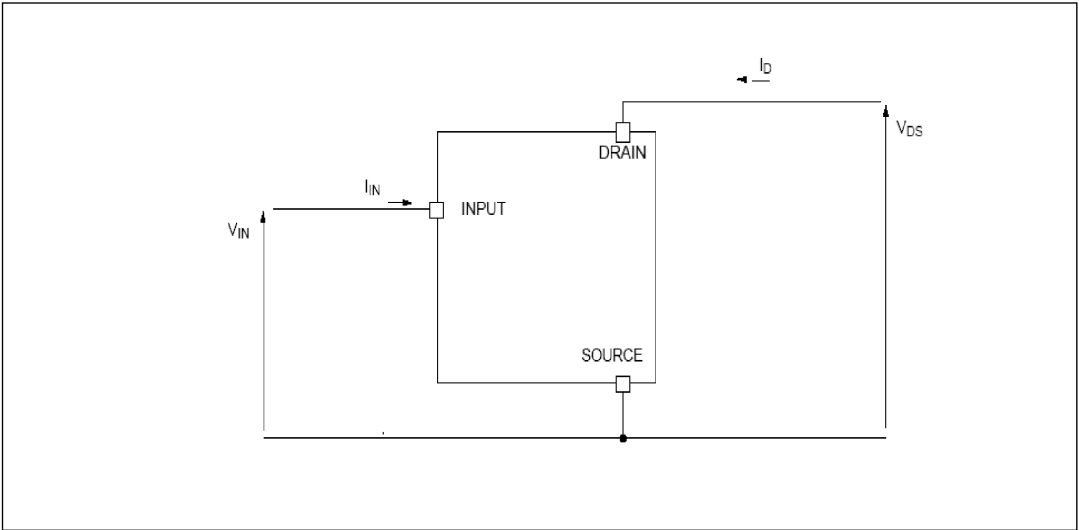


Figure 4. VNL5090S5-E current and voltage conventions

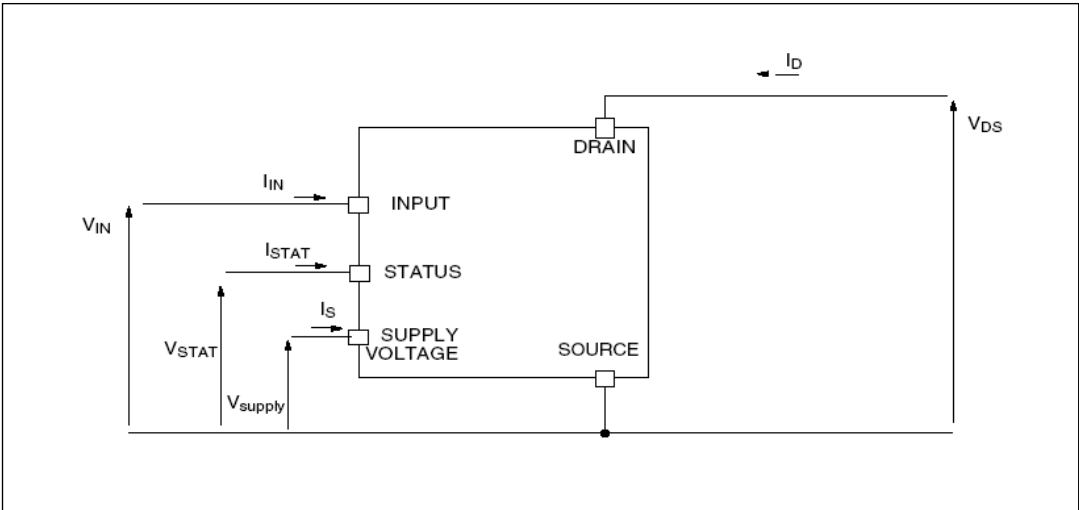


Figure 5. Configuration diagrams (top view)

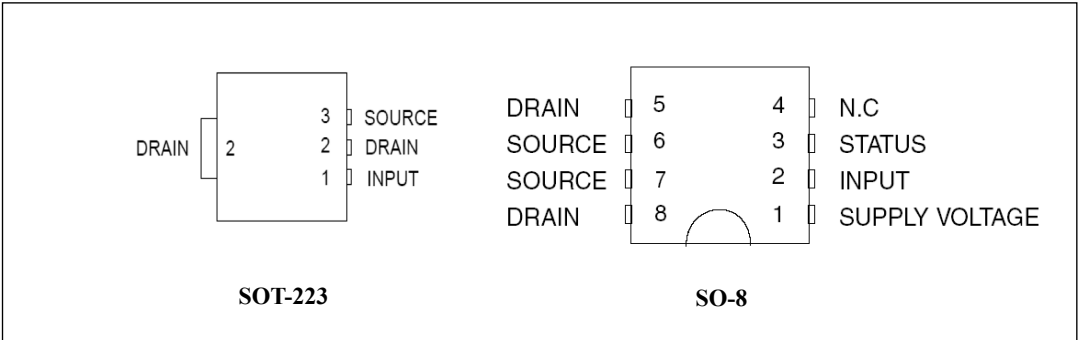


Table 3. Suggested connections for unused and N.C. pins

| Connection / pin | Status           | N.C. | Input                  |
|------------------|------------------|------|------------------------|
| Floating         | X <sup>(1)</sup> | X    | X                      |
| To ground        | Not allowed      | X    | Through 10 kΩ resistor |

1. X: do not care.

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

| Symbol     | Parameter                                                                                                               | Value              |          | Unit |
|------------|-------------------------------------------------------------------------------------------------------------------------|--------------------|----------|------|
|            |                                                                                                                         | SOT-223            | SO-8     |      |
| $V_{DS}$   | Drain-source voltage ( $V_{IN} = 0\text{ V}$ )                                                                          | Internally clamped |          | V    |
| $I_D$      | DC drain current                                                                                                        | Internally limited |          | A    |
| $-I_D$     | Reverse DC drain current                                                                                                | 12.5               |          | A    |
| $I_S$      | DC supply current                                                                                                       | —                  | -1 to 10 | mA   |
| $I_{IN}$   | DC input current                                                                                                        | -1 to 10           |          | mA   |
| $I_{STAT}$ | DC status current                                                                                                       | —                  | -1 to 10 | mA   |
| $V_{ESD1}$ | Electrostatic discharge<br>( $R = 1.5\text{ k}\Omega$ ; $C = 100\text{ pF}$ )                                           |                    |          |      |
|            | – DRAIN                                                                                                                 | 5000               |          | V    |
|            | – SUPPLY, INPUT, STATUS                                                                                                 | 4000               |          | V    |
| $V_{ESD2}$ | Electrostatic discharge on output pin only<br>( $R = 330\text{ }\Omega$ , $C = 150\text{ pF}$ )                         | 2000               |          | V    |
| $T_j$      | Junction operating temperature                                                                                          | -40 to 150         |          | °C   |
| $T_{stg}$  | Storage temperature                                                                                                     | -55 to 150         |          | °C   |
| $E_{AS}$   | Single pulse avalanche energy<br>( $L = 1.1\text{ mH}$ , $T_j = 150^\circ\text{C}$ , $R_L = 0$ , $I_{OUT} = I_{limL}$ ) | 50                 |          | mJ   |

### 2.2 Thermal data

**Table 5. Thermal data**

| Symbol        | Parameter                           | Maximum value      |      | Unit |
|---------------|-------------------------------------|--------------------|------|------|
|               |                                     | SOT-223            | SO-8 |      |
| $R_{thj-amb}$ | Thermal resistance junction-ambient | 147 <sup>(1)</sup> | 102  | °C/W |

1. When mounted on a standard single-sided FR4 board with 0.5 cm<sup>2</sup> of Cu (at least 35  $\mu\text{m}$  thick) connected to all DRAIN pins

## 2.3 Electrical characteristics

Values specified in this section are for  $V_{\text{supply}} = V_{\text{IN}} = 4.5 \text{ V}$  to  $5.5 \text{ V}$ ,  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ , unless otherwise stated.

**Table 6. PowerMOS section**

| Symbol              | Parameter                            | Test conditions                                                                                                  | Min. | Typ. | Max. | Unit             |
|---------------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------|------|------|------|------------------|
| $V_{\text{supply}}$ | Operating supply voltage             |                                                                                                                  | 3.5  | 5    | 5.5  | V                |
| $R_{\text{ON}}$     | ON-state resistance                  | $I_D = 1.6 \text{ A}$ ; $T_j = 25^\circ\text{C}$ ;<br>$V_{\text{supply}} = V_{\text{IN}} = 5 \text{ V}$          |      |      | 90   | $\text{m}\Omega$ |
|                     |                                      | $I_D = 1.6 \text{ A}$ ; $T_j = 150^\circ\text{C}$ ;<br>$V_{\text{supply}} = V_{\text{IN}} = 5 \text{ V}$         |      |      | 180  |                  |
|                     |                                      | $I_D = 1.6 \text{ A}$ ; $T_j = 150^\circ\text{C}$ ;<br>$V_{\text{supply}} = V_{\text{IN}} = 4.5 \text{ V}^{(1)}$ |      |      | 190  |                  |
| $V_{\text{CLAMP}}$  | Drain-source clamp voltage           | $V_{\text{IN}} = 0 \text{ V}$ ; $I_D = 1.6 \text{ A}$                                                            | 41   | 46   | 52   | V                |
| $V_{\text{CLTH}}$   | Drain-source clamp threshold voltage | $V_{\text{IN}} = 0 \text{ V}$ ; $I_D = 2 \text{ mA}$                                                             | 36   |      |      | V                |
| $I_{\text{DSS}}$    | OFF-state output current             | $V_{\text{IN}} = 0 \text{ V}$ ; $V_{\text{DS}} = 13 \text{ V}$ ;<br>$T_j = 25^\circ\text{C}$                     | 0    |      | 3    | $\mu\text{A}$    |
|                     |                                      | $V_{\text{IN}} = 0 \text{ V}$ ; $V_{\text{DS}} = 13 \text{ V}$ ;<br>$T_j = 125^\circ\text{C}$                    | 0    |      | 5    |                  |

1. Valid only for VNL5090N3-E.

**Table 7. Source drain diode**

| Symbol          | Parameter          | Test conditions                                       | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|-------------------------------------------------------|------|------|------|------|
| $V_{\text{SD}}$ | Forward on voltage | $I_D = 1.6 \text{ A}$ ; $V_{\text{IN}} = 0 \text{ V}$ | —    | 0.8  | —    | V    |

**Table 8. Input section (VNL5090N3-E only)**

| Symbol            | Parameter                     | Test conditions                                                                                | Min. | Typ. | Max. | Unit          |
|-------------------|-------------------------------|------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{\text{ISS}}$  | Supply current from input pin | ON-state: $V_{\text{supply}} = V_{\text{IN}} = 5 \text{ V}$ ;<br>$V_{\text{DS}} = 0 \text{ V}$ |      | 30   | 65   | $\mu\text{A}$ |
| $V_{\text{ICL}}$  | Input clamp voltage           | $I_S = 1 \text{ mA}$                                                                           | 5.5  |      | 7    | V             |
|                   |                               | $I_S = -1 \text{ mA}$                                                                          |      | -0.7 |      |               |
| $V_{\text{INTH}}$ | Input threshold voltage       | $V_{\text{DS}} = V_{\text{IN}}$ ; $I_D = 1 \text{ mA}$                                         | 1    |      | 3.5  | V             |

**Table 9. Status pin (VNL5090S5-E only)**

| Symbol             | Parameter                 | Test conditions                                      | Min. | Typ. | Max. | Unit          |
|--------------------|---------------------------|------------------------------------------------------|------|------|------|---------------|
| $V_{\text{STAT}}$  | Status low output voltage | $I_{\text{STAT}} = 1 \text{ mA}$                     |      |      | 0.5  | V             |
| $I_{\text{LSTAT}}$ | Status leakage current    | Normal operation,<br>$V_{\text{STAT}} = 5 \text{ V}$ |      |      | 10   | $\mu\text{A}$ |

Table 9. Status pin (VNL5090S5-E only) (continued)

| Symbol     | Parameter                    | Test conditions                              | Min. | Typ. | Max. | Unit |
|------------|------------------------------|----------------------------------------------|------|------|------|------|
| $C_{STAT}$ | Status pin input capacitance | Normal operation,<br>$V_{STAT} = 5\text{ V}$ |      |      | 100  | pF   |
| $V_{STCL}$ | Status clamp voltage         | $I_{STAT} = 1\text{ mA}$                     | 5.5  |      | 7    | V    |
|            |                              | $I_{STAT} = -1\text{ mA}$                    |      | -0.7 |      |      |

Table 10. Logic input (VNL5090S5-E only)

| Symbol        | Parameter                | Test conditions         | Min. | Typ. | Max. | Unit          |
|---------------|--------------------------|-------------------------|------|------|------|---------------|
| $V_{IL}$      | Low-level input voltage  |                         |      |      | 0.9  | V             |
| $I_{IL}$      | Low-level input current  | $V_{IN} = 0.9\text{ V}$ | 1    |      |      | $\mu\text{A}$ |
| $V_{IH}$      | High-level input voltage |                         | 2.1  |      |      | V             |
| $I_{IH}$      | High-level input current | $V_{IN} = 2.1\text{ V}$ |      |      | 10   | $\mu\text{A}$ |
| $V_{I(hyst)}$ | Input hysteresis voltage |                         | 0.13 |      |      | V             |
| $V_{ICL}$     | Input clamp voltage      | $I_{IN} = 1\text{ mA}$  | 5.5  |      | 7    | V             |
|               |                          | $I_{IN} = -1\text{ mA}$ |      | -0.7 |      |               |

Table 11. Openload detection (VNL5090S5-E only)

| Symbol         | Parameter                                                                      | Test conditions        | Min. | Typ. | Max. | Unit          |
|----------------|--------------------------------------------------------------------------------|------------------------|------|------|------|---------------|
| $V_{OI}$       | Openload OFF-state voltage detection threshold                                 | $V_{IN} = 0\text{ V}$  | 0.6  | 1.2  | 1.7  | V             |
| $t_{d(oloff)}$ | Delay between INPUT falling edge and STATUS falling edge in openload condition | $I_{OUT} = 0\text{ A}$ | 45   | 425  | 1100 | $\mu\text{s}$ |

Table 12. Supply section (VNL5090S5-E only)

| Symbol    | Parameter            | Test conditions                                                              | Min. | Typ. | Max. | Unit          |
|-----------|----------------------|------------------------------------------------------------------------------|------|------|------|---------------|
| $I_S$     | Supply current       | OFF-state; $T_j = 25^\circ\text{C}$ ;<br>$V_{IN} = V_{DRAIN} = 0\text{ V}$ ; |      | 10   | 25   | $\mu\text{A}$ |
|           |                      | ON-state; $V_{IN} = 5\text{ V}$ ; $V_{DS} = 0\text{ V}$                      |      | 25   | 65   |               |
| $V_{SCL}$ | Supply clamp voltage | $I_{SCL} = 1\text{ mA}$                                                      | 5.5  |      | 7    | V             |
|           |                      | $I_{SCL} = -1\text{ mA}$                                                     |      | -0.7 |      |               |

Table 13. Switching characteristics

| Symbol       | Parameter                           | Test conditions                               | SOT-223 <sup>(1)</sup> |      |     | SO-8 |      |      | Unit    |
|--------------|-------------------------------------|-----------------------------------------------|------------------------|------|-----|------|------|------|---------|
|              |                                     |                                               | Min.                   | Typ. | Max | Min. | Typ. | Max. |         |
| $t_{d(ON)}$  | Turn-on delay time                  | $R_L = 8.2 \Omega$ ,<br>$V_{CC} = 13 V^{(2)}$ | —                      | 8    | —   | —    | 8    | —    | $\mu s$ |
| $t_{d(OFF)}$ | Turn-off delay time                 | $R_L = 8.2 \Omega$ ,<br>$V_{CC} = 13 V^{(2)}$ | —                      | 3.4  | —   | —    | 18   | —    | $\mu s$ |
| $t_r$        | Rise time                           | $R_L = 8.2 \Omega$ ,<br>$V_{CC} = 13 V^{(2)}$ | —                      | 10   | —   | —    | 10   | —    | $\mu s$ |
| $t_f$        | Fall time                           | $R_L = 8.2 \Omega$ ,<br>$V_{CC} = 13 V^{(2)}$ | —                      | 2.7  | —   | —    | 10   | —    | $\mu s$ |
| $W_{ON}$     | Switching energy losses at turn-on  | $R_L = 8.2 \Omega$ ,<br>$V_{CC} = 13 V^{(2)}$ | —                      | 57   | —   | —    | 57   | —    | $\mu J$ |
| $W_{OFF}$    | Switching energy losses at turn-off | $R_L = 8.2 \Omega$ ,<br>$V_{CC} = 13 V^{(2)}$ | —                      | 14   | —   | —    | 55   | —    | $\mu J$ |

1.  $3.5 V \leq V_{supply} = V_{IN} \leq 5.5 V$

2. See [Figure 6: Switching characteristics](#)

Note:

See [Figure 7: VNL5090N3-E application schematic](#) and [Figure 8: VNL5090S5-E application schematic](#)

Table 14. Protection and diagnostics

| Symbol         | Parameter                                    | Test conditions <sup>(1)</sup>                                           | Min.         | Typ.         | Max. | Unit        |
|----------------|----------------------------------------------|--------------------------------------------------------------------------|--------------|--------------|------|-------------|
| $I_{limH}$     | DC short-circuit current                     | $V_{DS} = 13 V$ ;<br>$V_{supply} = V_{IN} = 5 V$                         | 13           | 18           | 25   | A           |
| $I_{limL}$     | Short-circuit current during thermal cycling | $V_{DS} = 13 V$ ; $T_R < T_J < T_{TSD}$ ;<br>$V_{supply} = V_{IN} = 5 V$ |              | 8            |      | A           |
| $t_{dimL}$     | Step response current limit                  | $V_{DS} = 13 V$ ; $V_{input} = 5 V$                                      |              | 44           |      | $\mu s$     |
| $T_{TSD}$      | Shutdown temperature                         |                                                                          | 150          | 175          | 200  | $^{\circ}C$ |
| $T_R^{(2)}$    | Reset temperature                            |                                                                          | $T_{RS} + 1$ | $T_{RS} + 5$ |      | $^{\circ}C$ |
| $T_{RS}^{(2)}$ | Thermal reset of STATUS                      |                                                                          | 135          |              |      | $^{\circ}C$ |
| $T_{HYST}$     | Thermal hysteresis ( $T_{TSD} - T_R$ )       |                                                                          |              | 7            |      | $^{\circ}C$ |

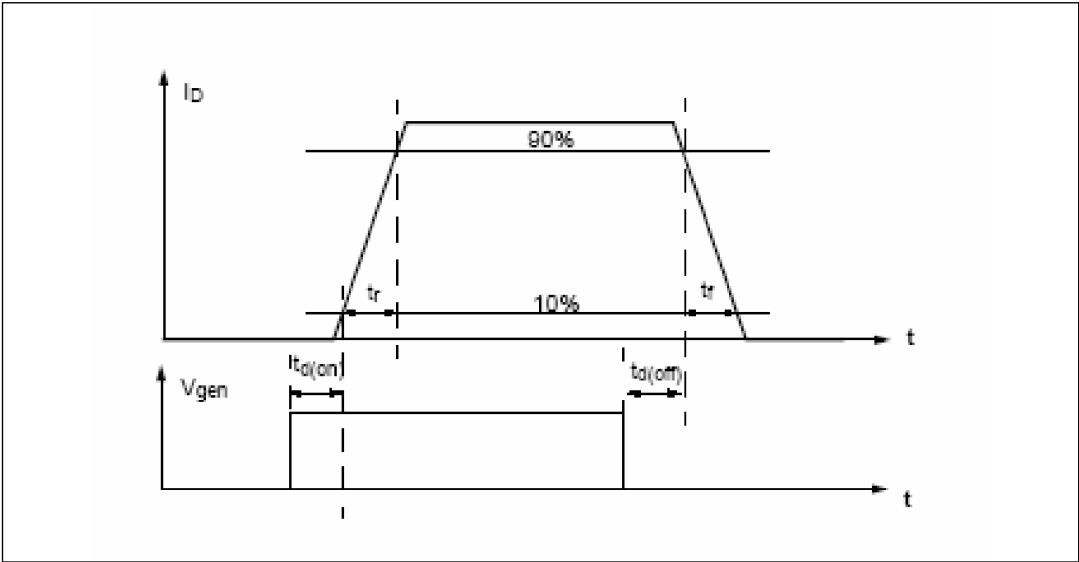
1.  $V_{supply} = V_{input}$  in VNL5090N3-E version.

2. Valid for VNL5090S5-E option.

Table 15. Truth table (VNL5090S5-E only)

| Conditions                       | INPUT | DRAIN | STATUS |
|----------------------------------|-------|-------|--------|
| Normal operation                 | L     | H     | H      |
|                                  | H     | L     | H      |
| Current limitation               | L     | H     | H      |
|                                  | H     | X     | H      |
| Overtemperature                  | L     | H     | H      |
|                                  | H     | H     | L      |
| Undervoltage                     | L     | H     | X      |
|                                  | H     | H     | X      |
| Output voltage < V <sub>OL</sub> | L     | L     | L      |
|                                  | H     | L     | H      |

Figure 6. Switching characteristics



### 3 Application information

Figure 7. VNL5090N3-E application schematic

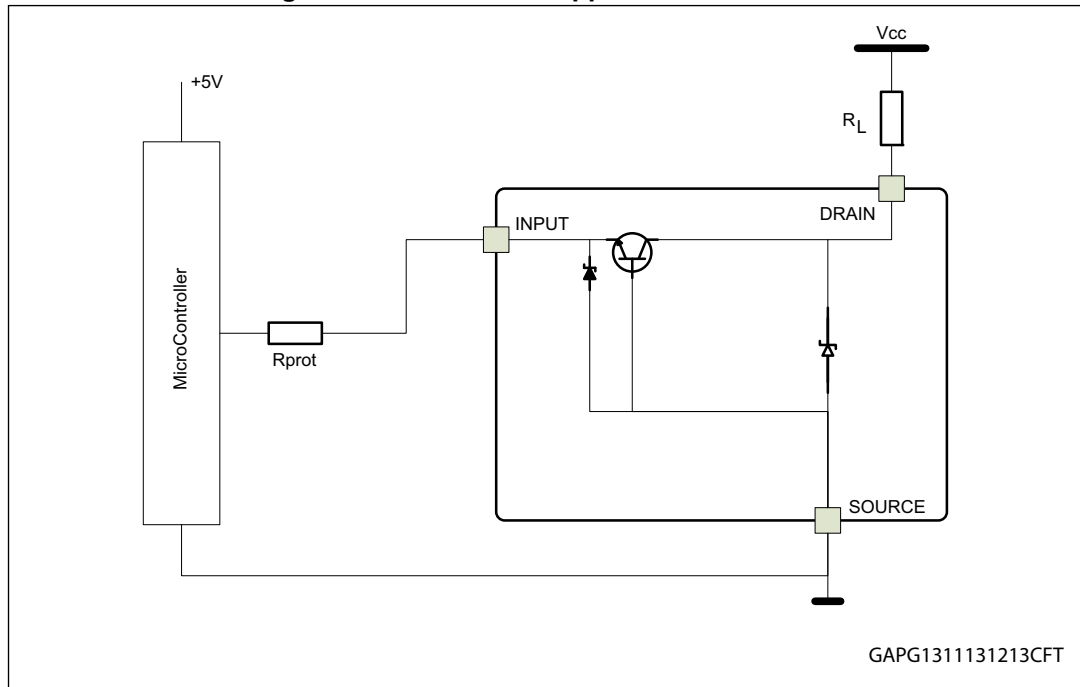
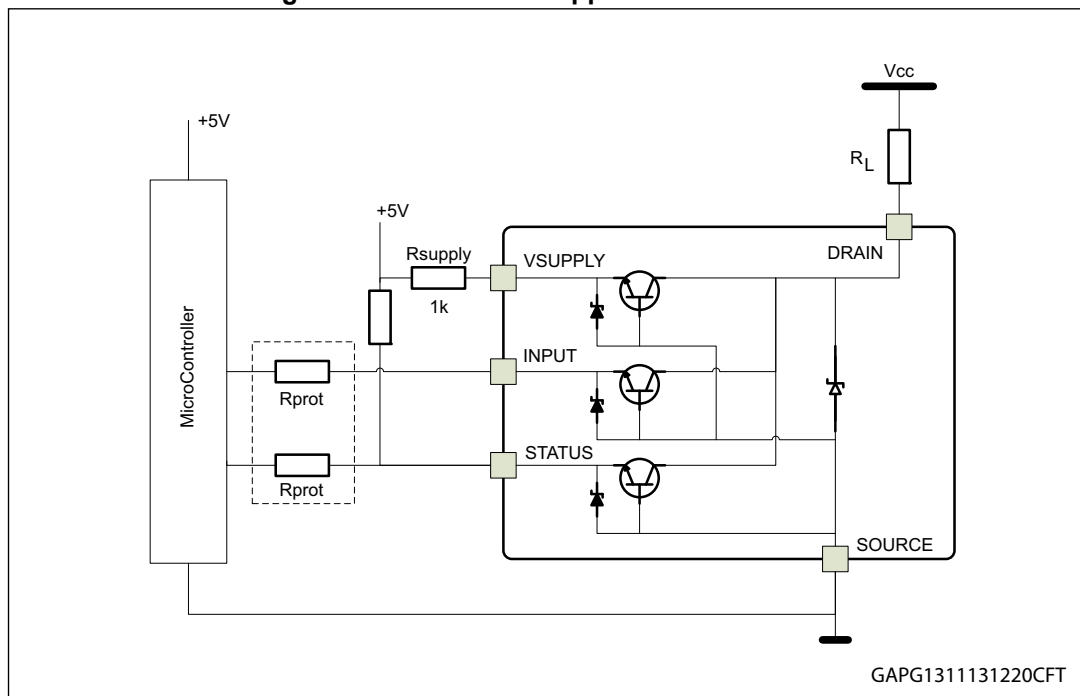


Figure 8. VNL5090S5-E application schematic



### 3.1 MCU I/O protection

ST suggests to insert a resistor ( $R_{\text{prot}}$ ) in line to prevent the microcontroller I/O pins from latching up<sup>(a)</sup>. The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the LSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os:

#### Equation 1

$$\frac{0.7}{I_{\text{latchup}}} \leq R_{\text{prot}} \leq \frac{(V_{\text{OH}\mu\text{C}} - V_{\text{IH}})}{I_{\text{IH max}}}$$

Let:

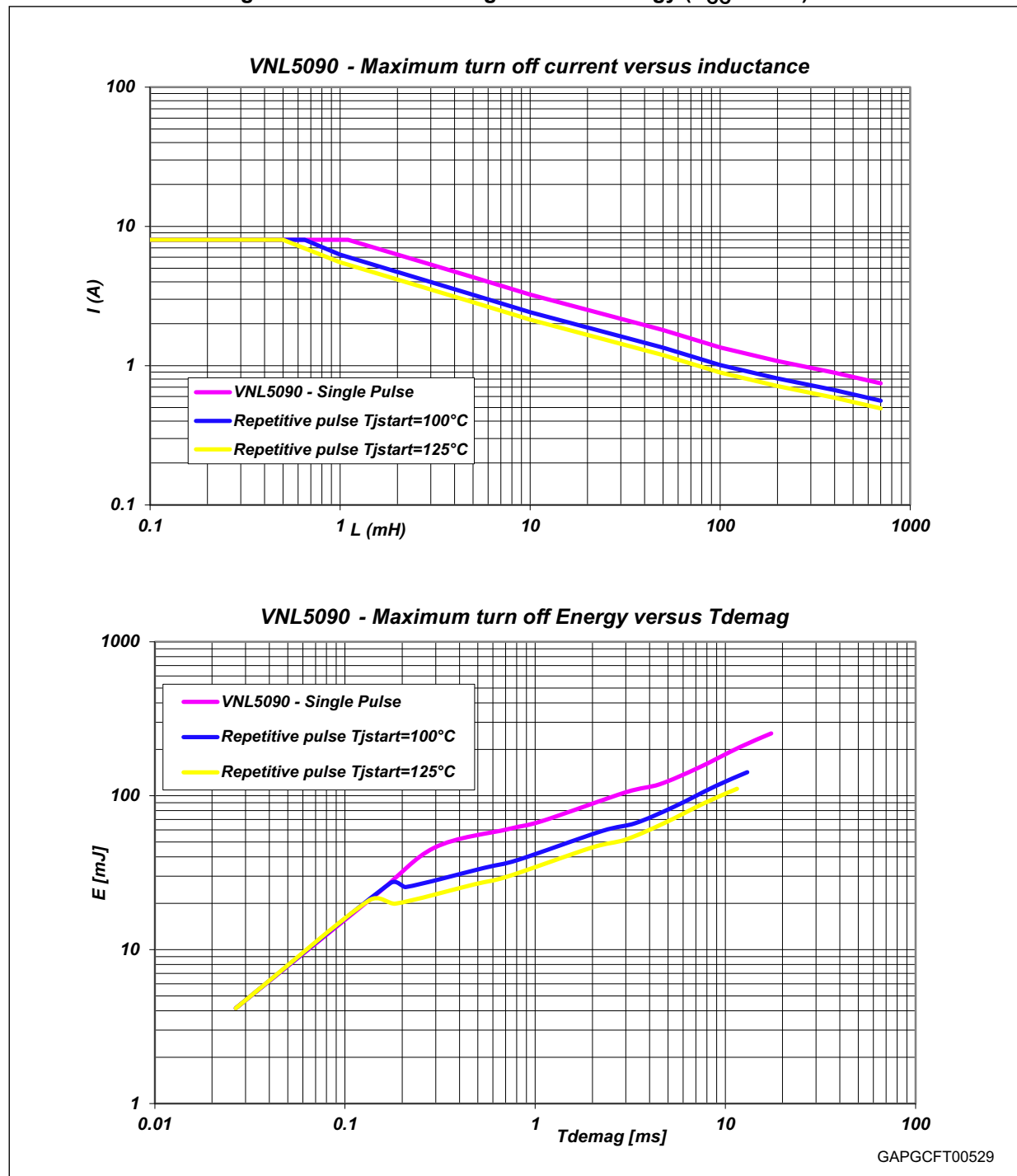
- $I_{\text{latchup}} \geq 20 \text{ mA}$
- $V_{\text{OH}\mu\text{C}} \geq 4.5 \text{ V}$
- $35 \Omega \leq R_{\text{prot}} \leq 100 \text{ K}\Omega$

Then, the recommended value is  $R_{\text{prot}} = 1 \text{ K}\Omega$

*Figure 9* shows the turn-off current drawn during the demagnetization.

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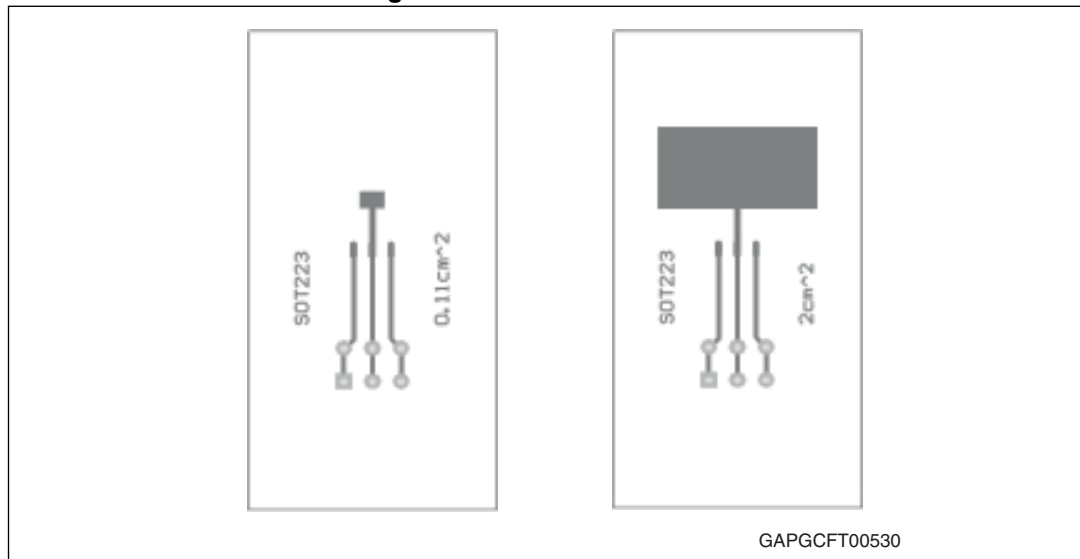
a. In case of negative transient on the drain pin.

Figure 9. Maximum demagnetization energy ( $V_{CC} = 16\text{ V}$ )

## 4 Package and PC board thermal data

### 4.1 SOT-223 thermal data

Figure 10. SOT-223 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area = 30 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35  $\mu$ m, copper areas: from minimum pad lay-out to 0.8 cm<sup>2</sup>).

Figure 11. SOT-223  $R_{thj-amb}$  vs PCB copper area in open box free air condition

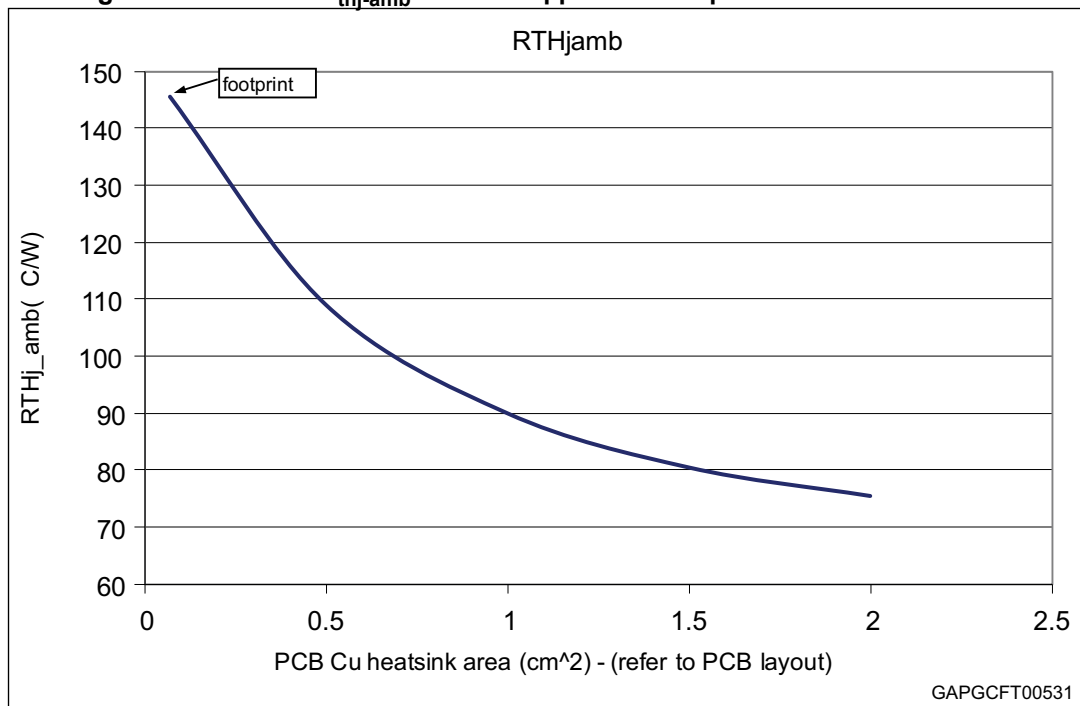
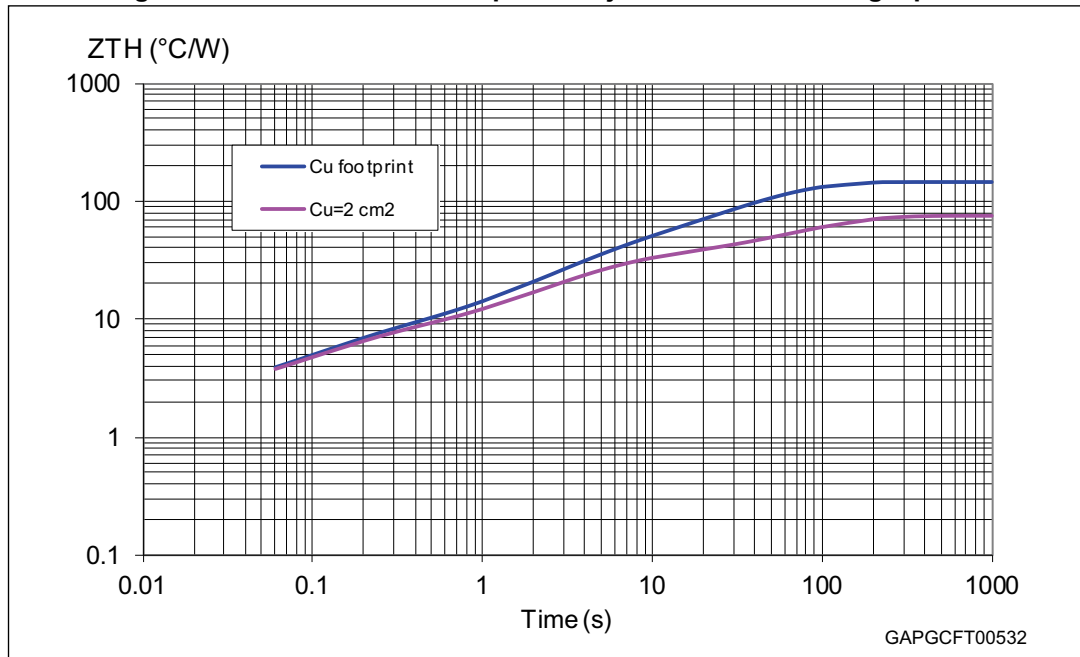


Figure 12. SOT-223 thermal impedance junction ambient single pulse

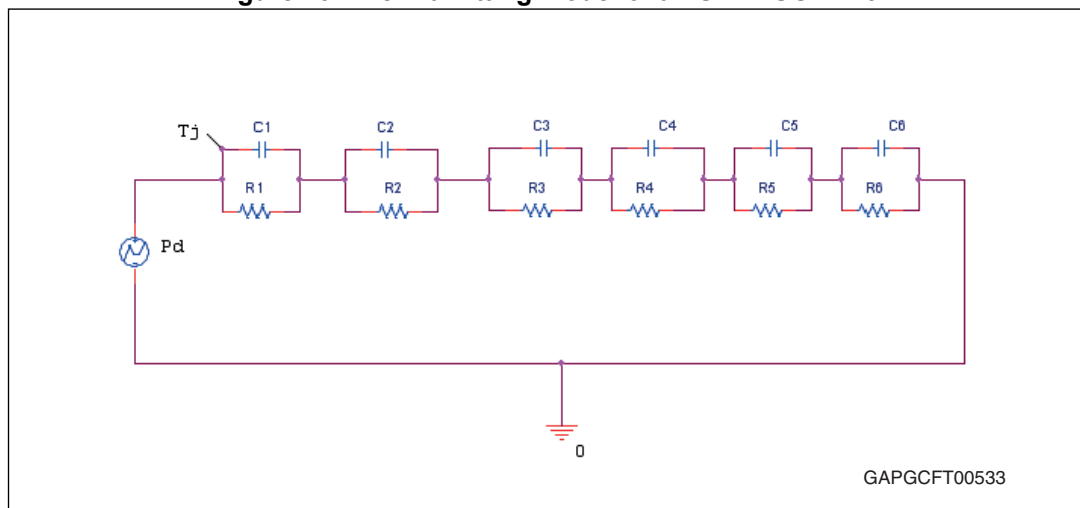


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$ 

Figure 13. Thermal fitting model of a LSD in SOT-223



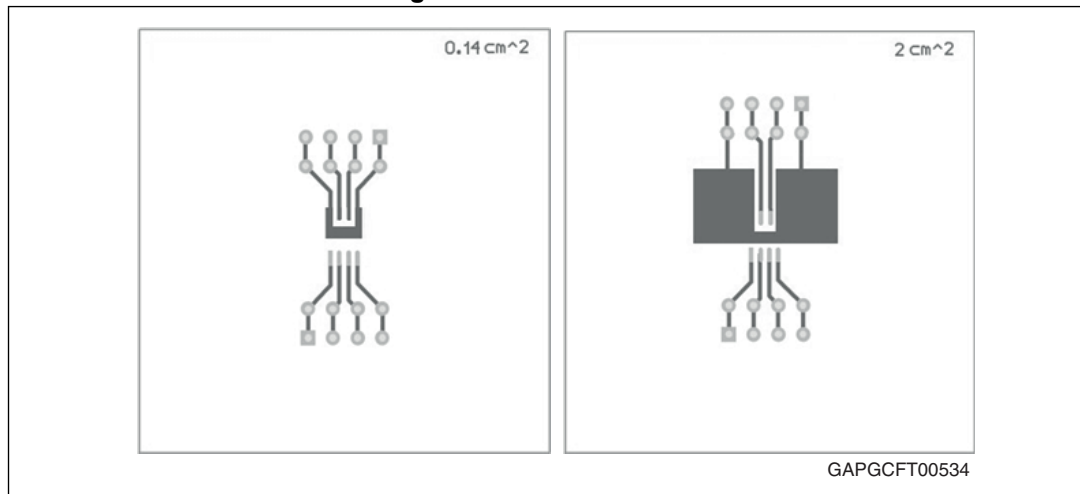
**Note:** The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. SOT-223 thermal parameters

| Area/island (cm <sup>2</sup> ) | Footprint | 2  |
|--------------------------------|-----------|----|
| R1 (°C/W)                      | 0.8       |    |
| R2 (°C/W)                      | 1         |    |
| R3 (°C/W)                      | 4.5       |    |
| R4 (°C/W)                      | 24        |    |
| R5 (°C/W)                      | 0.1       |    |
| R6 (°C/W)                      | 115       | 45 |
| C1 (W.s/°C)                    | 0.00004   |    |
| C2 (W.s/°C)                    | 0.0003    |    |
| C3 (W.s/°C)                    | 0.03      |    |
| C4 (W.s/°C)                    | 0.16      |    |
| C5 (W.s/°C)                    | 1000      |    |
| C6 (W.s/°C)                    | 0.4       | 2  |

## 4.2 SO-8 thermal data

Figure 14. SO-8 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35  $\mu$ m (front and back side), Copper areas: from minimum pad lay-out to 2 cm<sup>2</sup>).

Figure 15. SO-8  $R_{thj-amb}$  vs PCB copper area in open box free air condition

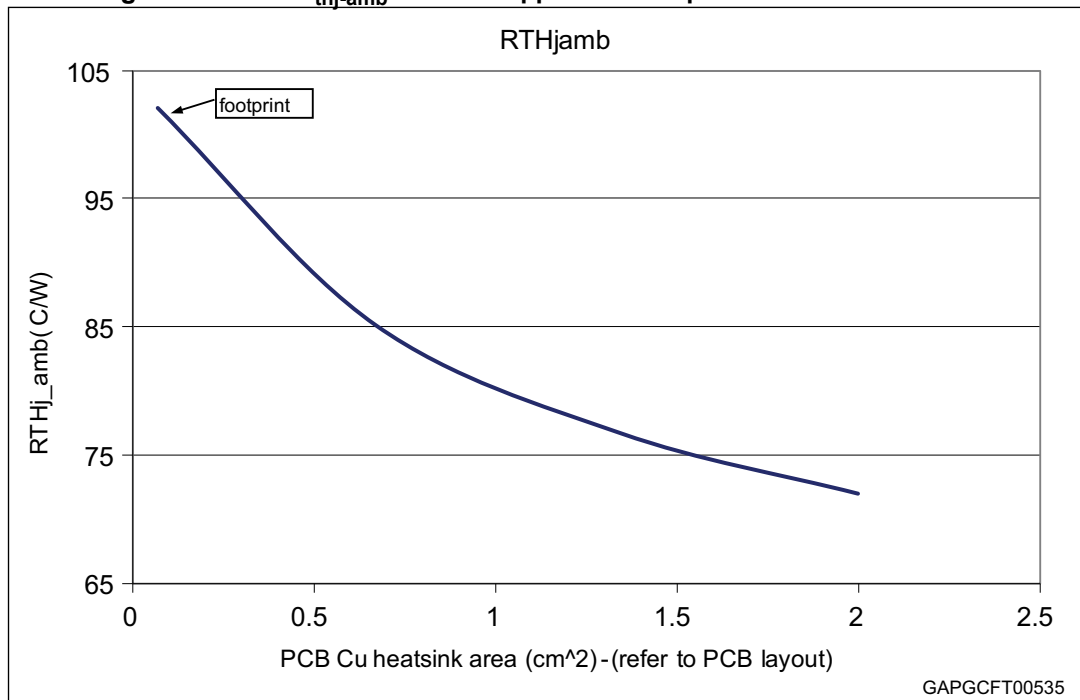
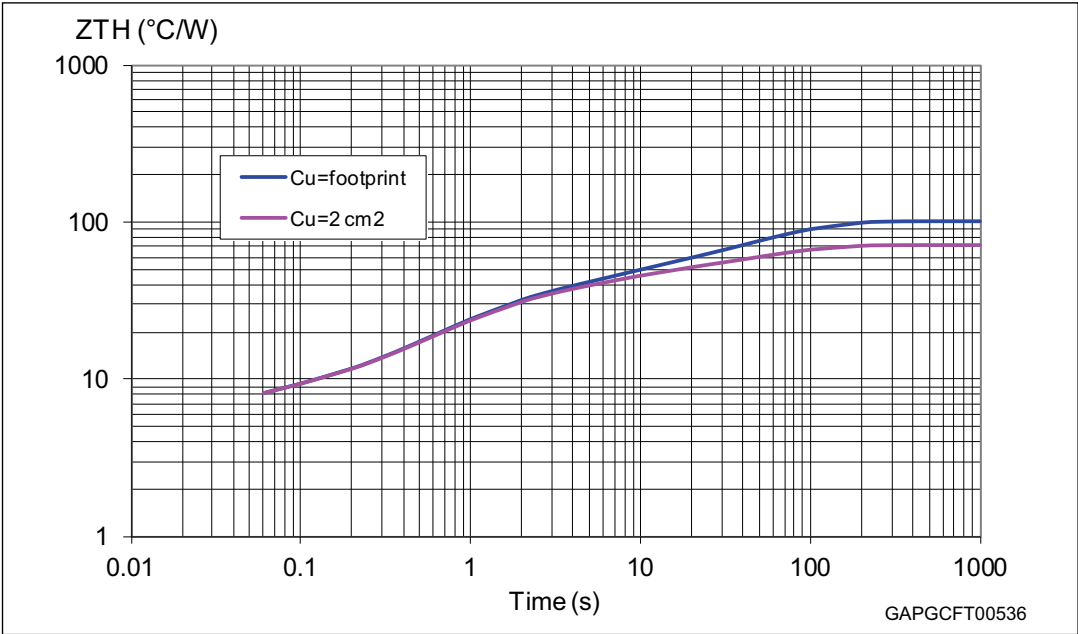


Figure 16. SO-8 thermal impedance junction ambient single pulse

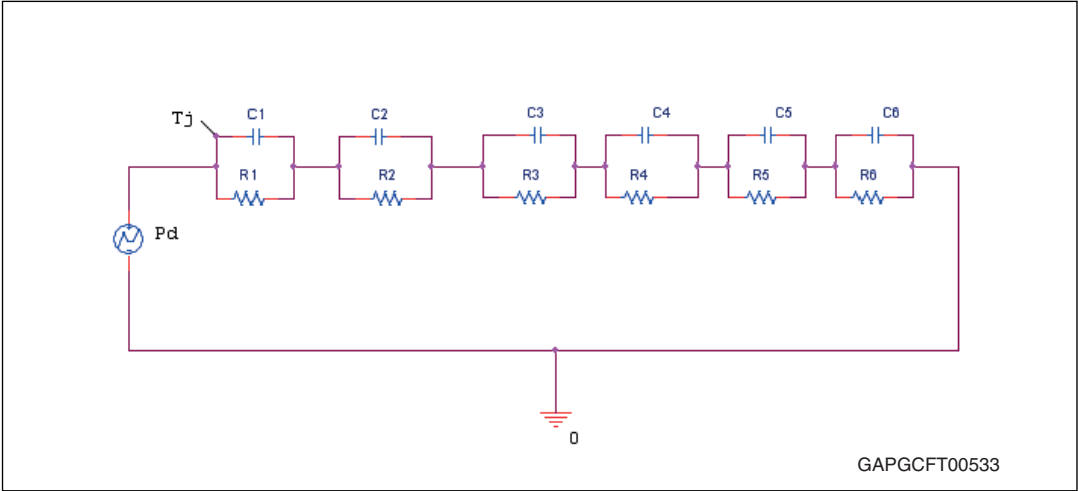


Equation 3: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 17. Thermal fitting model of a LSD in SO-8



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 17. SO-8 thermal parameters

| Area/island (cm <sup>2</sup> ) | Footprint | 2  |
|--------------------------------|-----------|----|
| R1 (°C/W)                      | 0.8       |    |
| R2 (°C/W)                      | 2.7       |    |
| R3 (°C/W)                      | 3.5       |    |
| R4 (°C/W)                      | 21        |    |
| R5 (°C/W)                      | 16        |    |
| R6 (°C/W)                      | 58        | 28 |
| C1 (W.s/°C)                    | 0.00005   |    |
| C2 (W.s/°C)                    | 0.001     |    |
| C3 (W.s/°C)                    | 0.0075    |    |
| C4 (W.s/°C)                    | 0.045     |    |
| C5 (W.s/°C)                    | 0.35      |    |
| C6 (W.s/°C)                    | 1.05      | 2  |

## 5 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 5.1 SOT-223 mechanical data

Figure 18. SOT-223 package dimensions

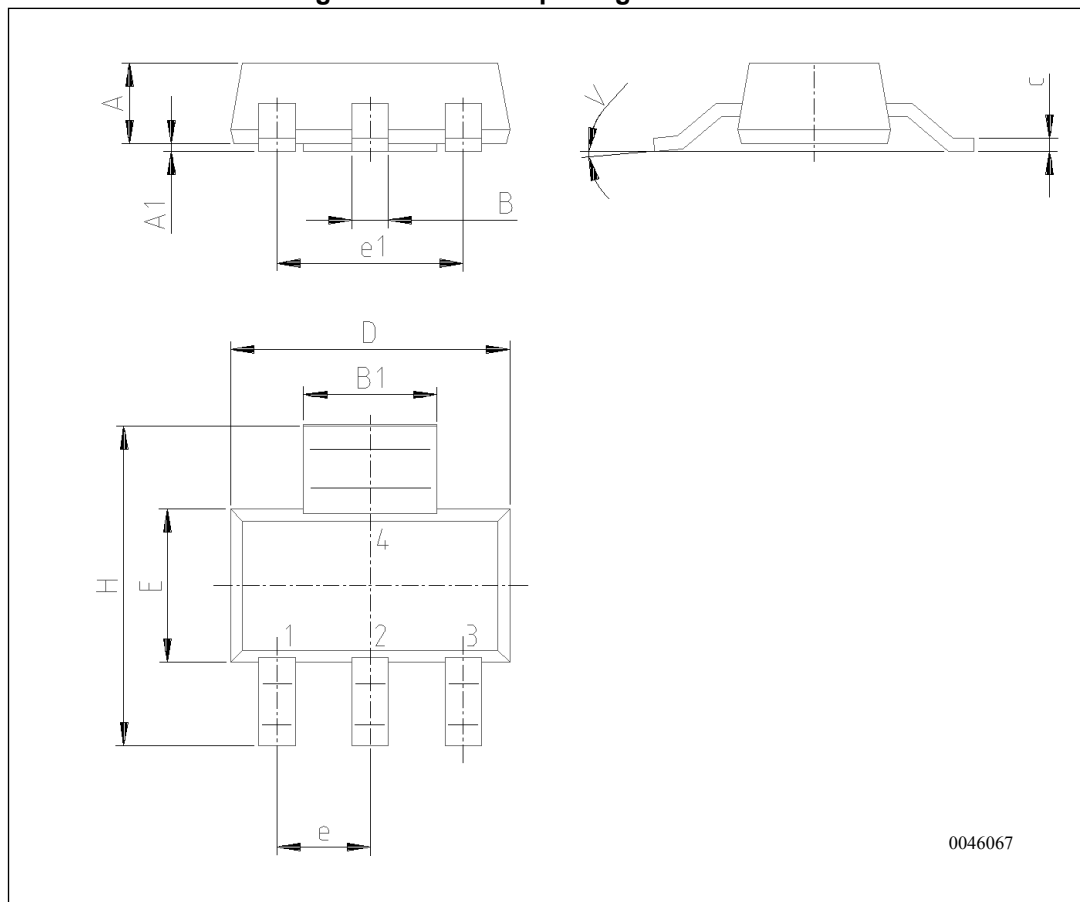


Table 18. SOT-223 mechanical data

| DIM. | mm.      |      |      | inch   |       |       |
|------|----------|------|------|--------|-------|-------|
|      | Min.     | Typ. | Max. | Min.   | Typ.  | Max.  |
| A    |          |      | 1.8  |        |       | 0.071 |
| B    | 0.6      | 0.7  | 0.85 | 0.024  | 0.027 | 0.033 |
| B1   | 2.9      | 3    | 3.15 | 0.114  | 0.118 | 0.124 |
| c    | 0.24     | 0.26 | 0.35 | 0.009  | 0.01  | 0.014 |
| D    | 6.3      | 6.5  | 6.7  | 0.248  | 0.256 | 0.264 |
| e    |          | 2.3  |      |        | 0.09  |       |
| e1   |          | 4.6  |      |        | 0.181 |       |
| E    | 3.3      | 3.5  | 3.7  | 0.13   | 0.138 | 0.146 |
| H    | 6.7      | 7    | 7.3  | 0.264  | 0.276 | 0.287 |
| V    | 10 (max) |      |      |        |       |       |
| A1   | 0.02     |      | 0.1  | 0.0008 |       | 0.004 |

## 5.2 SO-8 mechanical data

Figure 19. SO-8 package dimensions

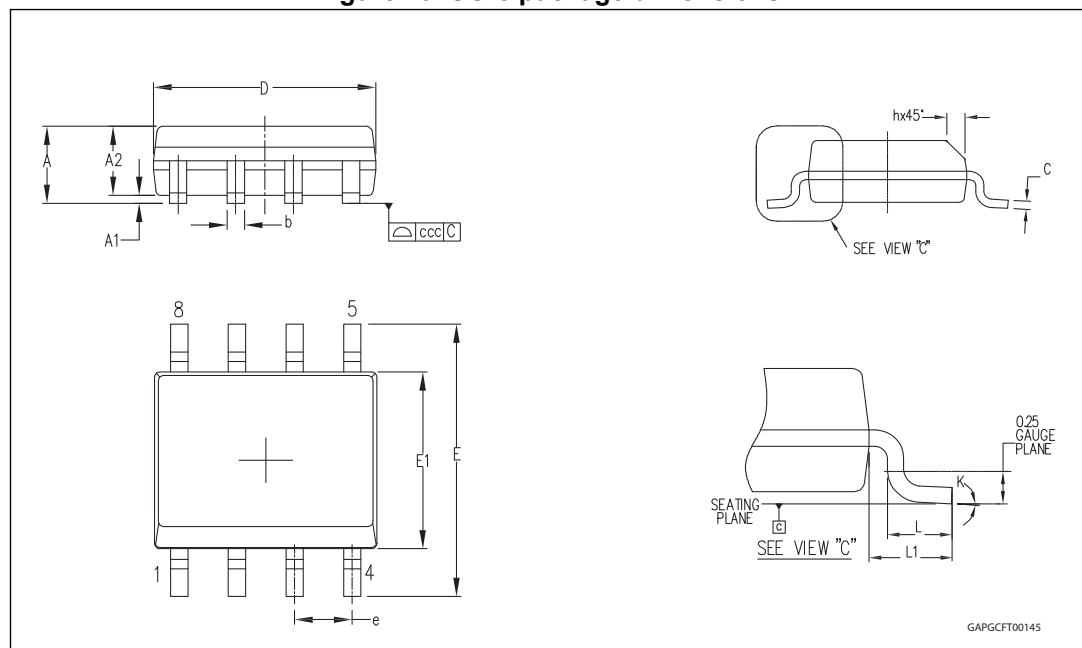


Table 19. SO-8 mechanical data

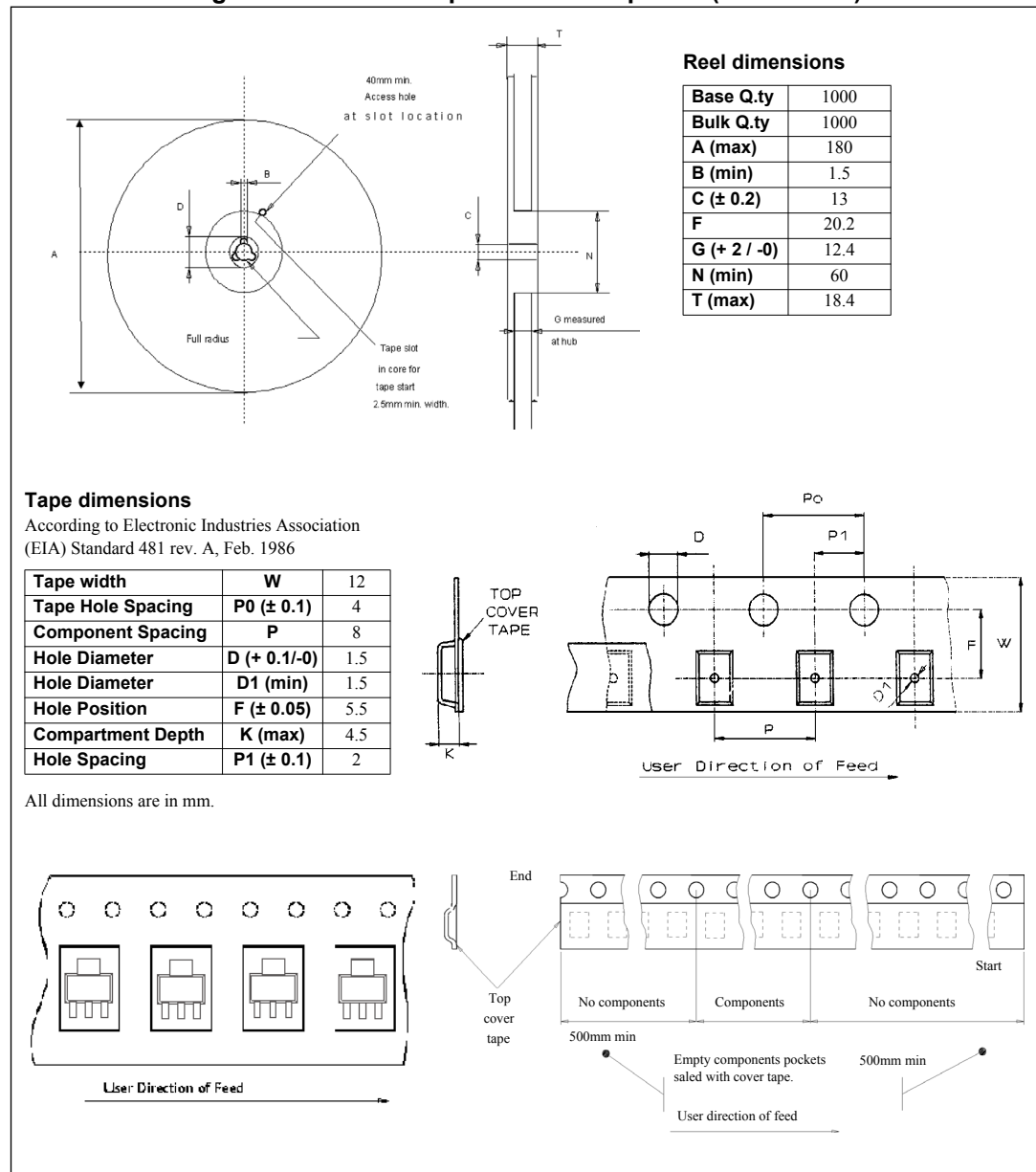
| Symbol            | Millimeters |      |      |
|-------------------|-------------|------|------|
|                   | Min.        | Typ. | Max. |
| A                 |             |      | 1.75 |
| A1                | 0.10        |      | 0.25 |
| A2                | 1.25        |      |      |
| b                 | 0.28        |      | 0.48 |
| c                 | 0.17        |      | 0.23 |
| D <sup>(1)</sup>  | 4.80        | 4.90 | 5.00 |
| E                 | 5.80        | 6.00 | 6.20 |
| E1 <sup>(2)</sup> | 3.80        | 3.90 | 4.00 |
| e                 |             | 1.27 |      |
| h                 | 0.25        |      | 0.50 |
| L                 | 0.40        |      | 1.27 |
| L1                |             | 1.04 |      |
| k                 | 0°          |      | 8°   |
| ccc               |             |      | 0.10 |

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

### 5.3 SOT-223 packing information

The devices can be packed in tube or tape and reel shipments (see the [Table 1: Devices summary on page 1](#)).

**Figure 20. SOT-223 tape and reel shipment (suffix “TR”)**



## 5.4 SO-8 packing information

Figure 21. SO-8 tube shipment (no suffix)

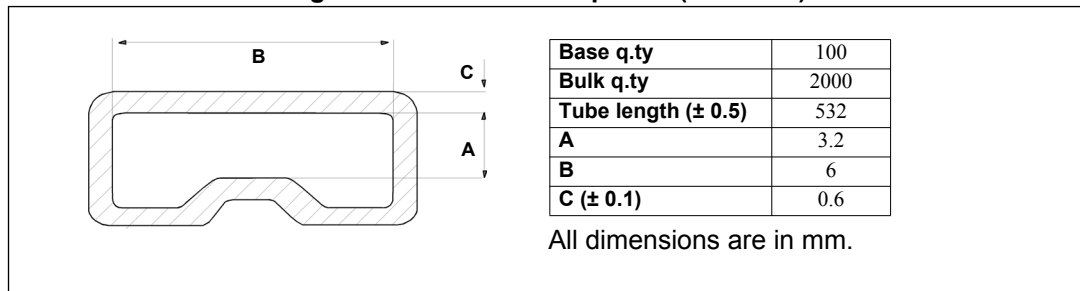
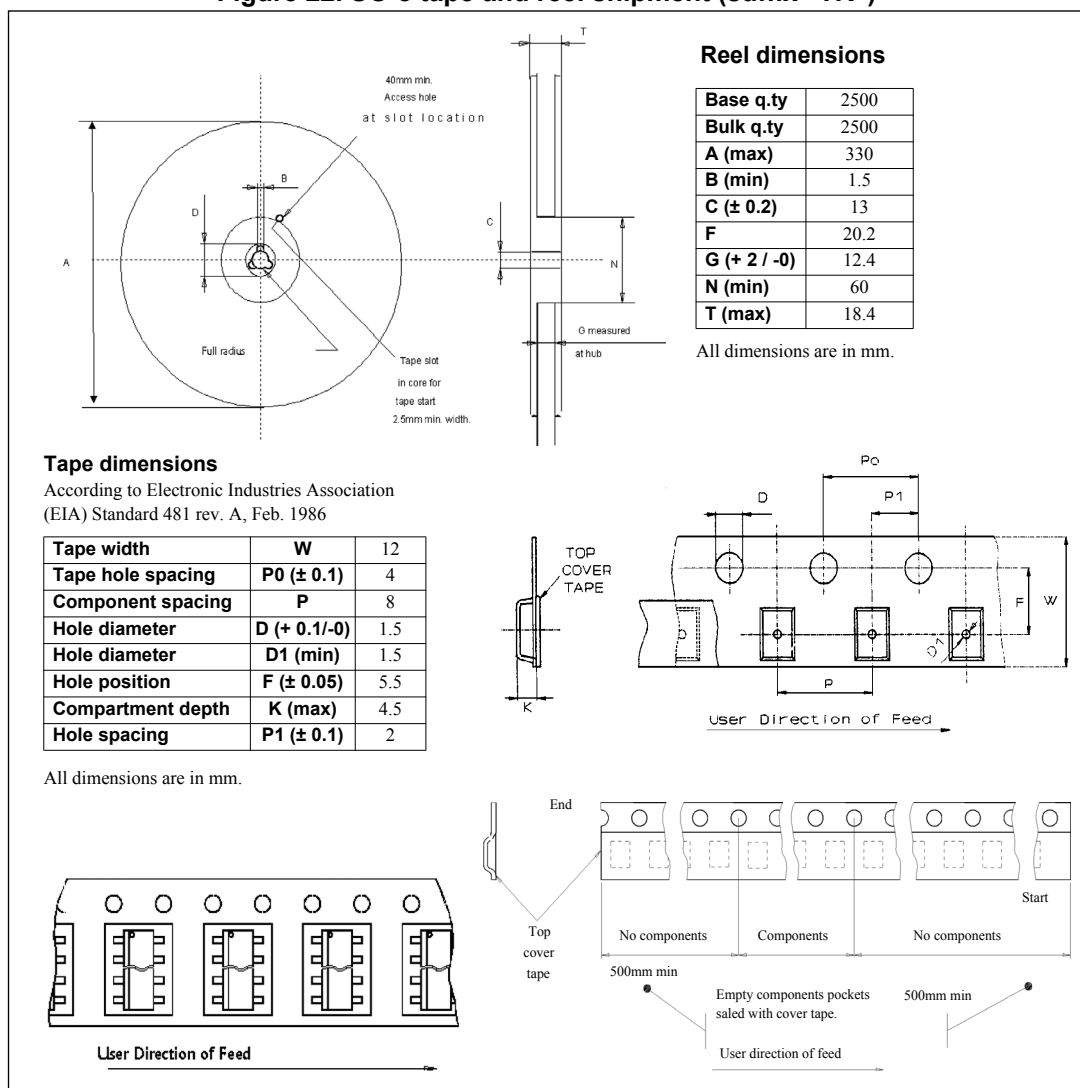


Figure 22. SO-8 tape and reel shipment (suffix "TR")



## 6 Revision history

**Table 20. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                           |
|-------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-Dec-2011 | 1        | Initial release.                                                                                                                                                                                                                                                                                                                                                                  |
| 20-Jan-2012 | 2        | <i>Table 4: Absolute maximum ratings:</i><br>– $I_D$ : updated value                                                                                                                                                                                                                                                                                                              |
| 18-Apr-2012 | 3        | Updated <a href="#">Features</a> list                                                                                                                                                                                                                                                                                                                                             |
| 10-Aug-2012 | 4        | Updated <i>Table 13: Switching characteristics</i>                                                                                                                                                                                                                                                                                                                                |
| 18-Sep-2013 | 5        | Updated disclaimer.                                                                                                                                                                                                                                                                                                                                                               |
| 13-Nov-2013 | 6        | Updated <a href="#">Features</a> list<br><i>Table 8: Input section:</i><br>– $I_{SS}$ : updated maximum value<br><i>Table 12: Supply section (VNL5090S5-E only):</i><br>– $I_S$ : updated maximum value<br>Updated <i>Figure 7: VNL5090N3-E application schematic</i> and<br><i>Figure 8: VNL5090S5-E application schematic</i><br>Updated <i>Section 3.1: MCU I/O protection</i> |
| 01-Apr-2015 | 7        | Updated <i>Table 1: Devices summary</i>                                                                                                                                                                                                                                                                                                                                           |
| 20-Nov-2018 | 8        | Updated title and features in cover page.<br>Removed note from table 8.<br>Updated A (max) value in Reel dimensions table, present in<br><a href="#">Figure 20: SOT-223 tape and reel shipment (suffix “TR”)</a> .<br>Minor text changes.                                                                                                                                         |

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