

Contents

1	Block diagram and pin description	7
2	Electrical specification	9
2.1	Absolute maximum ratings	9
2.2	Thermal data	10
2.3	Main electrical characteristics	11
2.4	Waveforms	23
2.5	Electrical characteristics curves	26
3	Protections	30
3.1	Power limitation	30
3.2	Thermal shutdown	30
3.3	Current limitation	30
3.4	Negative voltage clamp	30
4	Application information	31
4.1	GND protection network against reverse battery	31
4.1.1	Diode (DGND) in the ground line	32
4.2	Immunity against transient electrical disturbances	32
4.3	MCU I/Os protection	33
4.4	Multisense - analog current sense	33
4.4.1	Principle of Multisense signal generation	35
4.4.2	T _{CASE} and V _{CC} monitor	37
4.4.3	Short to VCC and OFF-state open-load detection	38
4.5	Maximum demagnetization energy (V _{CC} = 16 V)	39
5	Package and PCB thermal data	40
5.1	PowerSSO-16 thermal data	40
5.2	SO-8 thermal data	43
6	Package information	46
6.1	ECOPACK®	46
6.2	PowerSSO-16 package information	46

6.3	SO-8 package information	48
6.4	Packing information	49
7	Order codes	50
8	Revision history	51

List of tables

Table 1.	Pin functions	7
Table 2.	Suggested connections for unused and not connected pins	8
Table 3.	Absolute maximum ratings	9
Table 4.	Thermal data.	10
Table 5.	Power section	11
Table 6.	Switching ($V_{CC} = 13\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$, unless otherwise specified).	12
Table 7.	Logic Inputs ($7\text{ V} < V_{CC} < 28\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$).	12
Table 8.	Protections ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$).	13
Table 9.	MultiSense ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$).	14
Table 10.	Truth table.	22
Table 11.	MultiSense multiplexer addressing	22
Table 12.	ISO 7637-2 - electrical transient conduction along supply line	32
Table 13.	Multisense pin levels in off-state	37
Table 14.	PCB properties	40
Table 15.	Thermal parameters	42
Table 16.	PCB properties	43
Table 17.	Thermal parameters	45
Table 18.	PowerSSO-16 mechanical data	47
Table 19.	SO-8 mechanical data	48
Table 20.	Device summary	50
Table 21.	Document revision history	51

List of figures

Figure 1.	Block diagram	7
Figure 2.	Configuration diagram (top view)	8
Figure 3.	Current and voltage conventions	9
Figure 4.	I_{OUT}/I_{SENSE} versus I_{OUT}	19
Figure 5.	Current sense accuracy versus I_{OUT}	19
Figure 6.	Switching times and Pulse skew	20
Figure 7.	MultiSense timings (current sense mode)	20
Figure 8.	Multisense timings (chip temperature and VCC sense mode)(VN7050AJ-E only)	21
Figure 9.	T_{DSTKON}	21
Figure 10.	Latch functionality - behavior in hard short circuit condition ($T_{AMB} << T_{TSD}$)	23
Figure 11.	Latch functionality - behavior in hard short circuit condition	23
Figure 12.	Latch functionality - behavior in hard short circuit condition (autorestart mode + latch off)	24
Figure 13.	Standby mode activation	24
Figure 14.	Standby state diagram	25
Figure 15.	OFF-state output current	26
Figure 16.	Standby current	26
Figure 17.	$I_{GND(ON)}$ vs. I_{out}	26
Figure 18.	Logic Input high level voltage	26
Figure 19.	Logic Input low level voltage	26
Figure 20.	High level logic input current	26
Figure 21.	Low level logic input current	27
Figure 22.	Logic Input hysteresis voltage	27
Figure 23.	FaultRST Input clamp voltage	27
Figure 24.	Undervoltage shutdown	27
Figure 25.	On-state resistance vs. T_{case}	27
Figure 26.	On-state resistance vs. V_{CC}	27
Figure 27.	Turn-on voltage slope	28
Figure 28.	Turn-off voltage slope	28
Figure 29.	W_{on} vs. T_{case}	28
Figure 30.	W_{off} vs. T_{case}	28
Figure 31.	I_{LIMH} vs. T_{case}	28
Figure 32.	OFF-state open-load voltage detection threshold	28
Figure 33.	V_{sense} clamp vs. T_{case}	29
Figure 34.	V_{senseh} vs. T_{case}	29
Figure 35.	Application diagram	31
Figure 36.	Simplified internal structure	31
Figure 37.	Multisense and diagnostic – block diagram	34
Figure 38.	Multisense block diagram	35
Figure 39.	Analogue HSD – open-load detection in off-state	36
Figure 40.	Open-load / short to VCC condition	37
Figure 41.	GND voltage shift	38
Figure 42.	Maximum turn off current versus inductance	39
Figure 43.	PowerSSO-16 on two-layers PCB (2s0p to JEDEC JESD 51-5)	40
Figure 44.	PowerSSO-16 on four-layers PCB (2s2p to JEDEC JESD 51-7)	40
Figure 45.	PowerSSO-16 $R_{thj-amb}$ vs PCB copper area in open box free air conditions	41
Figure 46.	PowerSSO-16 thermal impedance junction ambient single pulse	41
Figure 47.	Thermal fitting model for PowerSSO-16	42
Figure 48.	S0-8 on two-layers PCB (2s0p to JEDEC JESD 51-5)	43

Figure 49.	SO-8 on four-layers PCB (2s2p to JEDEC JESD 51-7)	43
Figure 50.	SO-8 $R_{thj-amb}$ vs PCB copper area in open box free air conditions	44
Figure 51.	SO-8 thermal impedance junction ambient single pulse.	44
Figure 52.	Thermal fitting model for SO-8	45
Figure 53.	PowerSSO-16 package dimensions.	46
Figure 54.	SO-8 package dimensions	48
Figure 55.	SO-8 tube shipment (no suffix)	49
Figure 56.	SO-8 tape and reel shipment (suffix "TR")	49

1 Block diagram and pin description

Figure 1. Block diagram

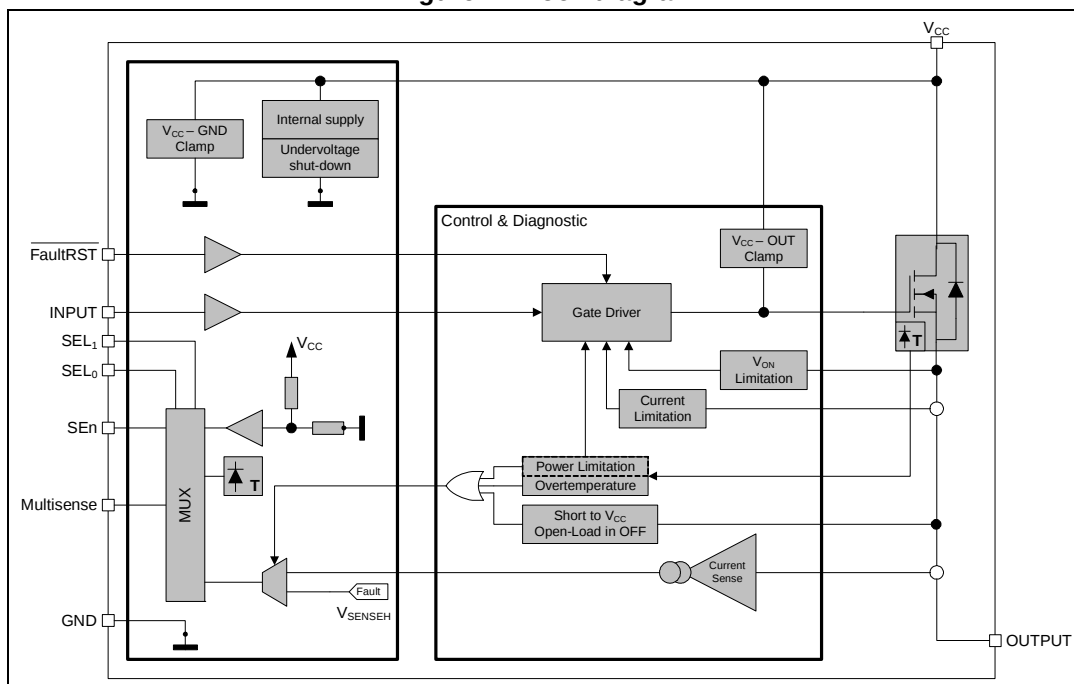


Table 1. Pin functions

Name	Function
V _{CC}	Battery connection.
OUTPUT	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode / resistor network.
INPUT	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
MultiSense	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3 V and 5 V CMOS output pin; it enables the MultiSense diagnostic pin.
SEL _{0,1}	Active high compatible with 3 V and 5 V CMOS output pin; they address the MultiSense multiplexer.
FaultRST	Active low compatible with 3 V and 5 V CMOS output pin; unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode.

Figure 2. Configuration diagram (top view)

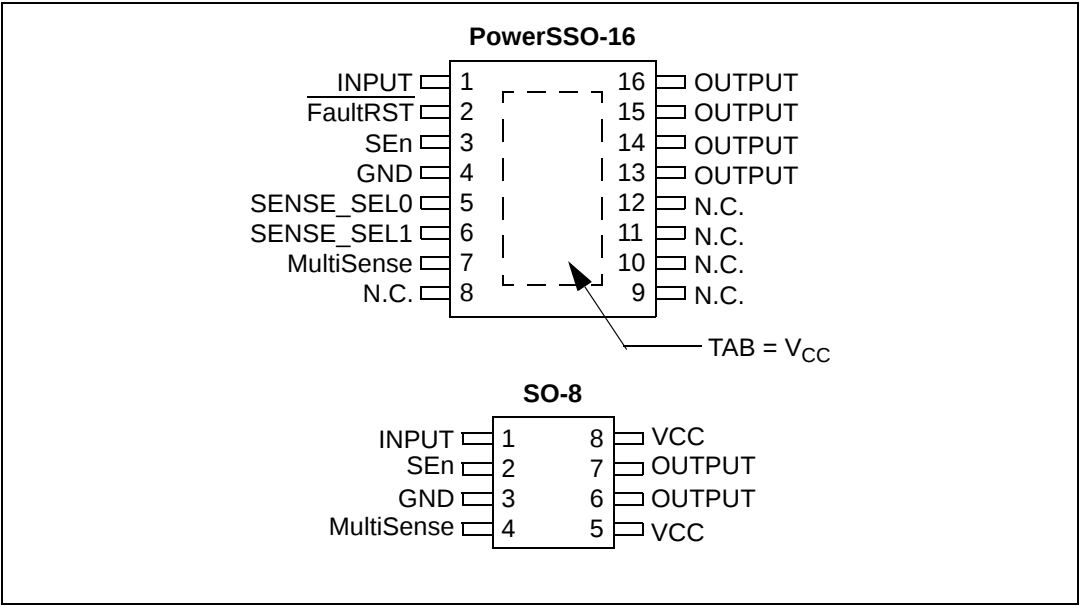


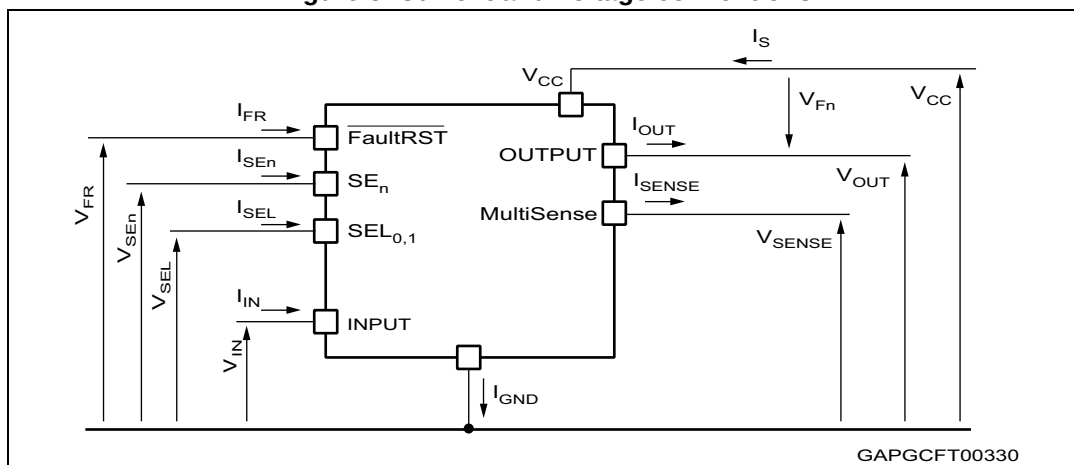
Table 2. Suggested connections for unused and not connected pins

Connection / pin	MultiSense	N.C.	Output	Input	SEn, SELx, FaultRST
Floating	Not allowed	X ⁽¹⁾	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions



Note: $V_F = V_{OUT} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
V_{CCPK}	Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40 V; $R_L = 4 \Omega$)	40	
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	10	
I_{IN}	INPUT DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		
I_{SEL}	SEL _{0,1} DC input current		
I_{FR}	FaultRST DC input current	-1 to 10	mA
V_{FR}	FaultRST DC input voltage	7.5	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
I_{SENSE}	MultiSense pin DC output current ($V_{\text{GND}} = V_{\text{CC}}$ and $V_{\text{SENSE}} < 0 \text{ V}$)	10	mA
	MultiSense pin DC output current in reverse ($V_{\text{CC}} < 0 \text{ V}$)	-20	
E_{MAX}	Maximum switching energy (single pulse) ($T_{\text{DEMAG}} = 0.4 \text{ ms}$; $T_{\text{jstart}} = 150 \text{ }^{\circ}\text{C}$)	30	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F)		
	– INPUT	4000	V
	– MultiSense	2000	V
	– SEn, SEL _{0,1} , FaultRST	4000	V
	– OUTPUT	4000	V
	– V_{CC}	4000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_{j}	Junction operating temperature	-40 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value		Unit
		SO-8	PSSO-16	
$R_{\text{thj-board}}$	Thermal resistance junction-board (JEDEC JESD 51-5/51-8) ⁽¹⁾	29.4	6.8	$^{\circ}\text{C/W}$
$R_{\text{thj-amb}}$	Thermal resistance junction-ambient (JEDEC JESD 51-5) ⁽²⁾	67.5	58.5	
$R_{\text{thj-amb}}$	Thermal resistance junction-ambient (JEDEC JESD 51-7) ⁽¹⁾	45.8	24.5	

1. Device mounted on four-layers 2s2p PCB.
2. Device mounted on two-layers 2s0p PCB with 2 cm² heatsink copper trace.

2.3 Main electrical characteristics

$7\text{ V} < V_{CC} < 28\text{ V}$; $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise specified.

All typical values refer to $V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	
$V_{USDReset}$	Undervoltage shutdown reset				5	
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		
R_{ON}	On-state resistance	$I_{OUT} = 2\text{ A}$; $T_j = 25\text{ °C}$		50		mΩ
		$I_{OUT} = 2\text{ A}$; $T_j = 150\text{ °C}$			100	
		$I_{OUT} = 2\text{ A}$; $V_{CC} = 4\text{ V}$; $T_j = 25\text{ °C}$			75	
V_{clamp}	Clamp voltage	$I_S = 20\text{ mA}$; $T_j = -40\text{ °C}$	38			V
		$I_S = 20\text{ mA}$; $25\text{ °C} < T_j < 150\text{ °C}$	41	46	52	
I_{STBY}	Supply current in standby at $V_{CC} = 13\text{ V}^{(1)}$	$V_{CC} = 13\text{ V}$; $V_{IN} = V_{OUT} = V_{SEn} = 0\text{ V}$; $V_{FR} = V_{SEL0,1} = 0\text{ V}$; $T_j = 25\text{ °C}$			0.5	μA
		$V_{CC} = 13\text{ V}$; $V_{IN} = V_{OUT} = V_{SEn} = 0\text{ V}$; $V_{FR} = V_{SEL0,1} = 0\text{ V}$; $T_j = 85\text{ °C}^{(2)}$			0.5	
		$V_{CC} = 13\text{ V}$; $V_{IN} = V_{OUT} = V_{SEn} = 0\text{ V}$; $V_{FR} = V_{SEL0,1} = 0\text{ V}$; $T_j = 125\text{ °C}$			3	
t_{D_STBY}	Standby mode blanking time	$V_{CC} = 13\text{ V}$; $V_{IN} = V_{OUT} = V_{FR} = V_{SEL0,1} = 0\text{ V}$; $V_{SEn} = 5\text{ V}$ to 0 V	60	300	550	μs
$I_{S(ON)}$	Supply current	$V_{CC} = 13\text{ V}$; $V_{SEn} = 0\text{ V}$; $V_{SEL0,1} = V_{FR} = 0\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ A}$		3	5	mA
$I_{GND(ON)}$	Control stage current consumption in ON-state. All channels active.	$V_{CC} = 13\text{ V}$; $V_{SEn} = 5\text{ V}$; $V_{SEL0,1} = V_{FR} = 0\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 2\text{ A}$			6	mA
$I_{L(off)}$	Off-state output current at $V_{CC} = 13\text{ V}$	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$	0	0.01	0.5	μA
		$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 125\text{ °C}$	0		3	
V_F	Output - V_{CC} diode voltage	$I_{OUT} = -2\text{ A}$; $T_j = 150\text{ °C}$			0.7	V

1. PowerMOS leakage included.

2. Parameter specified by design; not subject to production test.

Table 6. Switching ($V_{CC} = 13\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}^{(1)}$	Turn-on delay time at $T_j = 25^{\circ}\text{C}$	$R_L = 6.5\ \Omega$	10	60	120	μs
$t_{d(off)}^{(1)}$	Turn-off delay time at $T_j = 25^{\circ}\text{C}$	$R_L = 6.5\ \Omega$	10	40	100	
$(dV_{OUT}/dt)_{on}^{(1)}$	Turn-on voltage slope at $T_j = 25^{\circ}\text{C}$	$R_L = 6.5\ \Omega$	0.1	0.3	0.7	$\text{V}/\mu\text{s}$
$(dV_{OUT}/dt)_{off}^{(1)}$	Turn-off voltage slope at $T_j = 25^{\circ}\text{C}$	$R_L = 6.5\ \Omega$	0.1	0.32	0.7	
W_{ON}	Switching energy losses at turn-on (t_{won})	$R_L = 6.5\ \Omega$	—	0.25	0.33 ⁽²⁾	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	$R_L = 6.5\ \Omega$	—	0.23	0.31 ⁽²⁾	mJ
$t_{SKEW}^{(1)}$	Differential Pulse skew ($t_{PHL} - t_{PLH}$)	$R_L = 6.5\ \Omega$	-80	-30	20	μs

1. See [Figure 6: Switching times and Pulse skew](#).
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 7. Logic Inputs ($7\text{ V} < V_{CC} < 28\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
INPUT characteristics						
V _{IL}	Input low level voltage				0.9	V
I _{IL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{IH}	Input high level voltage		2.1			V
I _{IH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{I(hyst)}	Input hysteresis voltage		0.2			V
V _{ICL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		
FaultRST characteristics (VN7050AJ-E only)						
V _{FRL}	Input low level voltage				0.9	V
I _{FRL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{FRH}	Input high level voltage		2.1			V
I _{FRH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{FR(hyst)}	Input hysteresis voltage		0.2			V
V _{FRCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.5	V
		I _{IN} = -1 mA		-0.3		
SEL _{0,1} characteristics (VN7050AJ-E only) (7 V < V _{CC} < 18 V)						
V _{SELL}	Input low level voltage				0.9	V
I _{SELL}	Low level input current	V _{IN} = 0.9 V	1			μA

Table 7. Logic Inputs (7 V < V_{CC} < 28 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SELH}	Input high level voltage		2.1			V
I _{SELH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{SEL(hyst)}	Input hysteresis voltage		0.2			V
V _{SELCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V _{CC} < 18 V)						
V _{SEnL}	Input low level voltage				0.9	V
I _{SEnL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{SEnH}	Input high level voltage		2.1			V
I _{SEnH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{SEn(hyst)}	Input hysteresis voltage		0.2			V
V _{SEnCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		

Table 8. Protections (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{LIMH}	DC short circuit current	V _{CC} = 13 V	21	30	42	A
		4 V < V _{CC} < 18 V ⁽¹⁾			42	A
I _{LIML}	Short circuit current during thermal cycling	V _{CC} = 13 V; T _R < T _j < T _{TSD}		10		A
T _{TSD}	Shutdown temperature		150	175	200	°C
T _R	Reset temperature ⁽¹⁾		T _{RS} + 1	T _{RS} + 7		
T _{RS}	Thermal reset of fault diagnostic indication	V _{FR} = 0 V; V _{SEn} = 5 V;	135			
T _{HYST}	Thermal hysteresis (T _{TSD} - T _R) ⁽¹⁾			7		
ΔT _{J_SD}	Dynamic temperature	T _j = -40 °C; V _{CC} = 13 V		60		K
t _{LATCH_RST}	Fault reset time for output unlatch ⁽¹⁾ (VN7050AJ-E only)	V _{FR} = 5 V to 0 V; V _{SEn} = 5 V; V _{IN} = 5 V; V _{SEL0,1} = 0 V	3	10	20	μs
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} = 2 A; L = 6 mH; T _j = -40 °C	V _{CC} - 38			V
		I _{OUT} = 2 A; L = 6 mH; T _j = 25 °C to 150 °C	V _{CC} - 41	V _{CC} - 46	V _{CC} - 52	V
V _{ON}	Output voltage drop limitation	I _{OUT} = 0.2 A		20		mV

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SENSE_CL}	MultiSense clamp voltage	V _{SEn} = 0 V; I _{SENSE} = 1 mA	-17		-12	V
		V _{SEn} = 0 V; I _{SENSE} = -1 mA		7		V
Current Sense characteristics						
K _{OL}	I _{OUT} /I _{SENSE}	I _{OUT} = 0.01 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	440			
dK _{cal} /K _{cal} ⁽¹⁾⁽²⁾	Current sense ratio drift at calibration point	I _{OUT} = 0.01 A to 0.03 A; I _{cal} = 17.5 mA; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	-30		30	%
K _{LED}	I _{OUT} /I _{SENSE}	I _{OUT} = 0.05 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	530	1445	2200	
dK _{LED} /K _{LED} ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 0.05 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	-25		25	%
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} = 0.2 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	830	1330	1935	
dK ₀ /K ₀ ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 0.2 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	-20		20	%
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 0.4 A; V _{SENSE} = 4 V; V _{SEn} = 5 V	915	1290	1700	
dK ₁ /K ₁ ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 0.4 A; V _{SENSE} = 4 V; V _{SEn} = 5 V	-15		15	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 1.5 A; V _{SENSE} = 4 V; V _{SEn} = 5 V	980	1200	1470	
dK ₂ /K ₂ ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 1.5 A; V _{SENSE} = 4 V; V _{SEn} = 5 V	-10		10	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 4.5 A; V _{SENSE} = 4 V; V _{SEn} = 5 V	1050	1190	1290	
dK ₃ /K ₃ ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 4.5 A; V _{SENSE} = 4 V; V _{SEn} = 5 V	-5		5	%

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{SENSE0}	MultiSense leakage current	MultiSense disabled: V _{SEN} = 0 V	0		0.5	μA
		MultiSense disabled: -1 V < V _{SENSE} < 5 V ⁽¹⁾	-0.5		0.5	
		MultiSense enabled: V _{SEN} = 5 V; Channel ON; I _{OUT} = 0 A; Diagnostic selected; V _{IN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; I _{OUT} = 0 A;	0		2	
		MultiSense enabled: V _{SEN} = 5 V Channel OFF; Diagnostic selected: V _{IN} = 0 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V	0		2	
V _{OUT_MSD} ⁽¹⁾	Output Voltage for MultiSense shutdown	V _{SEN} = 5 V; R _{SENSE} = 2.7 kΩ – E.g. Ch ₀ : V _{IN0} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; I _{OUT} = 2 A		5		V
V _{SENSE_SAT}	MultiSense saturation voltage	V _{CC} = 7 V; R _{SENSE} = 2.7 kΩ; V _{SEN} = 5 V; V _{IN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; I _{OUT} = 2 A; T _j = 150°C	5			V
I _{SENSE_SAT} ⁽¹⁾	CS saturation current	V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN} = 5 V; V _{SEN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; T _j = 150°C	4			mA
I _{OUT_SAT} ⁽¹⁾	Output saturation current	V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN} = 5 V; V _{SEN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; T _j = 150°C	6			A
OFF-state diagnostic						
V _{OL}	OFF-state open-load voltage detection threshold	V _{IN} = 0 V; V _{SEN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V;	2	3	4	V
I _{L(off2)}	OFF-state output sink current	V _{IN} = 0 V; V _{OUT} = V _{OL}	-100		-15	μA
t _{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see Figure 9)	V _{IN} = 5 V to 0 V; V _{SEN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; I _{OUT} = 0 A; V _{OUT} = 4 V	100	350	700	μs

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{D_OL_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SE_n	$V_{IN} = 0\text{ V}$; $V_{FR} = 0\text{ V}$; $V_{SEL0} = 0\text{ V}$; $V_{SEL1} = 0\text{ V}$; $V_{OUT} = 4\text{ V}$; $V_{SEn} = 0\text{ V to }5\text{ V}$			60	μs
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	$V_{IN} = 0\text{ V}$; $V_{SEn} = 5\text{ V}$; $V_{SEL0} = 0\text{ V}$; $V_{SEL1} = 0\text{ V}$; $V_{OUT} = 0\text{ V to }4\text{ V}$		5	30	μs
Chip temperature analog feedback (VN7050AJ-E only)						
V_{SENSE_TC}	MultiSense output voltage proportional to chip temperature	$V_{SEn} = 5\text{ V}$; $V_{SEL0} = 0\text{ V}$; $V_{SEL1} = 5\text{ V}$; $V_{IN} = 0\text{ V}$; $R_{SENSE} = 1\text{ k}\Omega$; $T_j = -40\text{ }^\circ\text{C}$	2.325	2.41	2.495	V
		$V_{SEn} = 5\text{ V}$; $V_{SEL0} = 0\text{ V}$; $V_{SEL1} = 5\text{ V}$; $V_{IN} = 0\text{ V}$; $R_{SENSE} = 1\text{ k}\Omega$; $T_j = 25\text{ }^\circ\text{C}$	1.985	2.07	2.155	V
		$V_{SEn} = 5\text{ V}$; $V_{SEL0} = 0\text{ V}$; $V_{SEL1} = 5\text{ V}$; $V_{IN} = 0\text{ V}$; $R_{SENSE} = 1\text{ k}\Omega$; $T_j = 125\text{ }^\circ\text{C}$	1.435	1.52	1.605	V
$dV_{SENSE_TC}/dT^{(1)}$	Temperature coefficient	$T_j = -40\text{ }^\circ\text{C to }150\text{ }^\circ\text{C}$		-5.5		mV/K
Transfer function		$V_{SENSE_TC}(T) = V_{SENSE_TC}(T_0) + dV_{SENSE_TC} / dT * (T - T_0)$				
V _{CC} supply voltage analog feedback (VN7050AJ-E only)						
V_{SENSE_VCC}	MultiSense output voltage proportional to V _{CC} supply voltage	$V_{CC} = 13\text{ V}$; $V_{SEn} = 5\text{ V}$; $V_{SEL0} = 5\text{ V}$; $V_{SEL1} = 5\text{ V}$; $V_{IN} = 0\text{ V}$; $R_{SENSE} = 1\text{ k}\Omega$	3.16	3.23	3.3	V
Transfer function ⁽³⁾		$V_{SENSE_VCC} = V_{CC} / 4$				
Fault diagnostic feedback (see Table 10)						
V_{SENSEH}	MultiSense output voltage in fault condition	$V_{CC} = 13\text{ V}$; $R_{SENSE} = 1\text{ k}\Omega$; $V_{SEn} = 5\text{ V}$; $V_{IN} = 0\text{ V}$; $V_{SEL0} = 0\text{ V}$; $V_{SEL1} = 0\text{ V}$; $I_{OUT} = 0\text{ A}$; $V_{OUT} = 4\text{ V}$	5		6.6	V
I_{SENSEH}	MultiSense output current in fault condition	$V_{CC} = 13\text{ V}$; $V_{SENSE} = 5\text{ V}$	7	20	30	mA

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
MultiSense timings (current sense mode - see Figure 7)						
t _{DSSENSE1H}	Current sense settling time from rising edge of SEn	V _{IN} = 5 V; V _{SEn} = 0 V to 5 V; R _{SENSE} = 1 kΩ; R _L = 6.5 Ω			60	μs
t _{DSSENSE1L}	Current sense disable delay time from falling edge of SEn	V _{IN} = 5 V; V _{SEn} = 5 V to 0 V; R _{SENSE} = 1 kΩ; R _L = 6.5 Ω		5	20	
t _{DSSENSE2H}	Current sense settling time from rising edge of INPUT	V _{IN} = 0 V to 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 6.5 Ω		100	250	
Δt _{DSSENSE2H}	Current sense settling time from rising edge of I _{OUT} (dynamic response to a step change of I _{OUT})	V _{IN} = 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; I _{SENSE} = 90 % of I _{SENSEMAX} ; R _L = 6.5 Ω			100	
t _{DSSENSE2L}	Current sense turn-off delay time from falling edge of INPUT	V _{IN} = 5 V to 0 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 6.5 Ω		50	250	
MultiSense timings (chip temperature sense mode - see Figure 8) (VN7050AJ-E only)						
t _{DSSENSE3H}	V _{SENSE_TC} settling time from rising edge of SEn	V _{SEn} = 0 V to 5 V; V _{SEL0} = 0 V; V _{SEL1} = 5 V; R _{SENSE} = 1 kΩ			60	μs
t _{DSSENSE3L}	V _{SENSE_TC} disable delay time from falling edge of SEn	V _{SEn} = 5 V to 0 V; V _{SEL0} = 0 V; V _{SEL1} = 5 V; R _{SENSE} = 1 kΩ			20	μs
MultiSense timings (V _{CC} voltage sense mode - see Figure 8) (VN7050AJ-E only)						
t _{DSSENSE4H}	V _{SENSE_VCC} settling time from rising edge of SEn	V _{SEn} = 0 V to 5 V; V _{SEL0} = 5 V; V _{SEL1} = 5 V; R _{SENSE} = 1 kΩ			60	μs
t _{DSSENSE4L}	V _{SENSE_VCC} disable delay time from falling edge of SEn	V _{SEn} = 5 V to 0 V; V _{SEL0} = 5 V; V _{SEL1} = 5 V; R _{SENSE} = 1 kΩ			20	μs
MultiSense timings (Multiplexer transition times) ⁽⁴⁾ (VN7050AJ-E only)						
t _{D_CStoTC}	MultiSense transition delay from current sense to T _C sense	V _{IN} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V to 5 V; I _{OUT} = 1 A; R _{SENSE} = 1 kΩ			60	μs

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{D_TCToCS}	MultiSense transition delay from T _C sense to current sense	V _{IN} = 5 V; V _{SEN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 5 V to 0 V; I _{OUT} = 1 A; R _{SENSE} = 1 kΩ			20	μs
t _{D_CStoVCC}	MultiSense transition delay from current sense to V _{CC} sense	V _{IN} = 5 V; V _{SEN} = 5 V; V _{SEL0} = 5 V; V _{SEL1} = 0 V to 5 V; I _{OUT} = 1 A; R _{SENSE} = 1 kΩ			60	μs
t _{D_VCCtoCS}	MultiSense transition delay from V _{CC} sense to current sense	V _{IN} = 5 V; V _{SEN} = 5 V; V _{SEL0} = 5 V; V _{SEL1} = 5 V to 0 V; I _{OUT} = 1 A; R _{SENSE} = 1 kΩ			20	μs
t _{D_TCToVCC}	MultiSense transition delay from T _C sense to V _{CC} sense	V _{CC} = 13 V; T _j = 125 °C; V _{SEN} = 5 V; V _{SEL1} = 5 V; V _{SEL0} = 0 V to 5 V; R _{SENSE} = 1 kΩ			20	μs
t _{D_VCCtoTC}	MultiSense transition delay from V _{CC} sense to T _C sense	V _{CC} = 13 V; T _j = 125 °C; V _{SEN} = 5 V; V _{SEL1} = 5 V; V _{SEL0} = 5 V to 0 V; R _{SENSE} = 1 kΩ			20	μs

1. Parameter guaranteed by design and characterization; not subject to production test.
2. All values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.
3. V_{CC} sensing and T_C are referred to GND potential.
4. Transition delay are measured up to +/- 10% of final conditions.

Figure 4. I_{OUT}/I_{SENSE} versus I_{OUT}

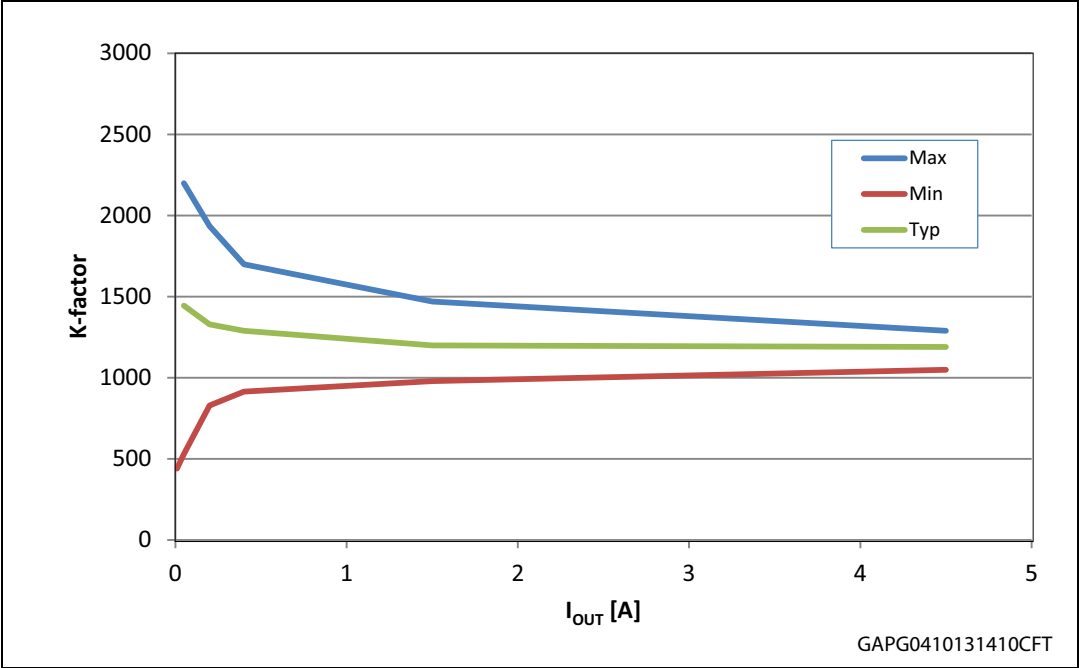


Figure 5. Current sense accuracy versus I_{OUT}

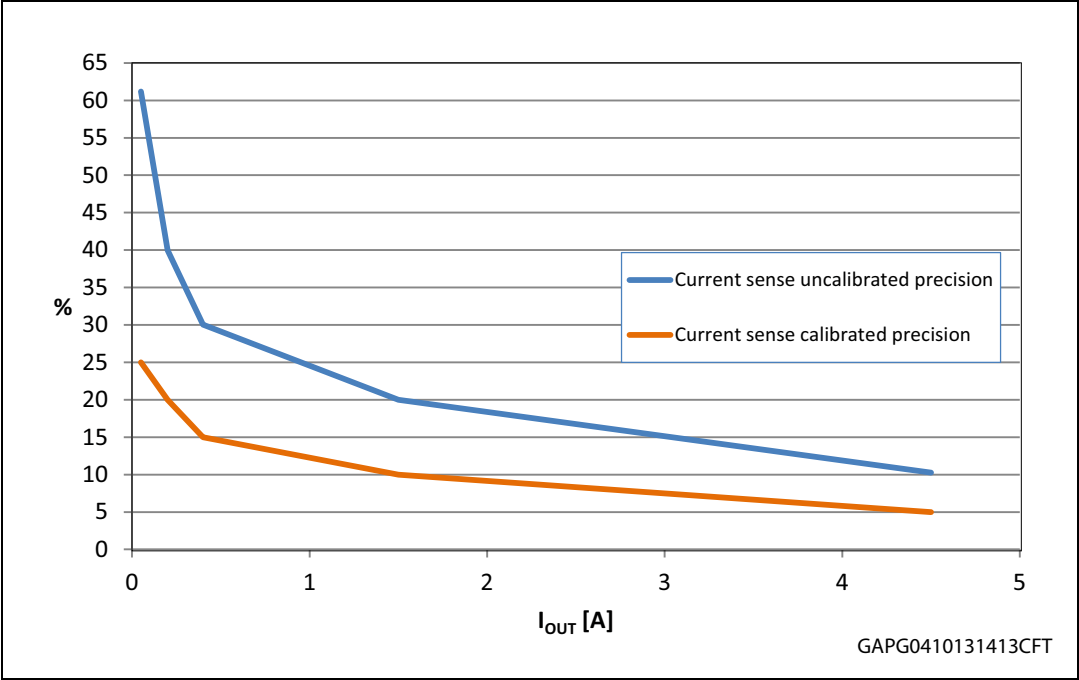


Figure 6. Switching times and Pulse skew

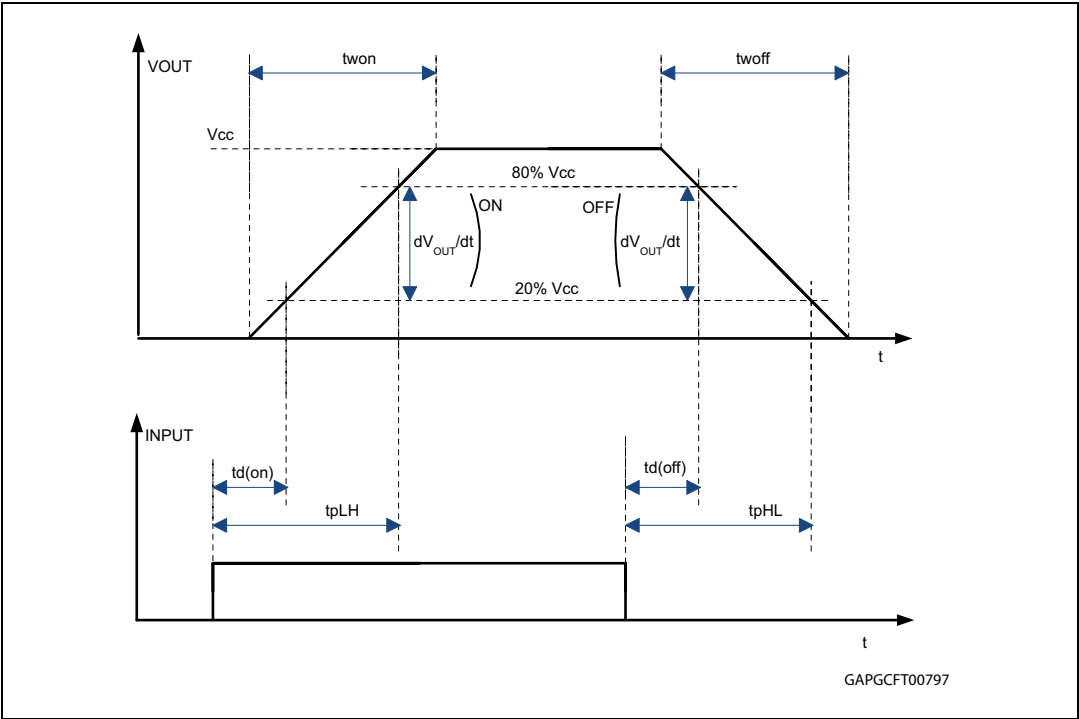


Figure 7. MultiSense timings (current sense mode)

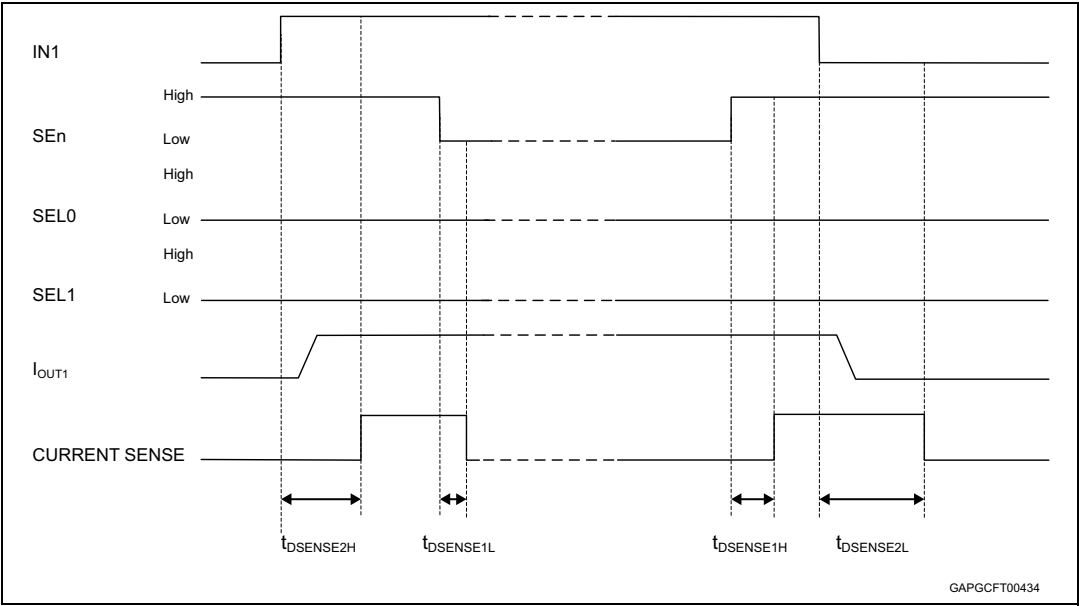


Figure 8. Multisense timings (chip temperature and V_{CC} sense mode)(VN7050AJ-E only)

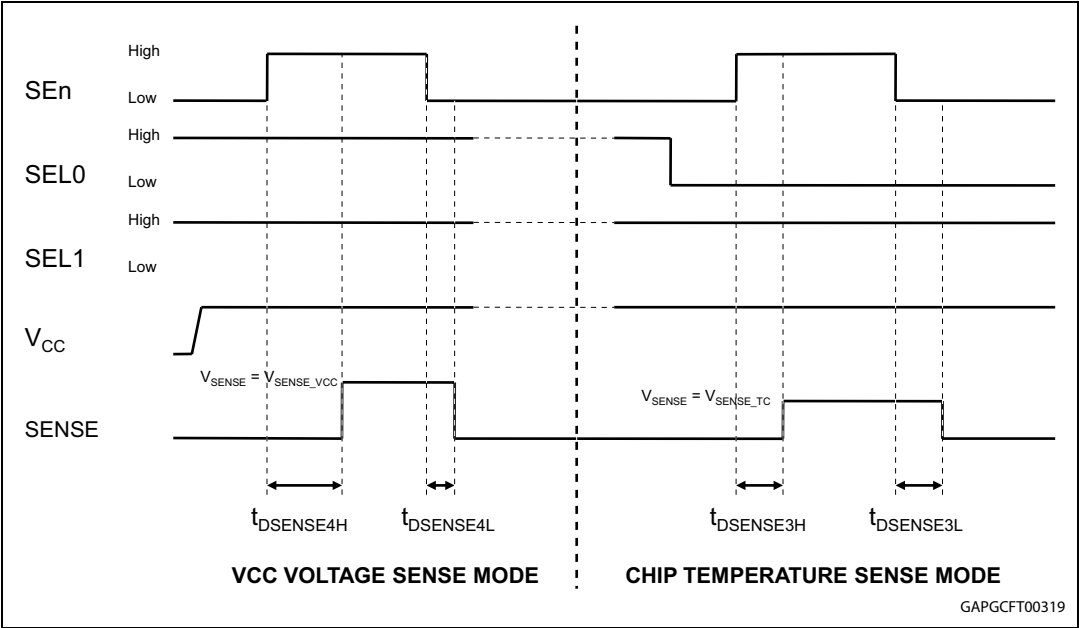


Figure 9. T_{DSTKON}

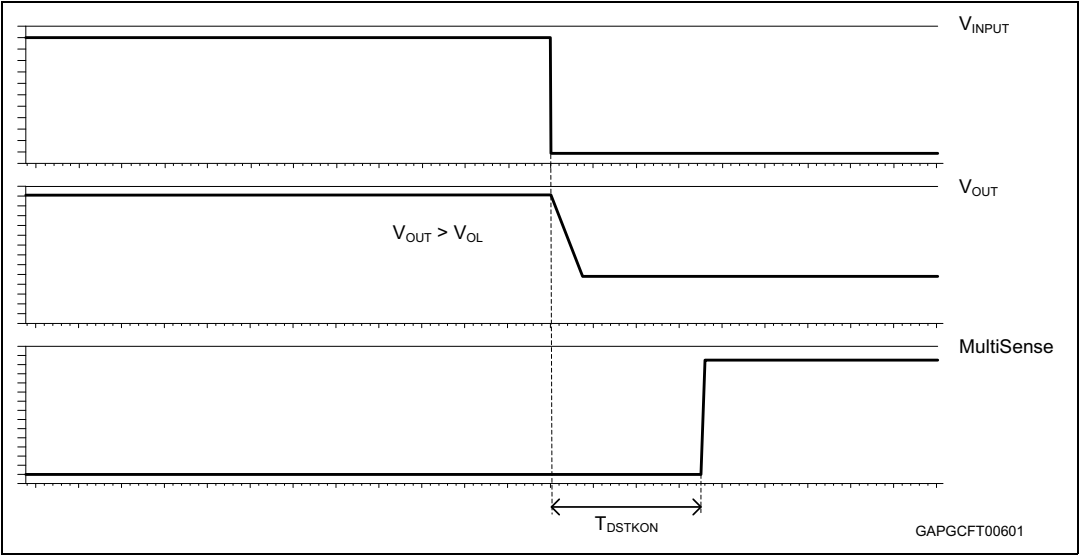


Table 10. Truth table

Mode	Conditions	IN _x	FR ⁽¹⁾	SEn	SEL _x ⁽¹⁾	OUT _x	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T _j < 150°C	L	X	Refer to Table 11		L	Refer to Table 11	
		H	L			H		Outputs configured for auto-restart
		H	H			H		Outputs configured for Latch-off ⁽¹⁾
Overload	Overload or short to GND causing: T _j > T _{TSD} or ΔT _j > ΔT _{j,SD}	L	X	Refer to Table 11		L	Refer to Table 11	
		H	L			H		Output cycles with temperature hysteresis
		H	H			L		Output latches-off ⁽¹⁾
Undervoltage	V _{CC} < V _{USD} (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when V _{CC} > V _{USD} + V _{USDhyst} (rising)
OFF-state diagnostics	Short to V _{CC}	L	X	Refer to Table 11		H	Refer to Table 11	
	Open-load	L	X			H		External pull-up
Negative output voltage	Inductive loads turn-off	L	X	Refer to Table 11		< 0 V	Refer to Table 11	

1. VN7050AJ-E only.

Table 11. MultiSense multiplexer addressing

SEn	SEL ₁	SEL ₀	MUX channel	MultiSense output			
				Nomal mode	Overload	OFF-state diag. ⁽¹⁾	Negative output
SO-8							
L	n.a.	n.a.	n.a.	Hi-Z			
H	n.a.	n.a.	Channel diagnostic	I _{SENSE} = 1/K * I _{OUT}	V _{SENSE} = V _{SENSEH}	V _{SENSE} = V _{SENSEH}	Hi-Z
PowerSSO-16							
H	L	L	Channel diagnostic	I _{SENSE} = 1/K * I _{OUT}	V _{SENSE} = V _{SENSEH}	V _{SENSE} = V _{SENSEH}	Hi-Z
H	L	H	Channel diagnostic	I _{SENSE} = 1/K * I _{OUT}	V _{SENSE} = V _{SENSEH}	V _{SENSE} = V _{SENSEH}	Hi-Z
H	H	L	T _{CHIP} Sense	V _{SENSE} = V _{SENSE_TC}			
H	H	H	V _{CC} Sense	V _{SENSE} = V _{SENSE_VCC}			

1. In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic.
 Example 1: FR = 1; IN₀ = 0; OUT₀ = L (latched); MUX channel = channel 0 diagnostic; Mutisense = 0
 Example 2: FR = 1; IN₀ = 0; OUT₀ = latched, V_{OUT0} > V_{OL}; MUX channel = channel 0 diagnostic; Mutisense = V_{SENSEH}

2.4 Waveforms

Figure 10. Latch functionality - behavior in hard short circuit condition ($T_{AMB} \ll T_{TSD}$)

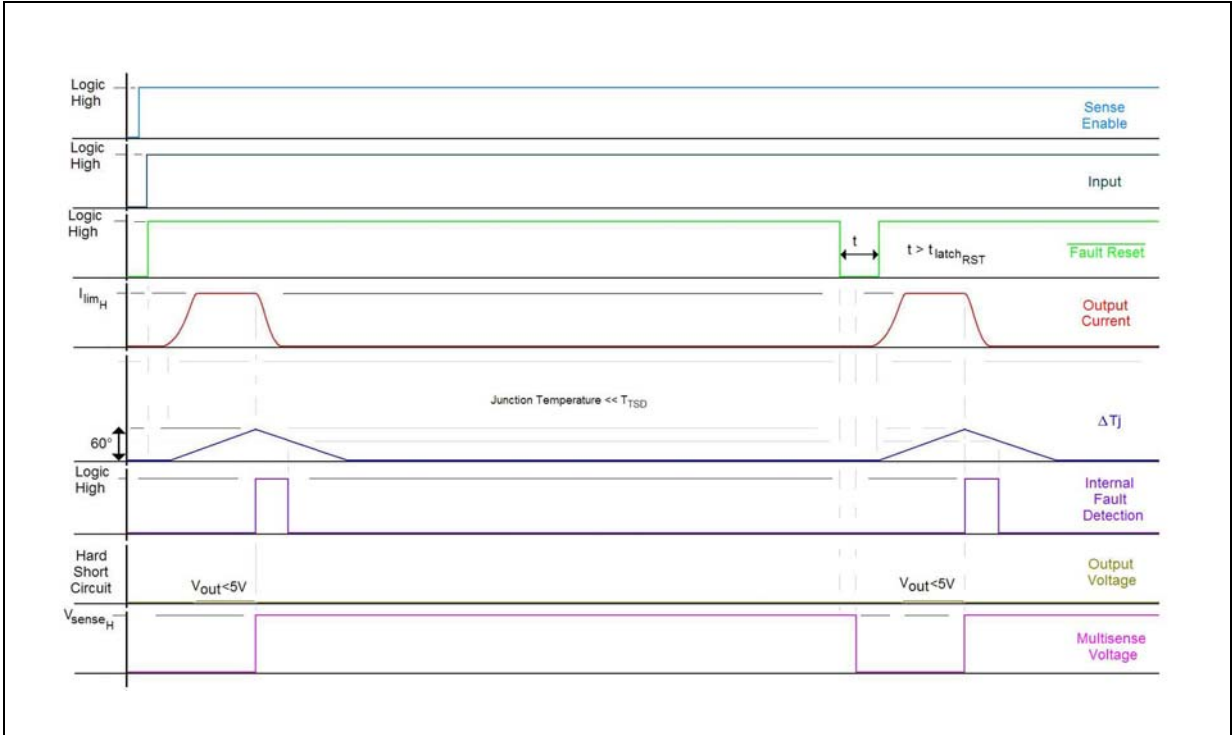


Figure 11. Latch functionality - behavior in hard short circuit condition

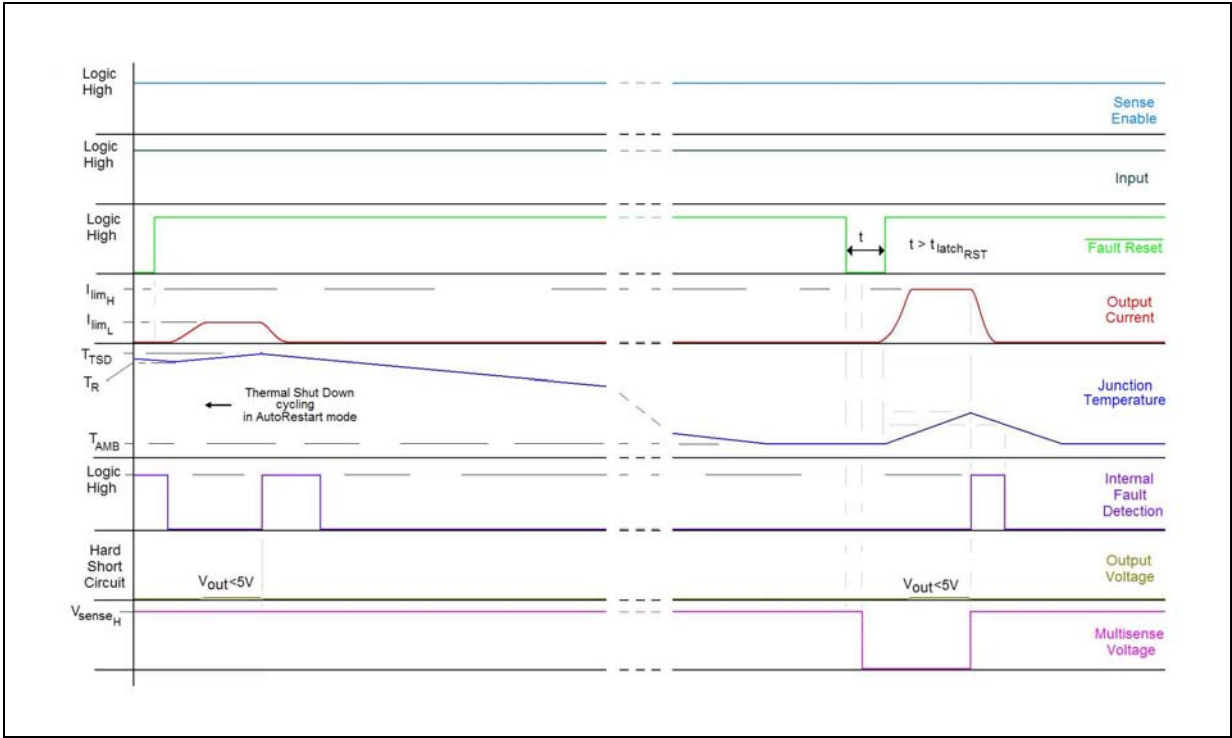


Figure 12. Latch functionality - behavior in hard short circuit condition (autorestart mode + latch off)

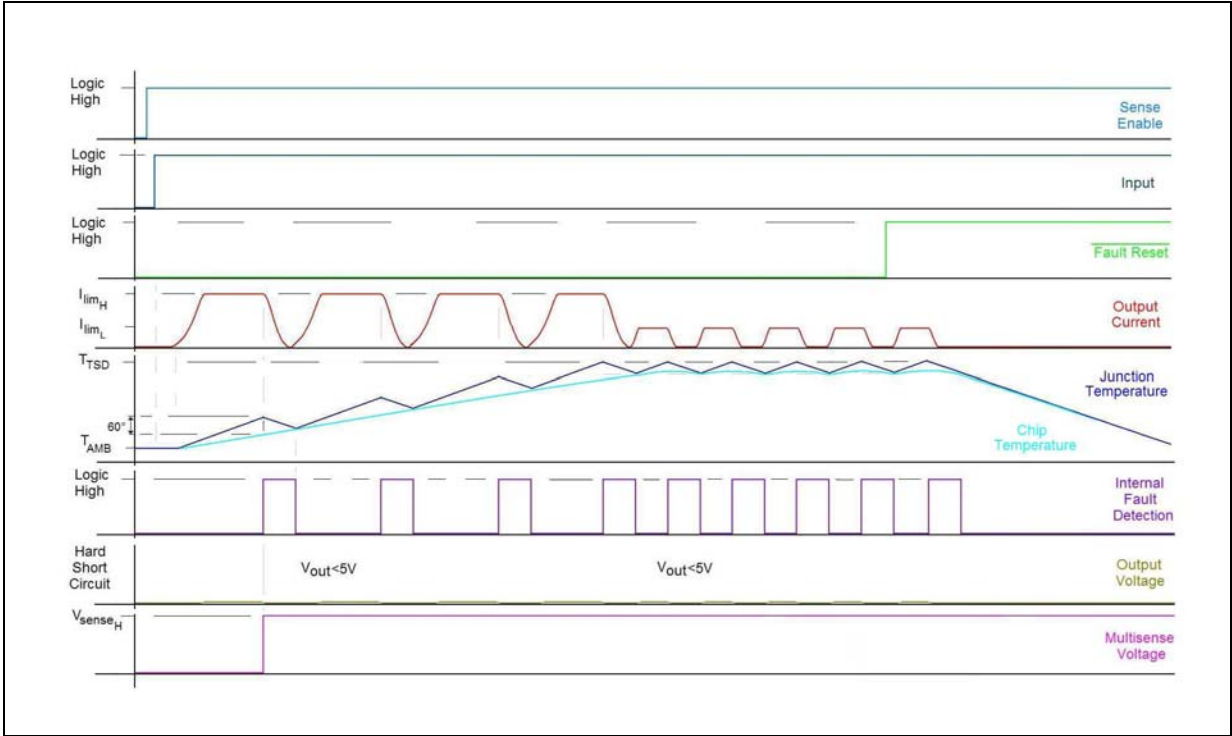


Figure 13. Standby mode activation

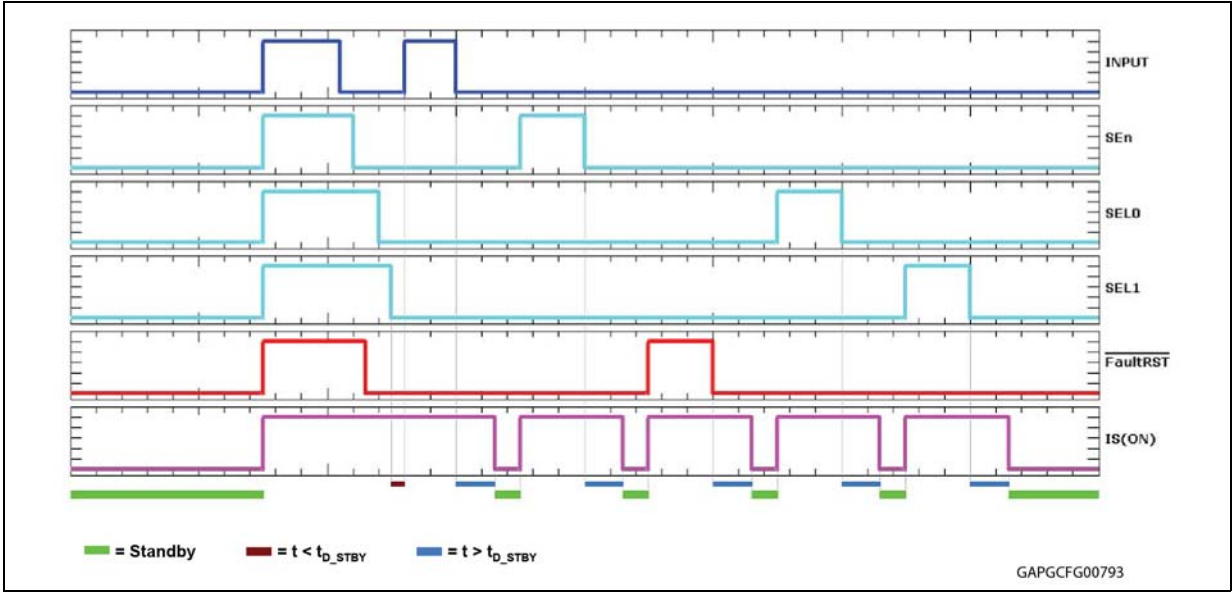
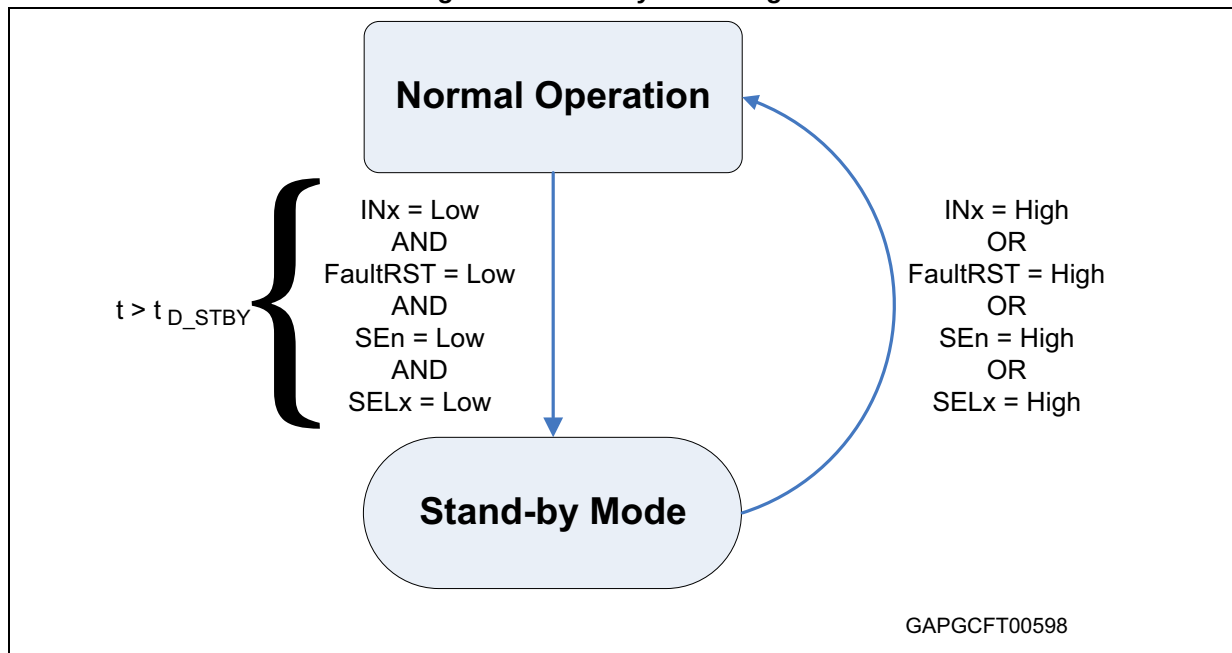


Figure 14. Standby state diagram



2.5 Electrical characteristics curves

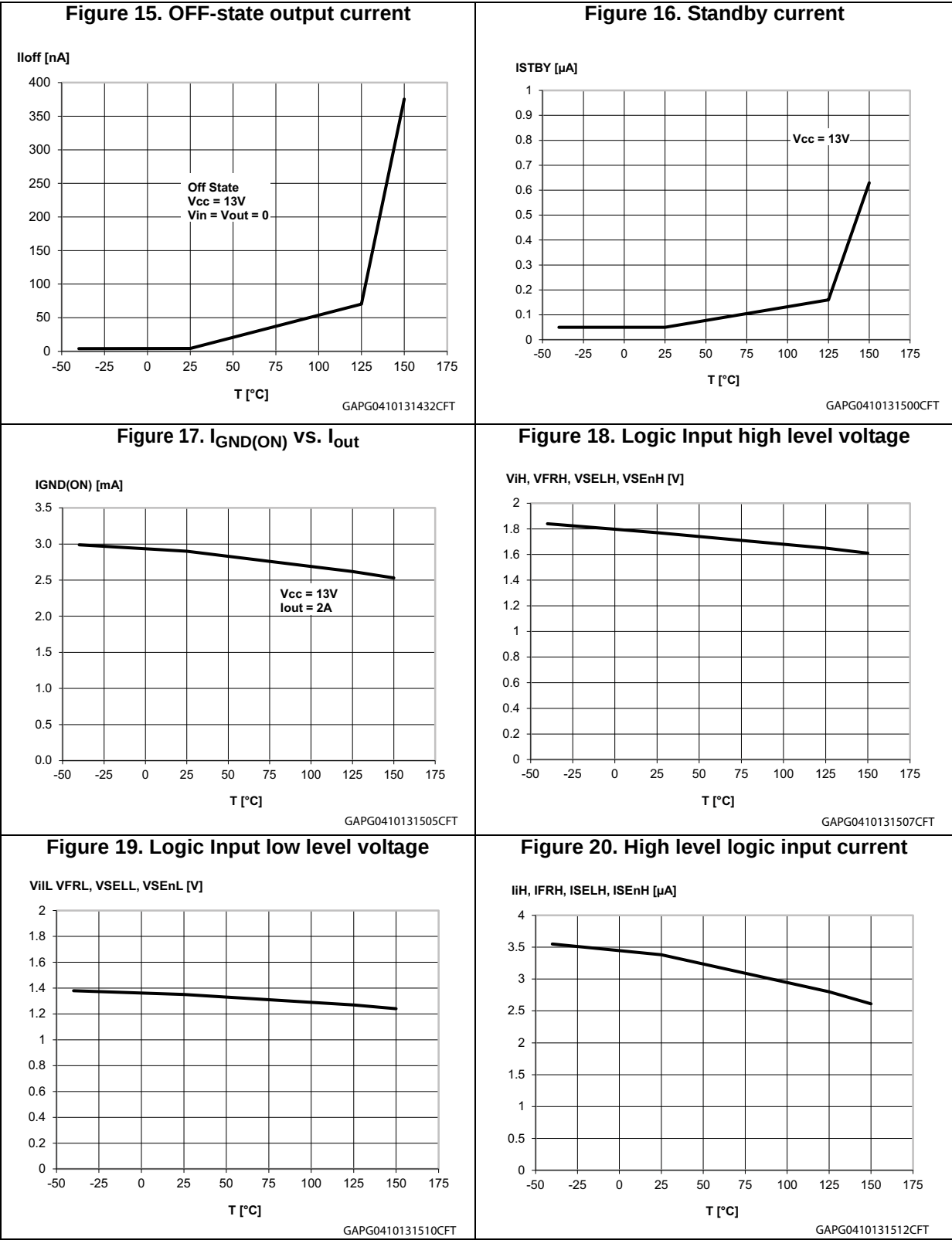


Figure 21. Low level logic input current

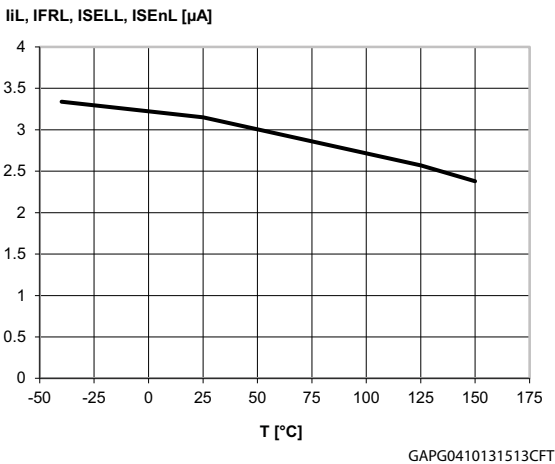


Figure 22. Logic Input hysteresis voltage

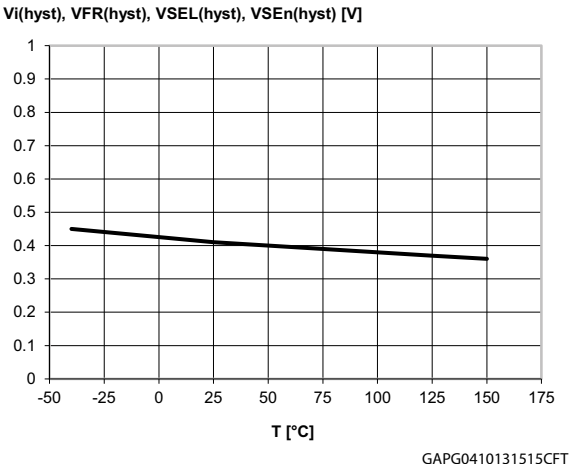


Figure 23. FaultRST Input clamp voltage

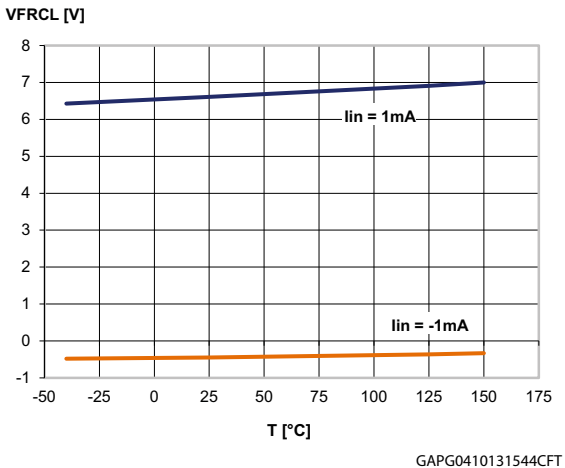


Figure 24. Undervoltage shutdown

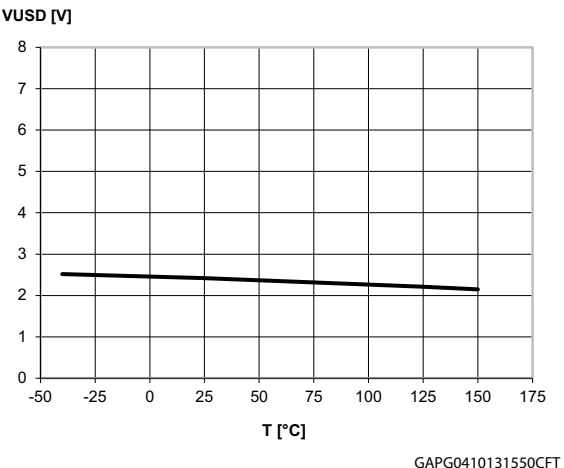


Figure 25. On-state resistance vs. T_{case}

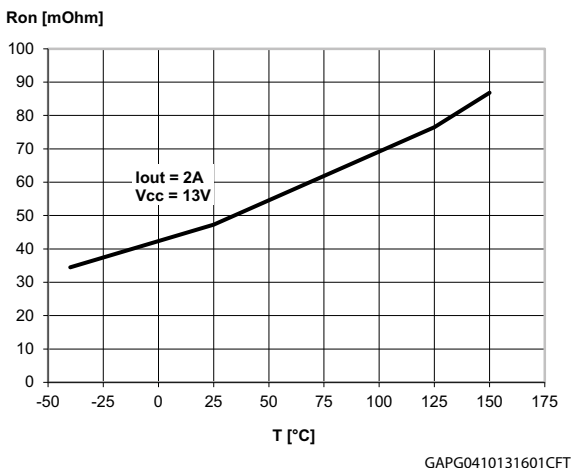


Figure 26. On-state resistance vs. V_{CC}

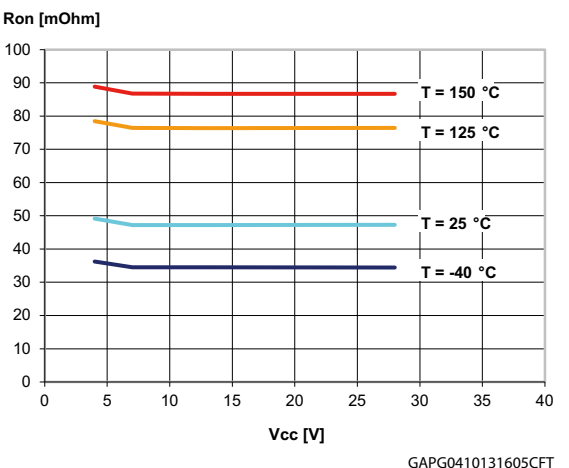


Figure 27. Turn-on voltage slope

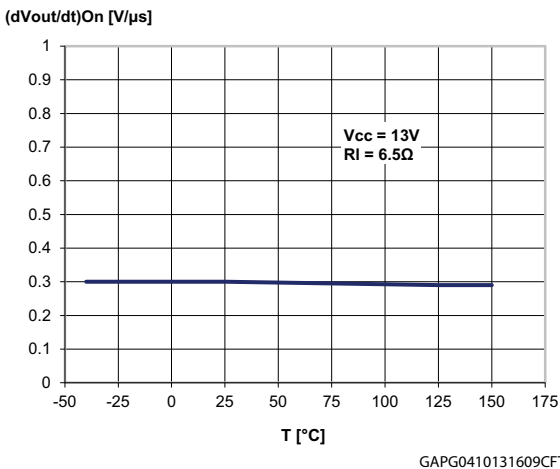


Figure 28. Turn-off voltage slope

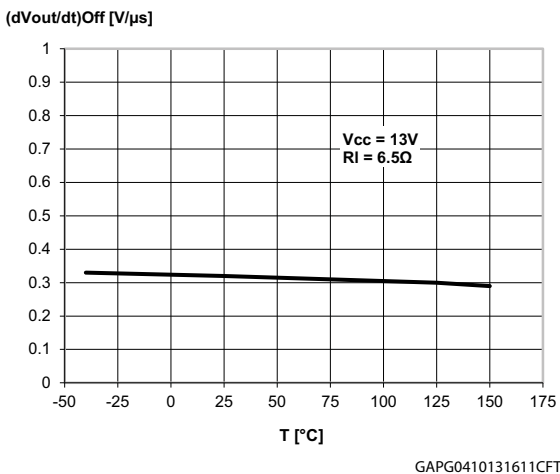


Figure 29. Won vs. T_{case}

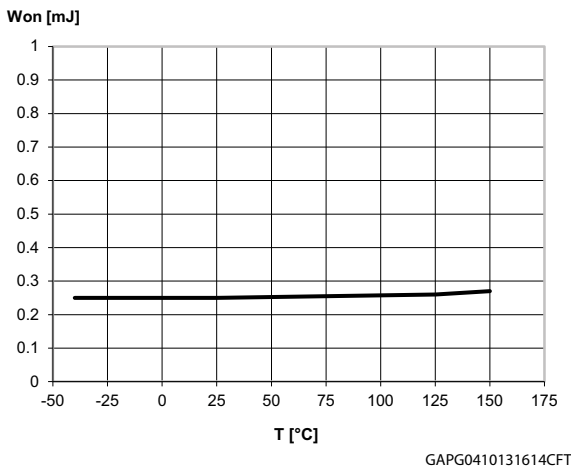


Figure 30. Woff vs. T_{case}

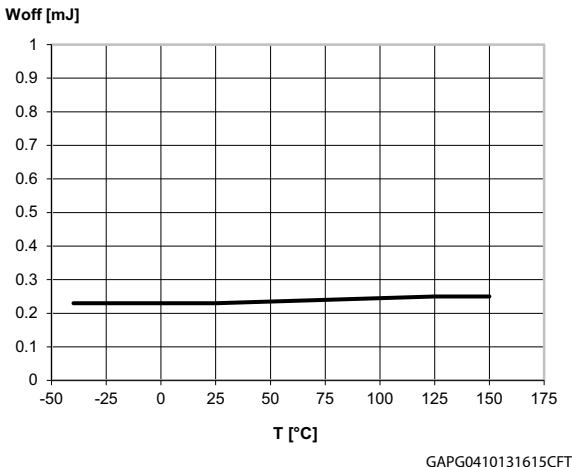


Figure 31. I_{LIMH} vs. T_{case}

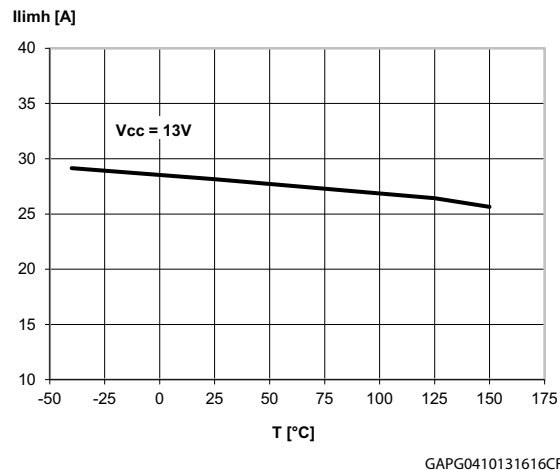
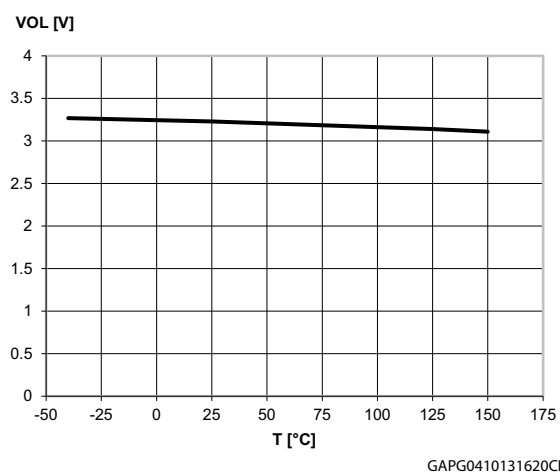
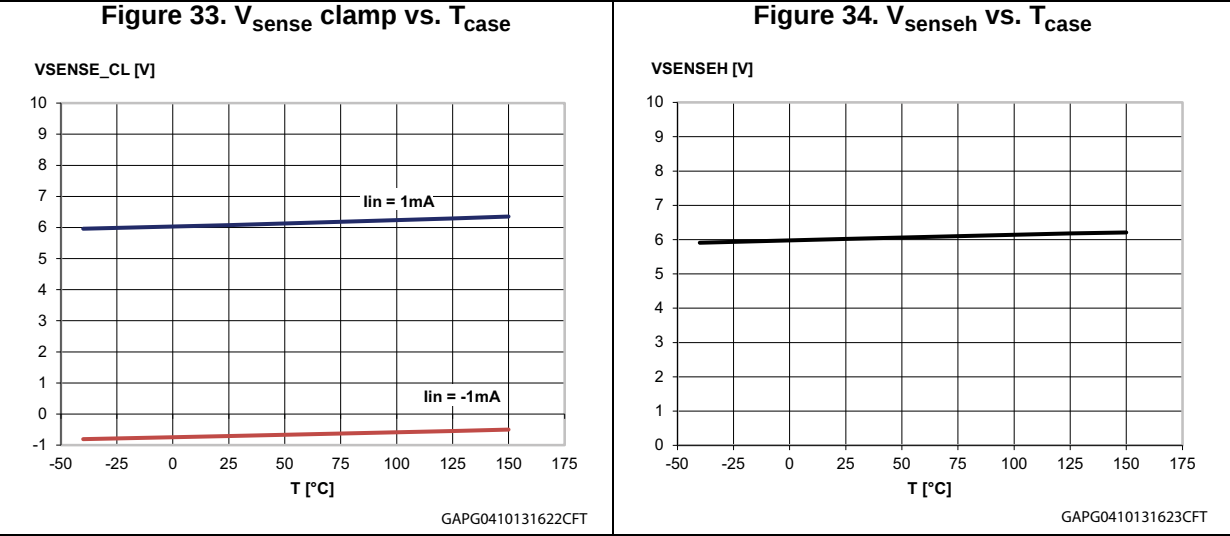


Figure 32. OFF-state open-load voltage detection threshold





3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD} . According to the voltage level on the FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FaultRST = Low) or remains off (FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FaultRST pin, the device switches on again as soon as its junction temperature drops to T_R (see [Table 8](#), FaultRST = Low) or remains off (FaultRST = High).

3.3 Current limitation

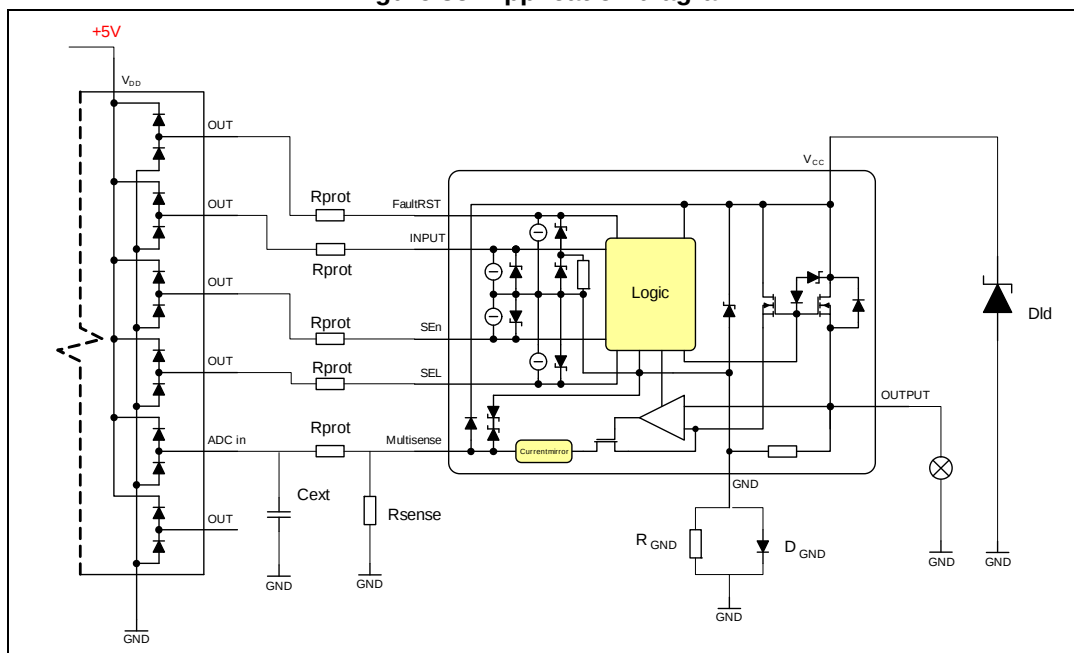
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH} , by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG} (see [Table 8](#)), allowing the inductor energy to be dissipated without damaging the device.

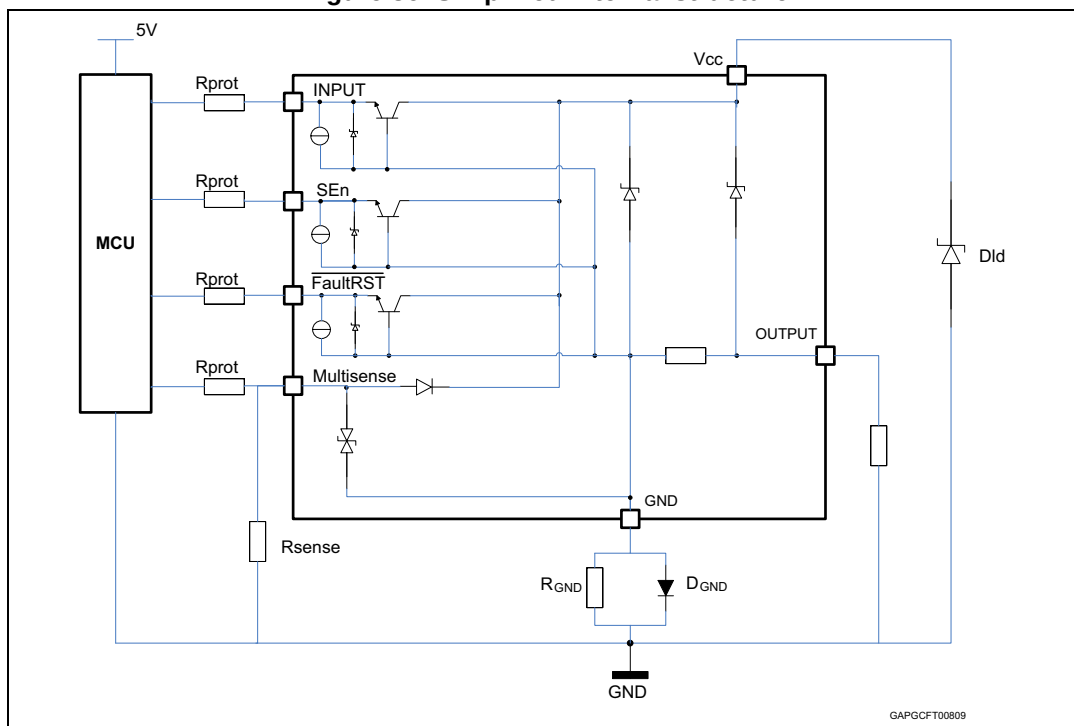
4 Application information

Figure 35. Application diagram



4.1 GND protection network against reverse battery

Figure 36. Simplified internal structure



4.1.1 Diode (D_{GND}) in the ground line

A resistor (typ. $R_{GND} = 4.7 \text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ($\approx 600 \text{ mV}$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO 7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in [Table 12](#).

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

Table 12. ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	$U_S^{(1)}$		min	max	
1	III	-112V	500 pulses	0,5 s		2ms, 10 Ω
2a	III	+55V	500 pulses	0,2 s	5 s	50 μ s, 2 Ω
3a	IV	-220V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	IV	+150V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4 ⁽²⁾	IV	-7V	1 pulse			100ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B ⁽³⁾		40V	5 pulse	1 min		400ms, 2 Ω

1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

2. Test pulse from ISO 7637-2:2004(E).

3. With 40 V external suppressor referred to ground ($-40^\circ\text{C} < T_j < 150^\circ\text{C}$).

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins to latch-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1

$$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -150\text{ V}$; $I_{latchup} \geq 20\text{mA}$; $V_{OH\mu C} \geq 4.5\text{V}$

$$7.5\text{ k}\Omega \leq R_{prot} \leq 140\text{ k}\Omega.$$

Recommended values: $R_{prot} = 15\text{ k}\Omega$

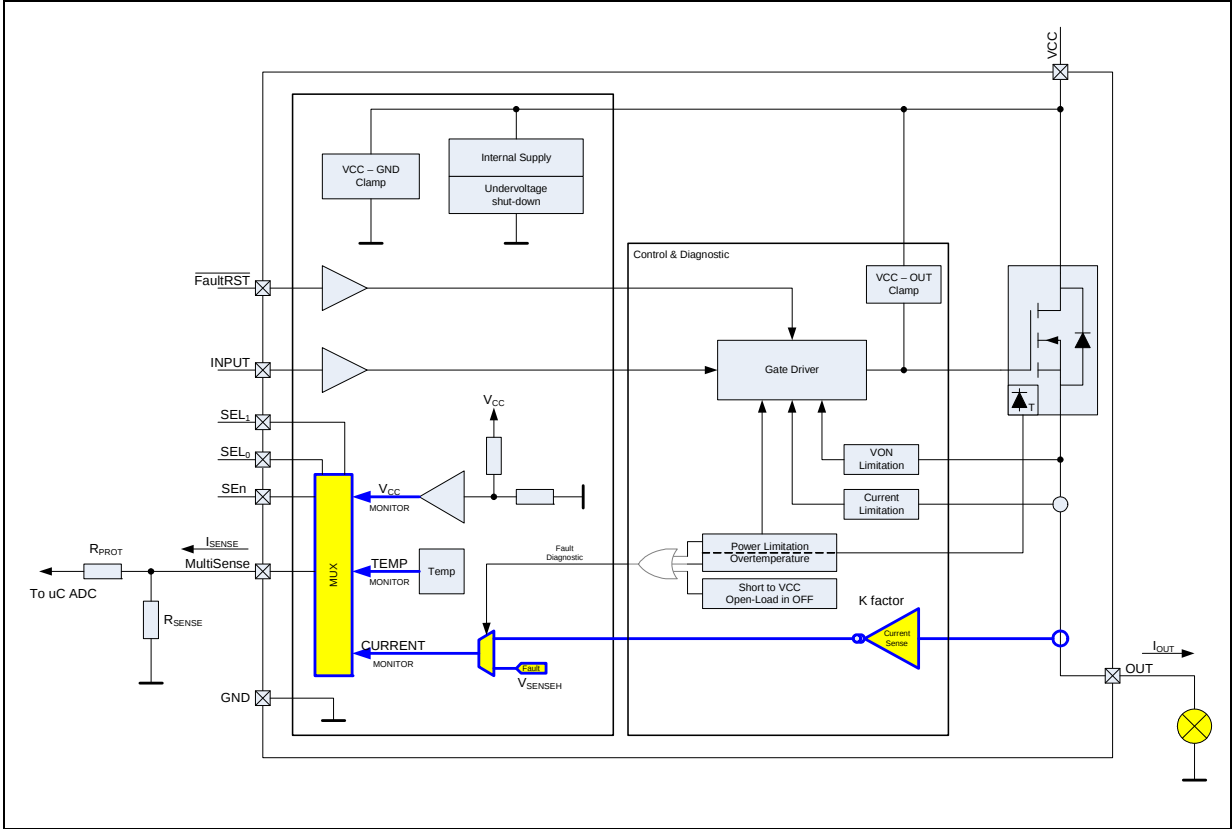
4.4 Multisense - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (Multisense) delivering the following signals:

- Current monitor: current mirror of channel output current
- V_{CC} monitor: voltage propotional to V_{CC}
- T_{CASE} : voltage propotional to chip temperature

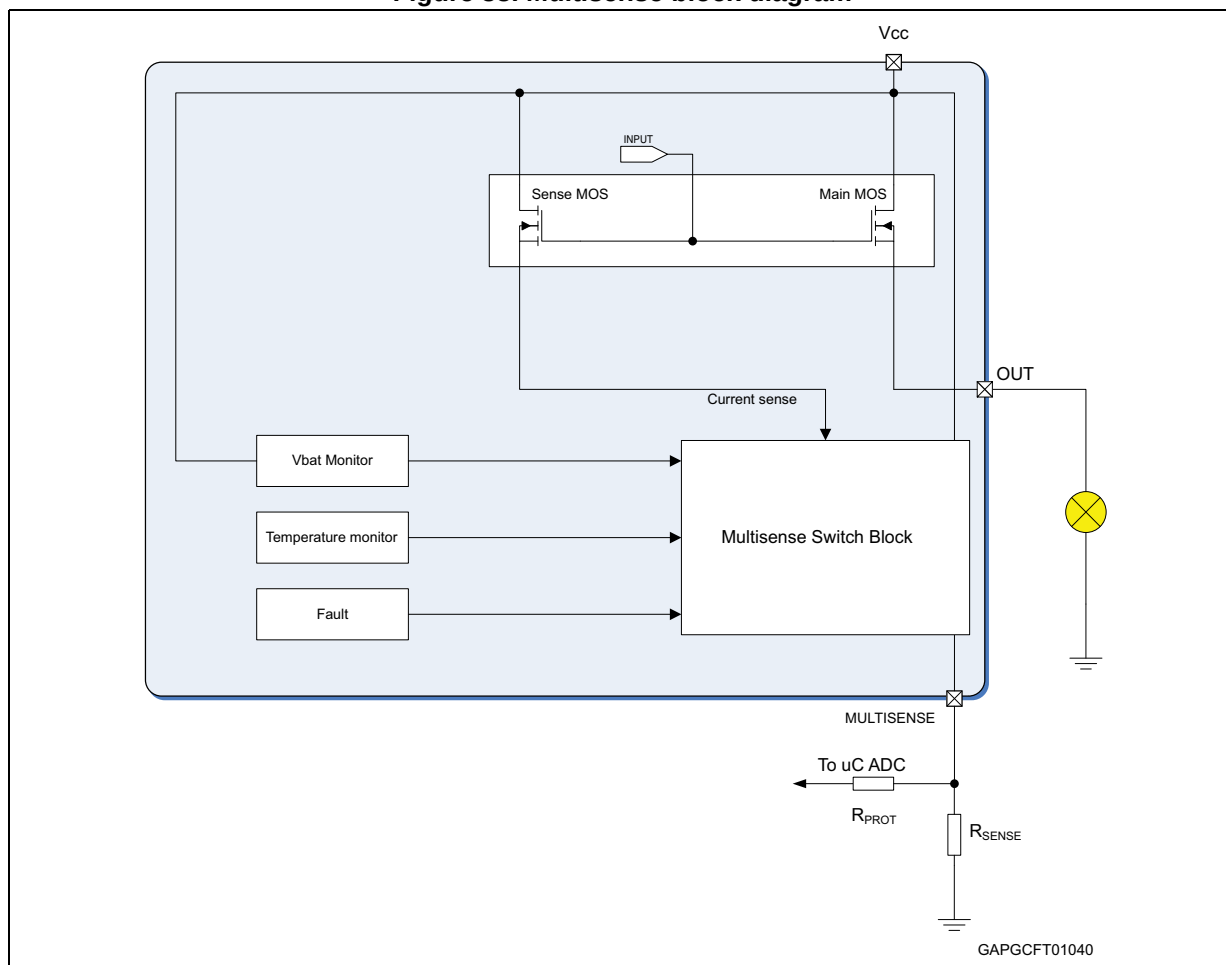
Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in [Table 11](#).

Figure 37. Multisense and diagnostic – block diagram



4.4.1 Principle of Multisense signal generation

Figure 38. Multisense block diagram



Current monitor

When current mode is selected in the Multisense, this output is capable to provide:

- **Current mirror proportional to the load current in normal operation**, delivering current proportional to the load according to known ratio named **K**
- **Diagnostics flag in fault conditions** delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE} , can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE} , allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by Multisense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE} : $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

- V_{SENSE} is voltage measurable on R_{SENSE} resistor
- I_{SENSE} is current provided from MultiSense pin in current output mode
- I_{OUT} is current flowing through output
- K factor represent the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between I_{OUT} and I_{SENSE} .

In case of power limitation/overtemperature, the fault is indicated by the Multisense pin which is switched to a “current limited” voltage source, V_{SENSEH} (see [Table 9](#)).

The typical behavior in case of overload or hard short circuit is shown in [Figure 10](#), [Figure 11](#) and [Figure 12](#).

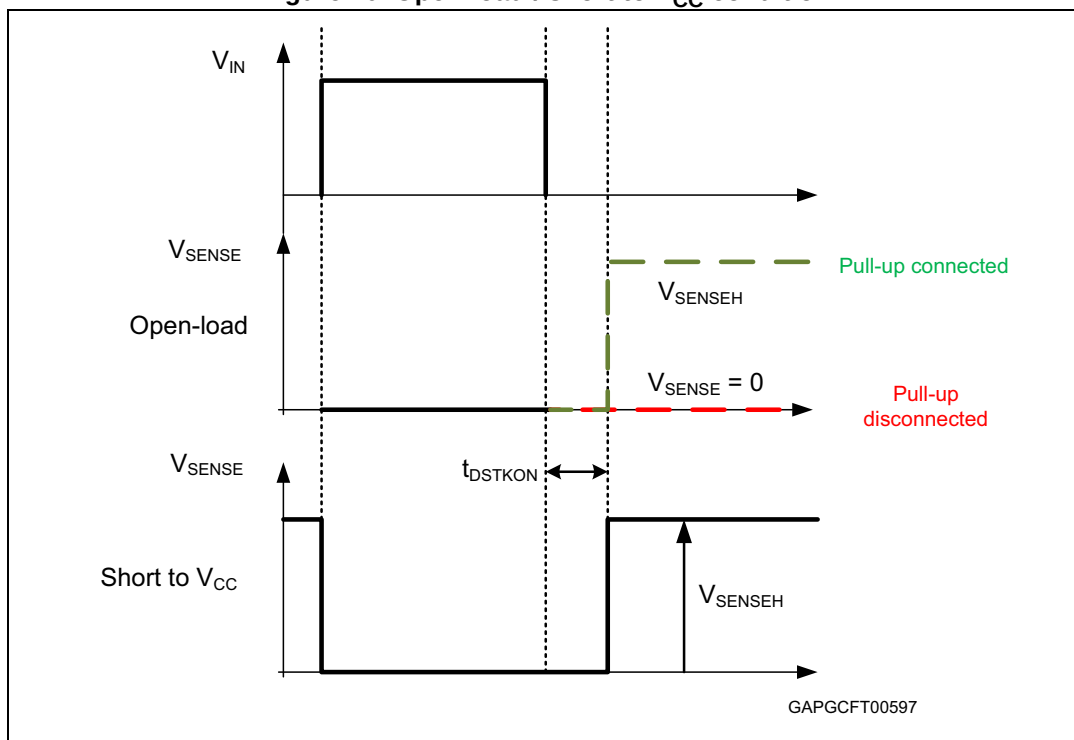
Figure 40. Open-load / short to V_{CC} condition

Table 13. Multisense pin levels in off-state

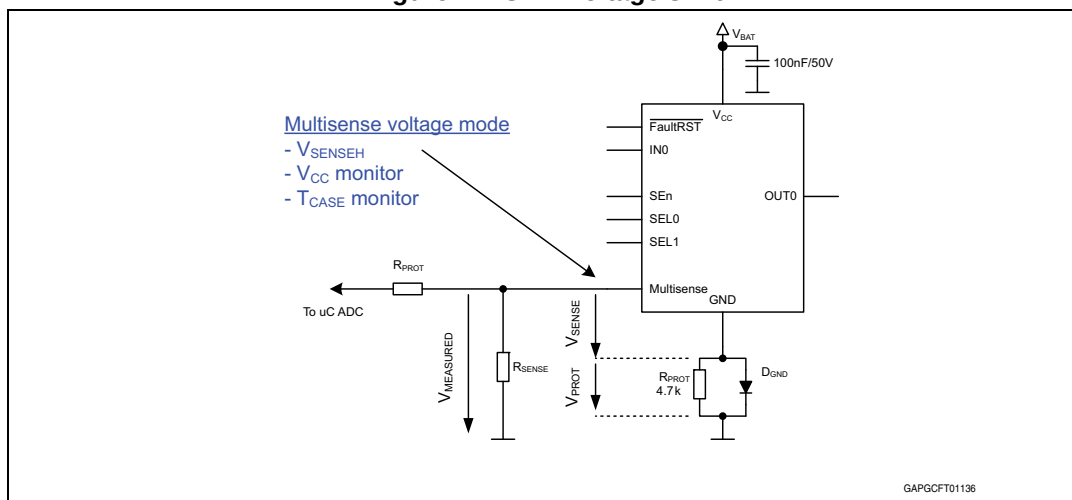
Condition	Output	Multisense	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 T_{CASE} and V_{CC} monitor

In this case, MultiSense output operates in voltage mode and output level is referred to device GND. Care must be taken in case a GND network protection is used, because of a voltage shift is generated between device GND and the microcontroller input GND reference.

Figure 41 shows link between $V_{MEASURED}$ and real V_{SENSE} signal.

Figure 41. GND voltage shift



V_{CC} monitor

Battery monitoring channel provides $V_{SENSE} = V_{CC} / 4$.

Case temperature monitor

Case temperature monitor is capable to provide information about actual device temperature. Since diode is used for temperature sensing, following equation describe link between temperature and output V_{SENSE} level:

$$V_{SENSE_TC}(T) = V_{SENSE_TC}(T_0) + dV_{SENSE_TC} / dT * (T - T_0)$$

where dV_{SENSE_TC} / dT ~ typically -5.5 mV/K (for temperature range (-40°C to +150°C)).

4.4.3 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU} .

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

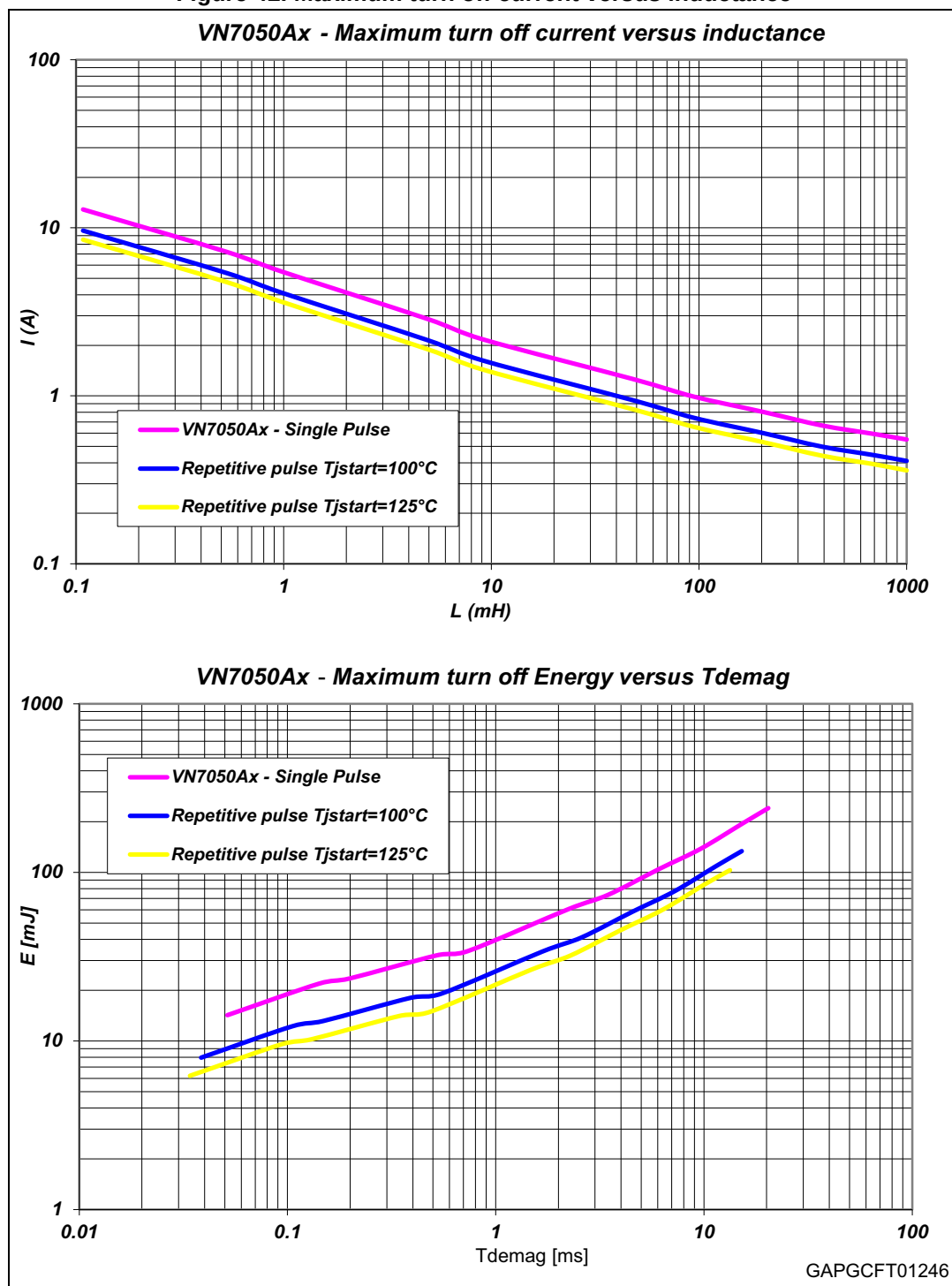
R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with to following equation:

Equation 2

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min @ 4V}}$$

4.5 Maximum demagnetization energy ($V_{CC} = 16\text{ V}$)

Figure 42. Maximum turn off current versus inductance



Note:

Values are generated with $R_L = 0\ \Omega$.

In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

5 Package and PCB thermal data

5.1 PowerSSO-16 thermal data

Figure 43. PowerSSO-16 on two-layers PCB (2s0p to JEDEC JESD 51-5)

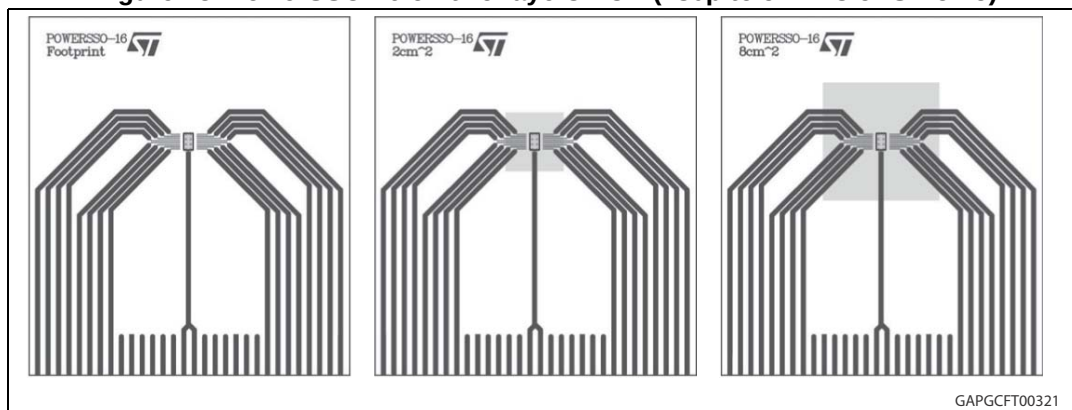


Figure 44. PowerSSO-16 on four-layers PCB (2s2p to JEDEC JESD 51-7)

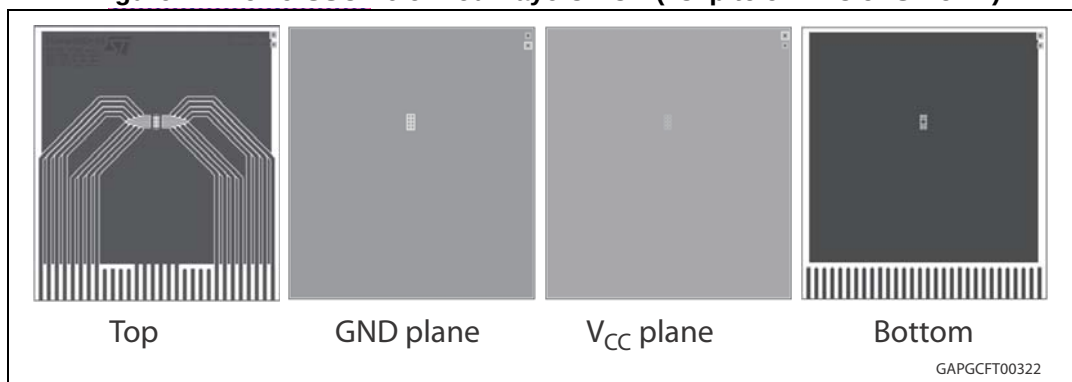
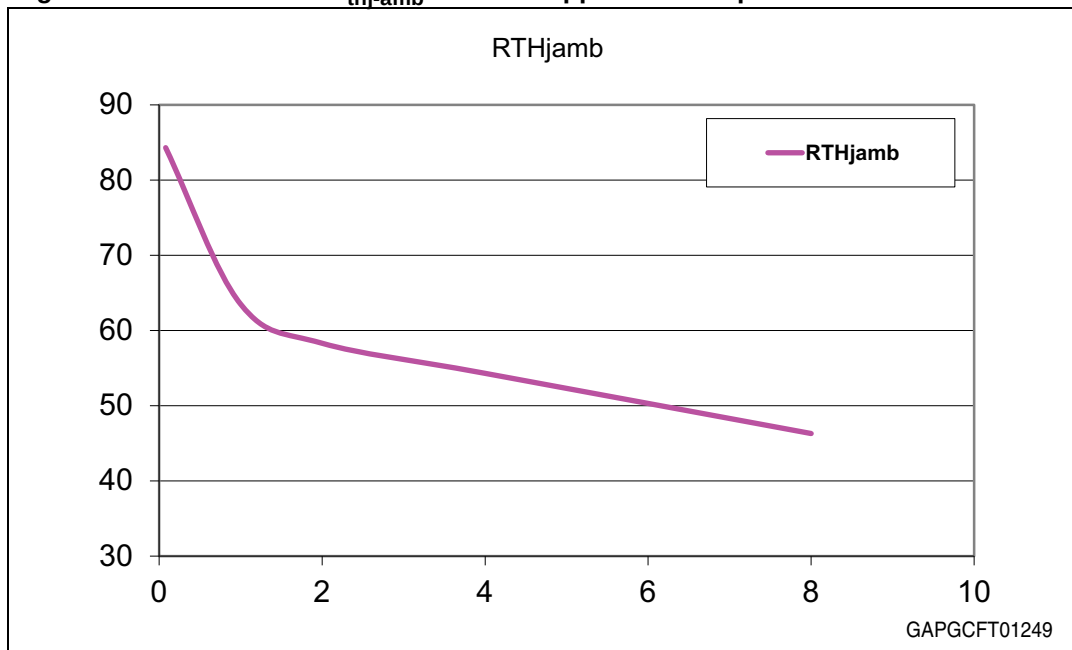
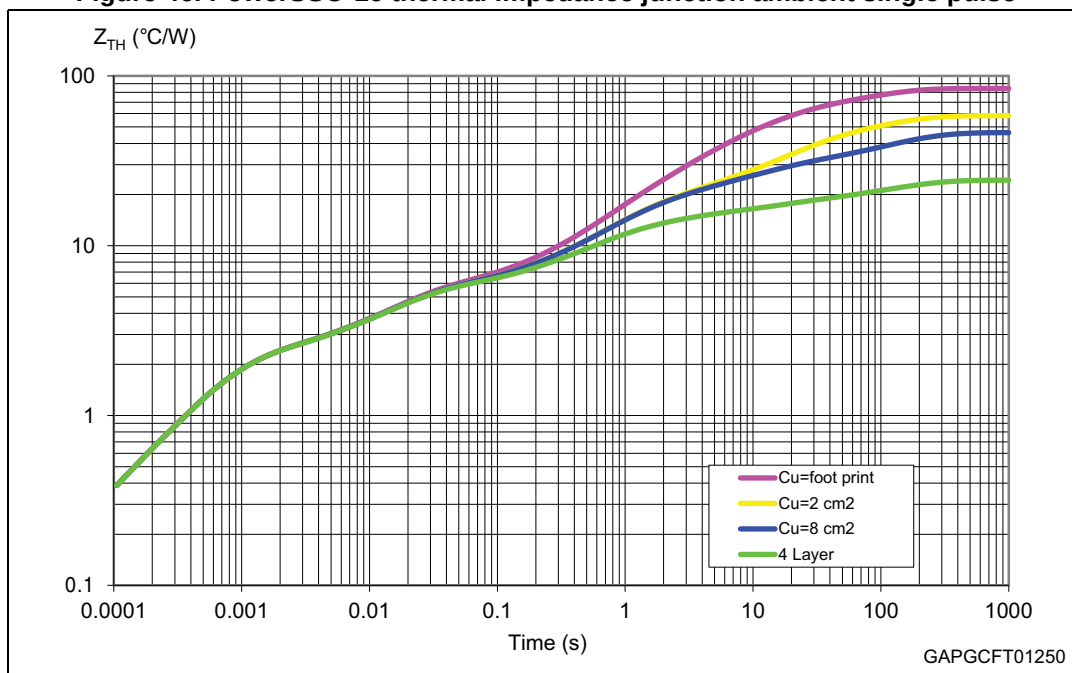


Table 14. PCB properties

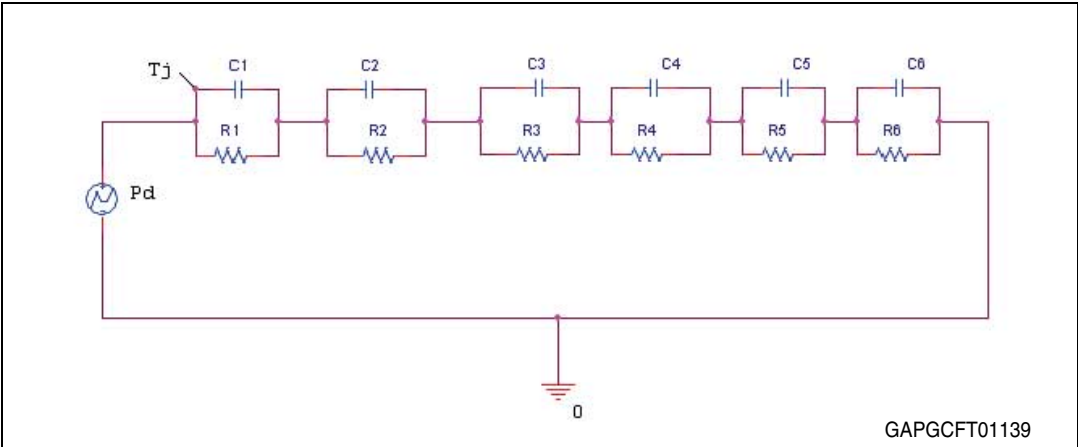
Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	2.2 mm x 3.9 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm ² or 8 cm ²

Figure 45. PowerSSO-16 $R_{thj-amb}$ vs PCB copper area in open box free air conditions**Figure 46. PowerSSO-16 thermal impedance junction ambient single pulse****Equation 3: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 47. Thermal fitting model for PowerSSO-16



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameters

Area/island (cm ²)	Footprint	2	8	4L
R1 (°C/W)	2.1			
R2 (°C/W)	3.2			
R3 (°C/W)	7	7	7	5
R4 (°C/W)	14	6	6	4
R5 (°C/W)	30	20	10	3
R6 (°C/W)	26	20	18	7
C1 (W.s/°C)	0.0003			
C2 (W.s/°C)	0.005			
C3 (W.s/°C)	0.1			
C4 (W.s/°C)	0.2	0.3	0.3	0.4
C5 (W.s/°C)	0.4	1	1	4
C6 (W.s/°C)	3	5	7	18

5.2 SO-8 thermal data

Figure 48. SO-8 on two-layers PCB (2s0p to JEDEC JESD 51-5)

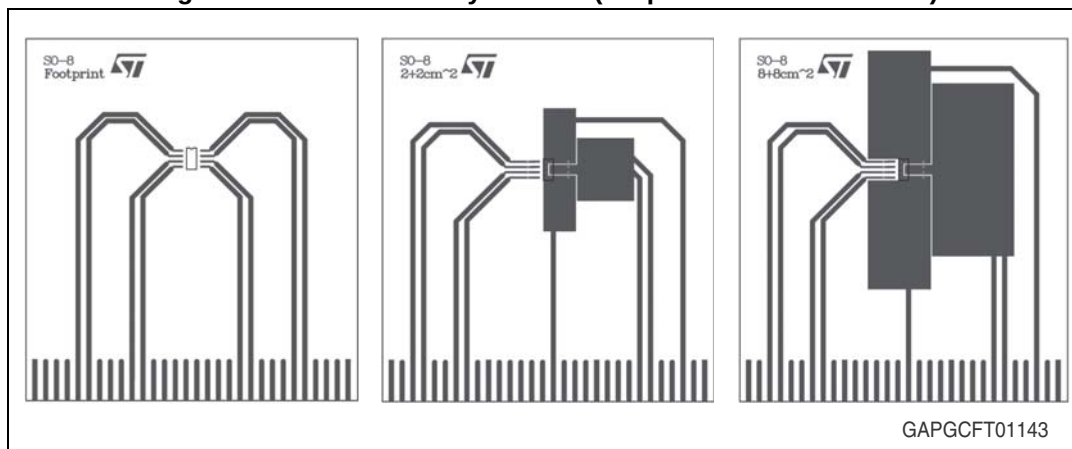


Figure 49. SO-8 on four-layers PCB (2s2p to JEDEC JESD 51-7)

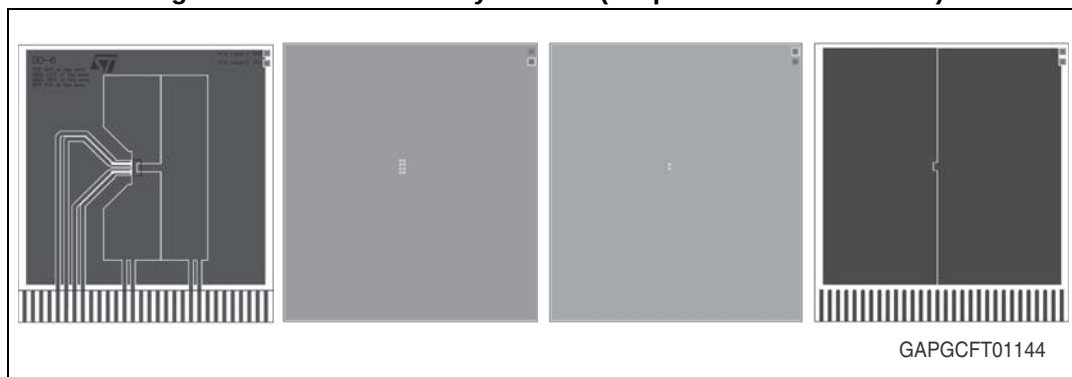


Table 16. PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 + 2 cm ² or 8 + 8 cm ²

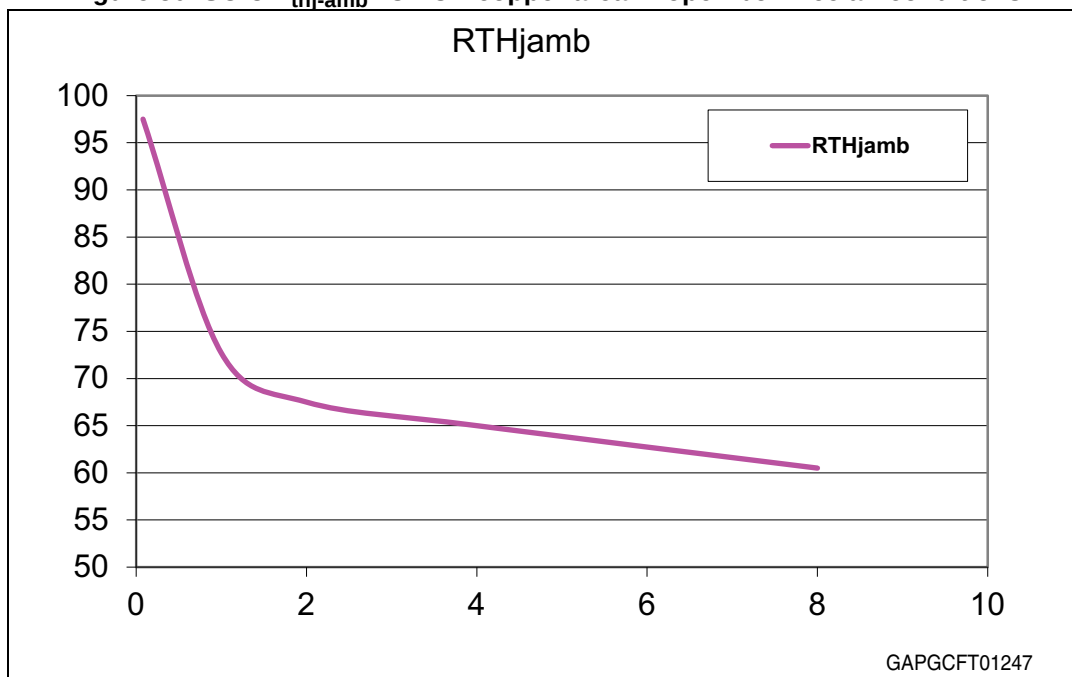
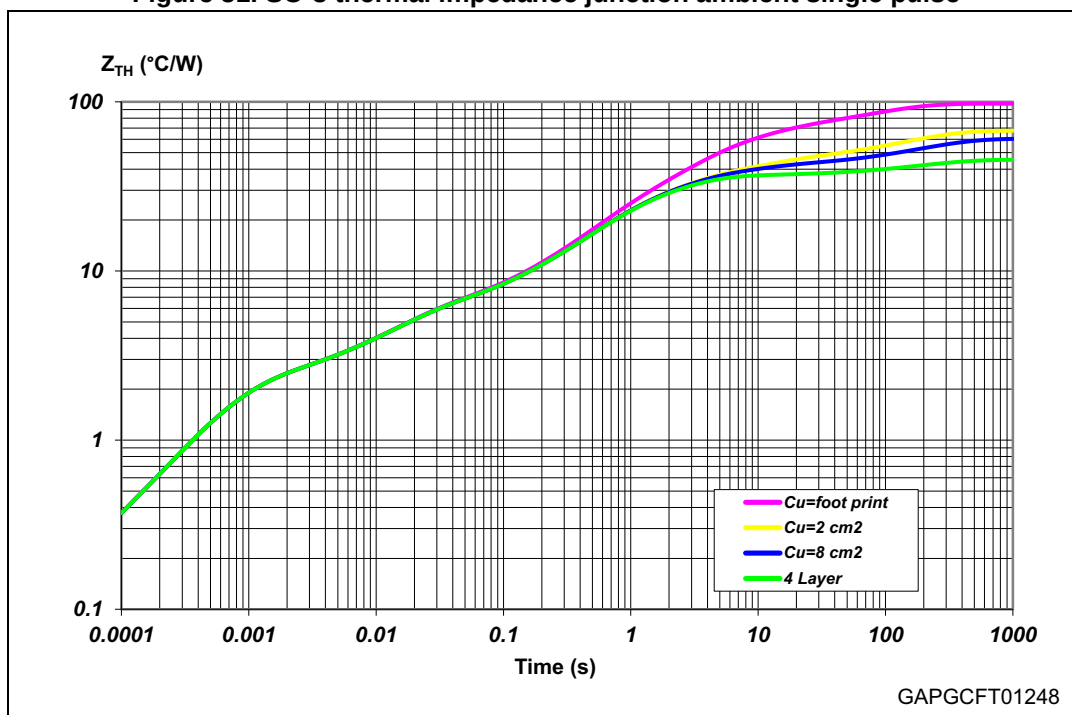
Figure 50. SO-8 $R_{thj-amb}$ vs PCB copper area in open box free air conditions

Figure 51. SO-8 thermal impedance junction ambient single pulse

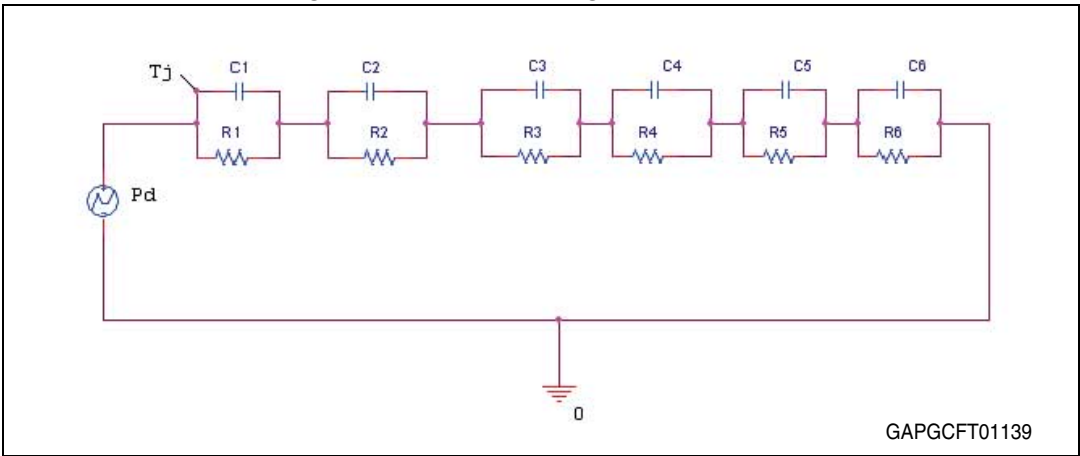


Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 52. Thermal fitting model for SO-8



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 17. Thermal parameters

Area/island (cm ²)	Footprint	2	8	4L
R1 (°C/W)	2.1			
R2 (°C/W)	3.5			
R3 (°C/W)	10			
R4 (°C/W)	28	17	17	17
R5 (°C/W)	24	12	9	4
R6 (°C/W)	30	23	19	9
C1 (W.s/°C)	0.0003			
C2 (W.s/°C)	0.0045			
C3 (W.s/°C)	0.05			
C4 (W.s/°C)	0.1			
C5 (W.s/°C)	0.4	0.8	0.8	0.8
C6 (W.s/°C)	3	7	11	22

6 Package information

6.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

6.2 PowerSSO-16 package information

Figure 53. PowerSSO-16 package dimensions

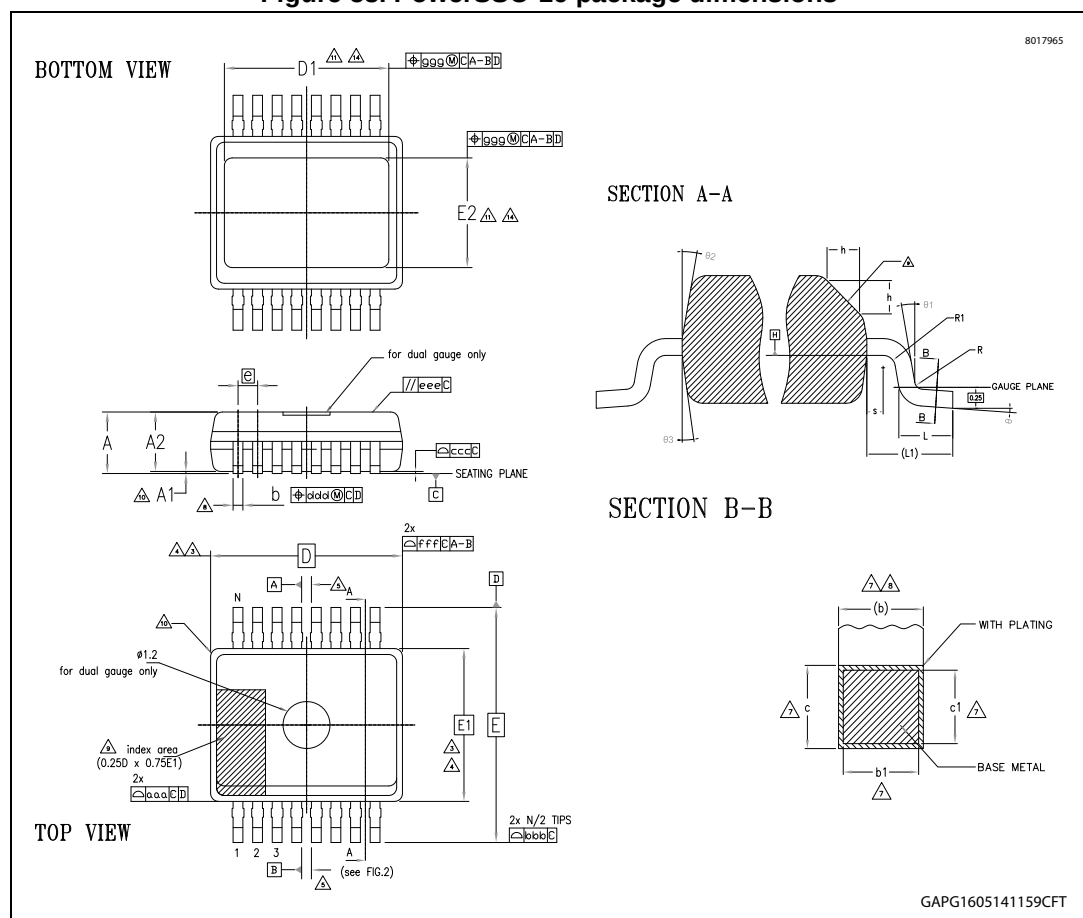


Table 18. PowerSSO-16 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
$\Theta 1$	0°		
$\Theta 2$	5°		15°
$\Theta 3$	5°		15°
A			1.70
A1	0.00		0.10
A2	1.10		1.60
b	0.20		0.30
b1	0.20	0.25	0.28
c	0.19		0.25
c1	0.19	0.20	0.23
D	4.90 BSC		
D1	2.90		3.50
e	0.50 BSC		
E	6.00 BSC		
E1	3.90 BSC		
E2	2.20		2.80
h	0.25		0.50
L	0.40	0.60	0.85
L1	1.00 REF		
N	16		
R	0.07		
R1	0.07		
S	0.20		
Tolerance of form and position			
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.08		
eee	0.10		
fff	0.10		
ggg	0.15		

6.3 SO-8 package information

Figure 54. SO-8 package dimensions

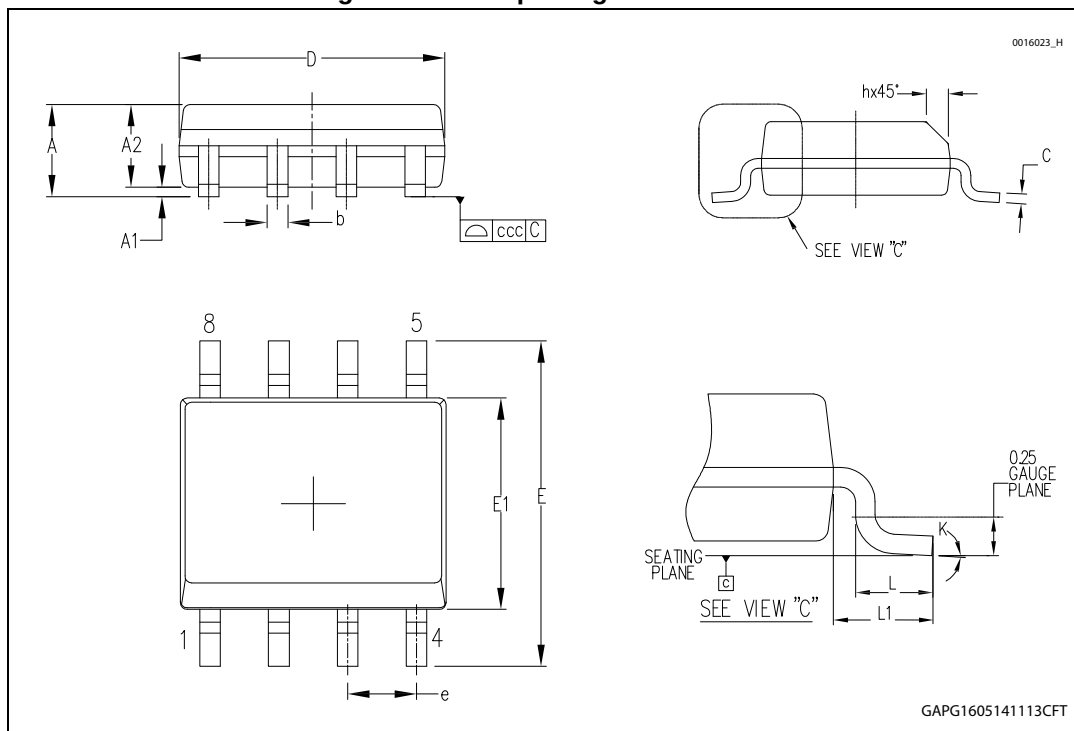


Table 19. SO-8 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

6.4 Packing information

Figure 55. SO-8 tube shipment (no suffix)

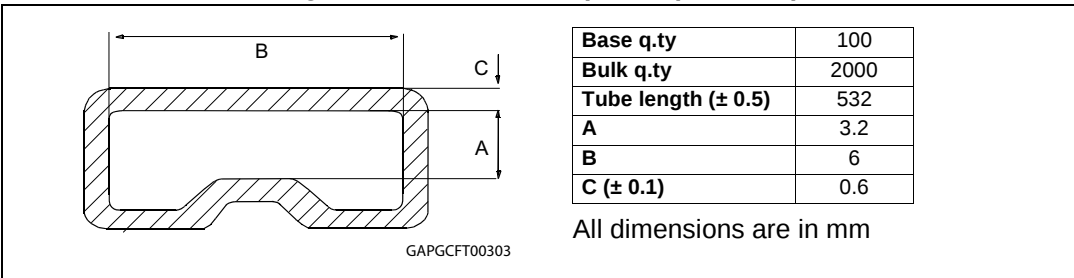
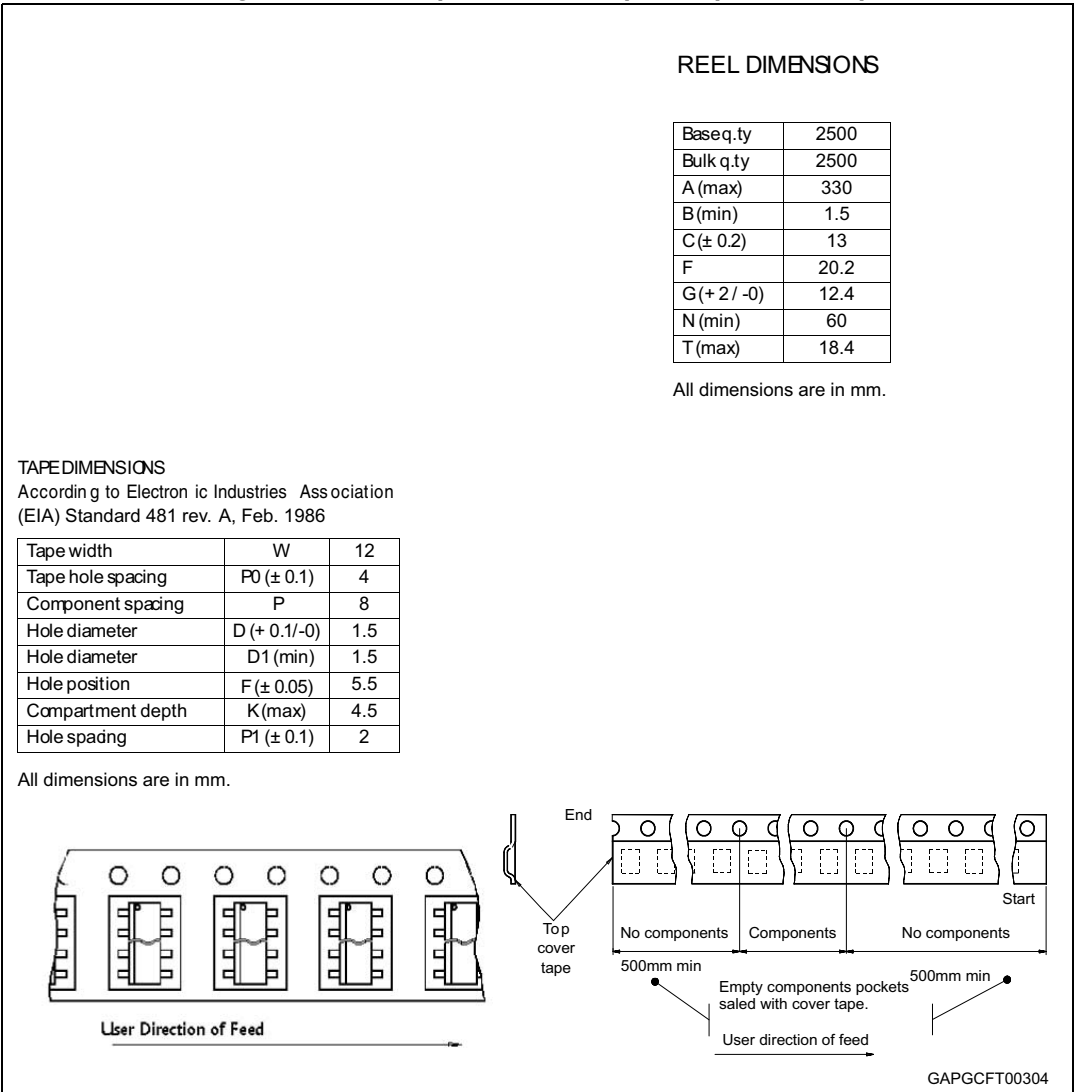


Figure 56. SO-8 tape and reel shipment (suffix “TR”)



7 Order codes

Table 20. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-16	VN7050AJ-E	VN7050AJTR-E
SO-8	VN7050AS-E	VN7050ASTR-E

8 Revision history

Table 21. Document revision history

Date	Revision	Changes
25-Oct-2011	1	Initial release
12-Dec-2012	2	Updated Features list Updated Table 1: Pin functions and Table 3: Absolute maximum ratings: – V_{CCPK}, I_{SENSE}, V_{ESD}: updated value – V_{CCJS}: added row – $-V_{SENSE}$: removed row Table 5: Power section: – $V_{USDRreset}$, $I_{GND(ON)}$: added row – V_{clamp}: updated test conditions Updated Table 6: Switching ($V_{CC} = 13\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$, unless otherwise specified) Table 8: Protections ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$): – I_{LIMH}, T_R: added note – t_{LATCH_RST}: added note, updated typ and max values – V_{ON}: updated test conditions Table 9: MultiSense ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$): – V_{SENSE_CL}: updated values; – K_{OL}, K_{LED}, K_0, K_1, K_2, K_3, I_{SENSE0}, $I_{L(off2)}$, V_{SENSE_TC}, V_{SENSE_VCC}, V_{SENSEH}, $t_{DSENSE1H}$: updated test conditions and values – dK_{LED}/K_{LED}, dK_0/K_0, dK_1/K_1, dK_2/K_2, dK_3/K_3, $t_{D_OL_V}$, I_{SENSEH}: updated values – V_{OUT_MSD}, V_{SENSE_SAT}, I_{SENSE_SAT}, I_{OUT_SAT}, $t_{D_OL_V}$: added rows – I_{SENSE0}, $I_{L(off2)}$, $t_{DSENSE1L}$, $t_{DSENSE2H}$, $\Delta t_{DSENSE2H}$, $t_{DSENSE2L}$, $t_{DSENSE3H}$, $t_{DSENSE3L}$, $t_{DSENSE4H}$, $t_{DSENSE4L}$, $t_{D_CS to TC}$, $t_{D_TC to CS}$, $t_{D_CS to VCC}$, $t_{D_VCC to CS}$, $t_{D_TC to VCC}$, $t_{D_VCC to TC}$: updated test conditions – $t_{D_CS to VSENSEH}$: removed row Updated Figure 6: Switching times and Pulse skew and Figure 8: Multisense timings (chip temperature and VCC sense mode)(VN7050AJ-E only) Removed Figure: Pulse skew Added Figure 9: TDSTKON Table 10: Truth table: – Updated overload conditions Table 11: MultiSense multiplexer addressing: – Added note – Updated Negative output values Updated Section 2.4: Waveforms Added Chapter 3: Protections and Chapter 4: Application information Table 18: PowerSSO-16 mechanical data: – X, Y: updated values

Table 21. Document revision history (continued)

Date	Revision	Changes
16-Apr-2013	3	Table 3: Absolute maximum ratings: – V_{CCPK}: updated parameter – E_{MAX}: updated parameter and value Updated Table 4: Thermal data Table 6: Switching ($V_{CC} = 13\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$, unless otherwise specified): – W_{ON}, W_{OFF}: updated values Table 9: MultiSense ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$): – dK_{cal}/K_{cal}: added row – K_{OL}, K_{LED}, K_0, K_1, K_2, K_3, V_{SENSE_H}: updated values – t_{DSTKON}: updated parameter Removed following tables: Table: Electrical transient requirements (part 1/3) Table: Electrical transient requirements (part 2/3) Table: Electrical transient requirements (part 3/3) Updated Section 4.1.1: Diode (DGND) in the ground line Removed Section: Load dump protection Added Section 4.2: Immunity against transient electrical disturbances Updated Figure 39: Analogue HSD – open-load detection in off-state and Figure 41: GND voltage shift Updated Table 13: Multisense pin levels in off-state Added Section 4.5: Maximum demagnetization energy ($V_{CC} = 16\text{ V}$) Updated Table 14: PCB properties Updated Chapter 5: Package and PCB thermal data and Chapter 6: Package information
27-May-2013	4	Table 3: Absolute maximum ratings: – I_{OUT}: updated value Table 6: Switching ($V_{CC} = 13\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$, unless otherwise specified): – $t_{d(on)}$, W_{ON}, t_{SKEW}: updated values Table 9: MultiSense ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$): – K_1, K_3: updated values
19-Sep-2013	5	Updated disclaimer.
07-Oct-2013	6	Table 6: Switching ($V_{CC} = 13\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$, unless otherwise specified): – $(dV_{OUT}/dt)_{on}$, W_{ON}, W_{OFF}: updated values Table 9: MultiSense ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$): – K_{OL}, K_{LED}, K_0, K_1, K_2, K_3: updated values Added Figure 4: IOUT/ISENSE versus IOUT and Figure 5: Current sense accuracy versus IOUT Added Section 2.5: Electrical characteristics curves Updated Figure 42: Maximum turn off current versus inductance and Figure 51: SO-8 thermal impedance junction ambient single pulse Updated Table 17: Thermal parameters

Table 21. Document revision history (continued)

Date	Revision	Changes
27-May-2014	7	Updated Section 6.2: PowerSSO-16 package information and Section 6.3: SO-8 package information
13-Oct-2014	8	Updated Figure 13: Standby mode activation Updated Table 53: PowerSSO-16 package dimensions

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2014 STMicroelectronics – All rights reserved