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TrueAuto is SMSC's automotive quality process. It has proven its ability to deliver leading-edge quality and services for IC device products to fulfill the needs of the most demanding automotive customers. TrueAuto is a proven total automotive-grade quality approach. TrueAuto IC device robustness begins with SMSC's design for reliability techniques within the silicon IC itself: automotive-grade robustness and testability are designed into the IC. Once available in silicon, the IC is fully-characterized and qualified over a multitude of operating parameters to prove quality under the harshest conditions. In this, SMSC's TrueAuto approach significantly exceeds the usual automotive reliability standards and customer-specific requirements and goes far beyond the stress tests prescribed by the AEC-Q100 specifications. During the fabrication of TrueAuto products, extensive technologies and processes, such as enhanced monitors are used in order to continuously drive improvements in accordance with SMSC's zero Defects per Million (DPM) goals.

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Chapter 1 Overview

1.1 Introduction

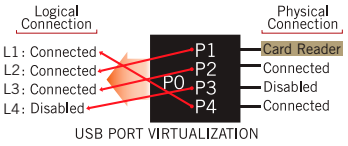
The SMSC Automotive Grade USB 2.0 4-Port Hub is a low-power, OEM configurable, MTT (Multi-Transaction Translator) hub controller IC with 4 downstream ports for embedded USB solutions. The 4-port hub is fully compliant with the USB 2.0 Specification. The USB82514 will attach to an upstream port as a full-speed hub or as a full-/hi-speed hub. The 4-port hub supports low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D- pins and all required pull-down and pull-up resistors on D+ and D- pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

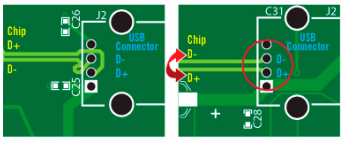
The USB82514 includes over 30 programmable features including:

MultiTRAK™ Technology which utilizes a dedicated TT per port to maintain consistent full-speed data throughput regardless of the number of active downstream connections. MultiTRAK outperforms conventional USB 2.0 hubs with a single TT in USB full-speed data transfers.

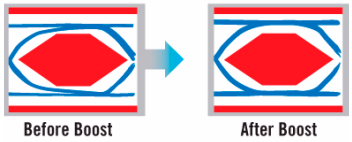
PortMap which provides flexible port mapping and disable sequences. The downstream ports of a USB82514 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB82514 automatically reorders the remaining ports to match the USB host controller's port numbering scheme.



PortSwap which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors avoiding uneven trace length or crossing of the USB differential signals on the PCB.



PHYBoost which enables four programmable levels of USB signal drive strength in downstream port transceivers. PHYBoost attempts to restore USB signal integrity that has been compromised by system level variables such as poor PCB layout, long cables, etc. The boost graphic shows an example of hi-speed USB eye diagrams before (PHYBoost at 0%) and after (PHYBoost at 12%) signal integrity restoration in a compromised system environment.



The USB82514 is specifically tailored for use in automotive applications requiring automotive grade robustness starting with the comprehension of proprietary design for reliability techniques within the silicon IC itself as well as for the package design. Automotive qualified technologies and processes are used to fabricate the products with enhanced monitors to continuously drive improvements in accordance with our zero-dpm methodology. Product qualification is focused on customer expectations and exceeds many of the automotive reliability standards including AEC-Q100.

SMSC automotive services are provided during the life of the product from a dedicated organization composed of operations, quality, and product support personnel specialized in meeting the requirements of the automotive customer.

1.2 OEM Selectable Features

A default configuration is available in the USB82514 following a reset. This configuration may be sufficient for some applications. Strapping option pins make it possible to modify a limited sub-set of the configuration options.

The USB82514 may also be configured by an external EEPROM or a microcontroller. When using the microcontroller interface, the hub appears as an SMBus slave device. If the hub is pin-strapped for external EEPROM configuration but no external EEPROM is present, then a value of '0' will be written to all configuration data bit fields (the hub will attach to the host with all '0' values).

The USB82514 supports several OEM selectable features:

- Optional OEM configuration via I^2C EEPROM or via the industry standard SMBus interface from an external SMBus host or microcontroller, see Table 7.1, "Hub Configuration Options" to configure the serial port interface behavior via the CFG_SEL1 and CFG_SEL0 pins.
- Compound device support (port is permanently hardwired to a downstream USB peripheral device), on a port-by-port basis, see "Register 07h: Configuration Data Byte 2", bit COMPOUND.
- Select Single-Transaction Translator (STT) or Multi-Transaction Translator (MTT), see "Register 06h: Configuration Data Byte 1", bit MTT_ENABLE.
- Select over-current sensing and port power control on an individual (port-by-port) or ganged (all ports together) basis to match the OEM's choice of circuit board component selection, see "Register 06h: Configuration Data Byte 1", bits CURRENT_SNS and PORT_PWR.
- Customize vendor ID, product ID, and device ID, see "Register 00h: Vendor ID (LSB)", "Register 01h: Vendor ID (MSB)", "Register 02h: Product ID (LSB)", "Register 03h: Product ID (MSB)", "Register 04h: Device ID (LSB)" and "Register 05h: Device ID (MSB)".
- Easily configure as a 2, 3 or 4-Port Hub in common PCB layout, see "Register 0Ah: Port Disable for Self-Powered Operation" and "Register 0Bh: Port Disable for Bus-Powered Operation".
- PortMap: Flexible port mapping and disable sequence. Ports can be disabled/reordered in any sequence to support multiple platforms with a single design. The hub will automatically reorder the remaining ports to match the host controller's numbering scheme, see "Register FBh: PortMap 12" and "Register FCh: PortMap 34".
- PortSwap: Programmable USB differential-pair pin location.
  - Eases PCB layout by aligning USB signal lines directly to connectors, see "Register FAh: PortSwap".
- PhyBoost: Programmable USB signal drive strength. Recover USB signal integrity due to compromised system environments using 4 levels of signal drive strength, see "Register F6h: Boost_Up" and "Register F8h: Boost_4:0".
- Configure the delay time for filtering the over-current sense inputs, see "Register 07h: Configuration Data Byte 2", bit OC_TIMER.
- Configure the downstream port power-on time reported to the host, see "Register 10h: Power-On Time".
- Indicate the maximum current that the 4-port hub consumes from the USB upstream port, see "Register 0Eh: Hub Controller Max Current for Self-Powered Operation" and "Register 0Fh: Hub Controller Max Current for Bus-Powered Operation".
- Indicate the maximum current required for the hub controller, see "Register 0Ch: Max Power for Self-Powered Operation" and "Register 0Dh: Max Power for Bus-Powered Operation".
- Support custom string descriptor up to 31 characters in length for:
  - Manufacturer string, see "Register 16h-53h: Manufacturer String".
  - Product string, see "Register 54h-91h: Product String".
  - Serial number string, see "Register 92h-CFh: Serial String".
- Pin selectable options for default configuration:
  - Downstream ports as non-removable ports, see "Register 09h: Non-Removable Device".
  - Downstream ports as disabled ports, see "Register 0Ah: Port Disable for Self-Powered Operation" and "Register 0Bh: Port Disable for Bus-Powered Operation".

Chapter 2 Acronyms

ACRONYM	DESCRIPTION
ACK	Handshake packet indicating a positive acknowledgement
EOF	End of (micro) Frame
EOP	End of Packet
I²C™	Inter-Integrated Circuit[1]
MTT	Multi-Transaction Translator
OCS	Over-current Sense
PCB	Printed Circuit Board
PHY	Physical Layer
PLL	Phase-Locked Loop
QFN	Quad Flat No Leads
RoHS	Restriction of Hazardous Substances directive
SMBus	System Management Bus
STT	Single-Transaction Translator
TT	Transaction Translator

1. I^2C is a trademark of Philips Corporation.

Chapter 3 Pin Configuration

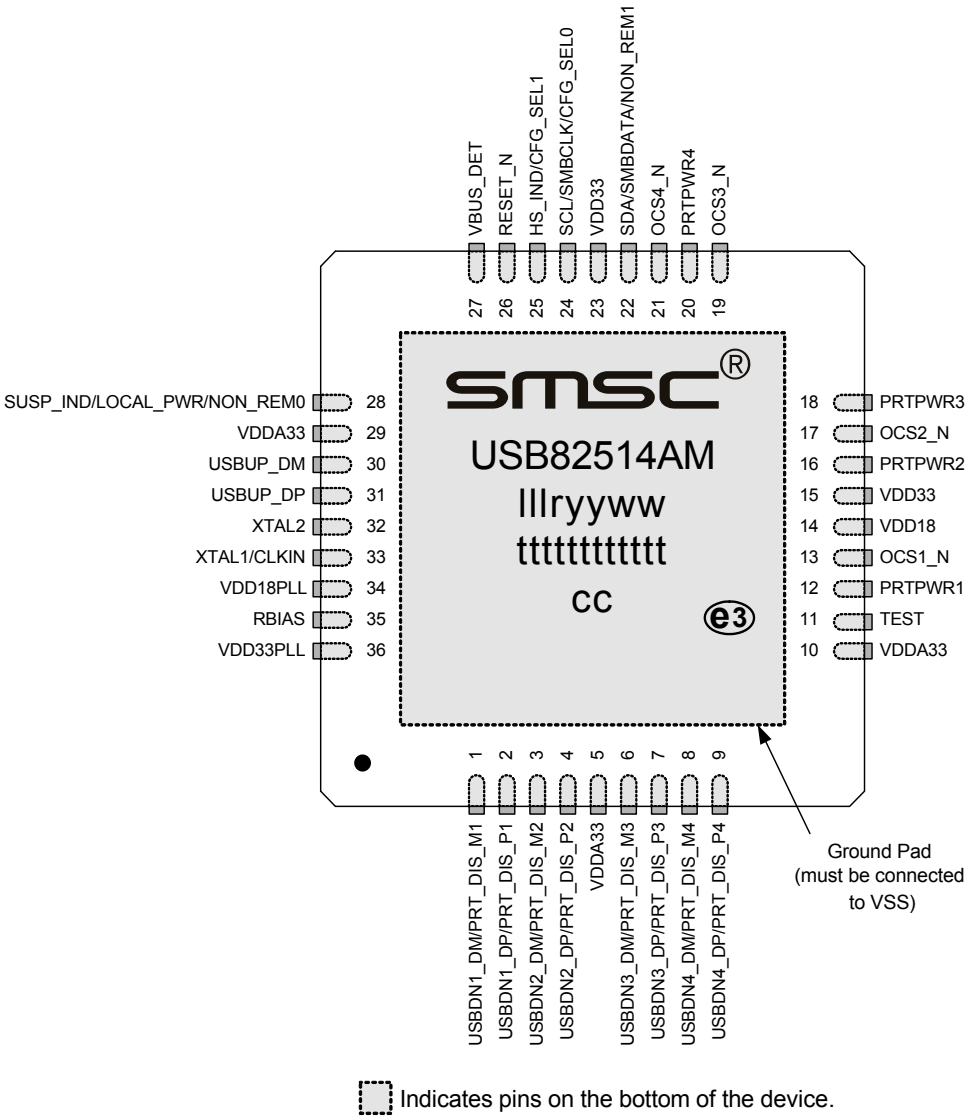


Figure 3.1 USB82514 36-Pin QFN (Top View)

The package designators are:

- lll - Lot Sequence Code
- r - Chip Revision Number
- yy - last two digits of Assembly Year
- ww - Assembly Work Week
- ttttttttttt - Tracking Number (up to 12 characters)
- cc - Country of Original Abbreviation (Optional - up to 2 characters)
- e3 - Pb Free Symbol

Chapter 4 Pin Table

Table 4.1 USB82514 36-Pin Table

UPSTREAM USB INTERFACES (3 PINS)			
USBUP_DP	USBUP_DM	VBUS_DET	
DOWNSTREAM USB 2.0 INTERFACES (17 PINS)			
USBDN1_DP/ PRT_DIS_P1	USBDN2_DP/ PRT_DIS_P2	USBDN3_DP/ PRT_DIS_P3	USBDN4_DP/ PRT_DIS_P4
USBDN1_DM/ PRT_DIS_M1	USBDN2_DM/ PRT_DIS_M2	USBDN3_DM/ PRT_DIS_M3	USBDN4_DM/ PRT_DIS_M4
PRTPWR1	PRTPWR2	PRTPWR3	PRTPWR4
OCS1_N	OCS2_N	OCS3_N	OCS4_N
RBIAS			
SERIAL PORT INTERFACES (3 PINS)			
SDA/ SMBDATA/ NON_REM1	SCL/ SMBCLK/ CFG_SEL0	HS_IND/ CFG_SEL1	
MISC (5 PINS)			
XTAL1/CLKIN	XTAL2	RESET_N	SUSP_IND/ LOCAL_PWR/ NON_REM0
TEST			
ANALOG / DIGITAL POWER (8 PINS)			
(2) VDD33	(3) VDDA33	VDD18	VDD18PLL
VDD33PLL			
TOTAL 36 PINS			

Chapter 5 Block Diagram

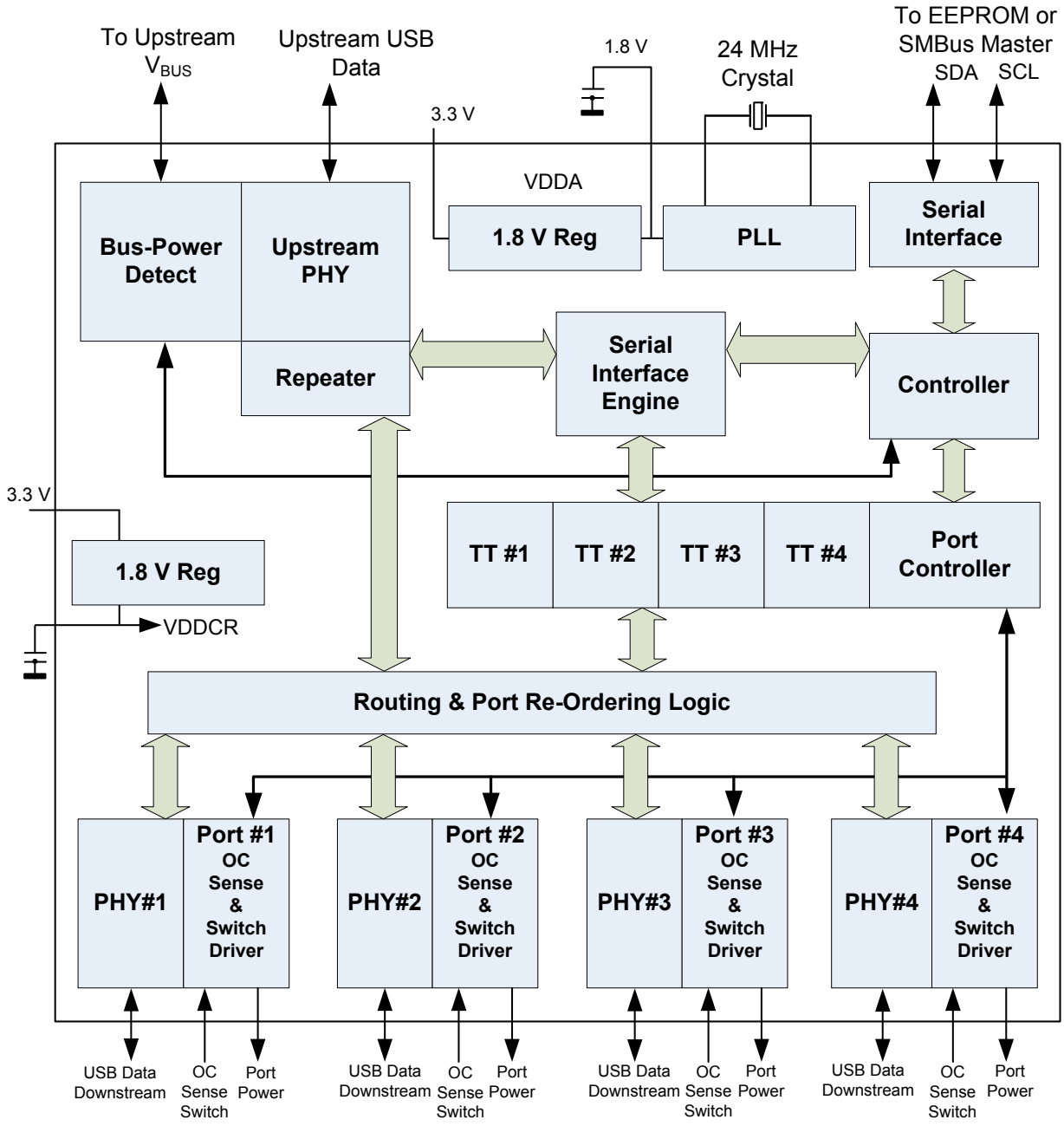


Figure 5.1 USB82514 Block Diagram

Chapter 6 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “N” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “N” is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Table 6.1 USB82514 Pin Descriptions

SYMBOL	36 QFN	BUFFER TYPE	DESCRIPTION
UPSTREAM USB INTERFACES			
USBUP_DP USBUP_DM	31 30	IO-U	USB Bus Data These pins connect to the upstream USB bus data signals (host port or upstream hub).
VBUS_DET	27	I	Detect Upstream VBUS Power Detects state of upstream VBUS power. The SMSC hub monitors VBUS_DET to determine when to assert the internal D+ pull-up resistor (signaling a connect event). When designing a detachable hub, this pin must be connected to the VBUS on the upstream port via a 2 to 1 voltage divider. For self-powered applications with a permanently attached host, this pin must be connected to 3.3 V (typically VDD33).
DOWNSTREAM USB 2.0 INTERFACE			
USBDN[4:1]_DP/ PRT_DIS_P[4:1] &	9 7 4 2	IO-U	Hi-Speed USB Data These pins connect to the downstream USB peripheral devices attached to the hub’s port.
USBDN[4:1]_DM/ PRT_DIS_M[4:1]	8 6 3 1		Downstream Port Disable Strap Option If this strap is enabled by package and configuration settings (see Table 7.1, "Hub Configuration Options"), this pin will be sampled at RESET_N negation to determine if the port is disabled. Both USB data pins for the corresponding port must be tied to the VDDA33 to disable the associated downstream port.
PRTPWR[4:1]	20 18 16 12	O12	USB Port Power Enable Enables power to downstream USB peripheral devices. **Note:** The hub will only support active high power controllers.

Table 6.1 USB82514 Pin Descriptions (continued)

SYMBOL	36 QFN	BUFFER TYPE	DESCRIPTION
OCS_N[4:1]	21 19 17 13	IPU	Over-current Sense Input from external current monitor indicating an over-current condition.
RBIAS	35	I-R	USB Transceiver Bias A 12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.
SERIAL PORT INTERFACE			
SDA/ SMBDATA/ NON_REM1	22	I/OSD12	Serial Data SMB Data NON_REM1: Non-removable port strap option. If this strap is enabled by package and configuration settings (see Table 7.1, "Hub Configuration Options"), this pin will be sampled (in conjunction with SUSP_IND/LOCAL_PWR/NON_REM0) at RESET_N negation to determine if ports [4:1] contain permanently attached (non-removable) devices: NON_REM[1:0] = '00', All ports are removable, NON_REM[1:0] = '01', Port 1 is non-removable, NON_REM[1:0] = '10', Ports 1 & 2 are non-removable, NON_REM[1:0] = '11', Ports 1, 2 & 3 are non-removable.
SCL/ SMBCLK/ CFG_SEL0	24	I/OSD12	Serial Clock (SCL) SMBus Clock (SMBCLK) Configuration Select_SEL0: The logic state of this multifunction pin is internally latched on the rising edge of RESET_N (RESET_N negation) and will determine the hub configuration method as described in Table 7.1, "Hub Configuration Options".

Table 6.1 USB82514 Pin Descriptions (continued)

SYMBOL	36 QFN	BUFFER TYPE	DESCRIPTION
HS_IND/ CFG_SEL1	25	I/O12	Hi-Speed Upstream Port Indicator Configuration Programming Select HS_IND: Hi-Speed Indicator for upstream port connection speed. The active state of HS_IND will be determined as follows: CFG_SEL1 = '0', Configuration Programming Select HS_IND is active high, CFG_SEL1 = '1', HS_IND is active low, 'Asserted' = Hub is connected at HS 'Negated' = Hub is connected at FS **Note:** An LED can be attached to this signal for visual indication.
			CFG_SEL1: The logic state of this pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in Table 7.1, "Hub Configuration Options".
MISC			
XTAL1/ CLKIN	33	ICLKx	Crystal Input/External Clock Input This pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used. When used with an external clock, the signal level must comply with the ICLK buffer levels.
XTAL2	32	OCLKx	Crystal Output 24 MHz Crystal This is the other terminal of the crystal, or it is left disconnected when an external clock source is used to drive XTAL1/CLKIN. **Note:** This output must not be used to drive any external circuitry other than the crystal circuit.
RESET_N	26	IS	RESET Input The system can reset the chip by driving this input low. The minimum active low pulse is 1 µs after all power supply voltages are at nominal levels.

Table 6.1 USB82514 Pin Descriptions (continued)

SYMBOL	36 QFN	BUFFER TYPE	DESCRIPTION
SUSP_IND/ LOCAL_PWR/ NON_REM0	28	I/O12	Active/Suspend Status Signal Indicator or Local-Power & Non-Removable Strap Option Suspend Indicator: Indicates USB state of the hub. 'negated' = Unconfigured, or configured and in USB suspend 'asserted' = Hub is configured, and is active (i.e., not in suspend) **Note:** An LED can be attached to this signal for visual indication.
			Local Power: Detects availability of local self-power source Low = Self/local power source is NOT available (i.e., hub gets all power from Upstream USB VBus). High = Self/local power source is available. NON_REM0 Strap Option: If this strap is enabled by package and configuration settings (see Table 7.1, "Hub Configuration Options"), this pin will be sampled (in conjunction with NON_REM1) at RESET_N negation to determine if ports [4:1] contain permanently attached (non-removable) devices. Also, the active state of the signal will be determined as follows: NON_REM[1:0] = '00', All ports are removable, and the SUSP_IND signal is active high, NON_REM[1:0] = '01', Port 1 is non-removable, and the SUSP_IND signal is active low, NON_REM[1:0] = '10', Ports 1 & 2 are non-removable, and the SUSP_IND signal is active high, NON_REM[1:0] = '11', Ports 1, 2 & 3 are non-removable, and the SUSP_IND signal is active low.
TEST	11	IPD	TEST pin Tie this pin to ground for normal operation.
POWER / GROUND			
VDD18	14		VDD Core +1.8 V core power. This pin must have a 1.0 µF (or greater) ±20% (ESR <0.1 Ω) capacitor to VSS.
VDD33PLL	36		VDD 3.3 PLL Regulator Reference +3.3 V power supply for the PLL.
VDD18PLL	34		VDD PLL +1.8 V Filtered analog power for internal PLL. This pin must have a 1.0 µF (or greater) ±20% (ESR <0.1 Ω) capacitor to VSS.
VDDA33	5 10 29		VDD Analog I/O +3.3 V Filtered analog PHY power, shared between adjacent ports.

Table 6.1 USB82514 Pin Descriptions (continued)

SYMBOL	36 QFN	BUFFER TYPE	DESCRIPTION
VDD33	23 15		VDDIO/VDD 3.3 Core Regulator Reference +3.3 V power supply for the digital I/O. VDD33 acts as the regulator input.
VSS			VSS Ground (The thermal slug must be connected to VSS.)

Table 6.2 USB82514 Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input
IPD	Input with internal weak pull-down resistor
IPU	Input with internal weak pull-up resistor
IS	Input with Schmitt trigger
O12	Output 12 mA
I/O12	Input/Output buffer with 12 mA sink and 12 mA source
I/OSD12	Open drain with Schmitt trigger 12 mA sink. Meets I^2C-Bus specification version 2.1 requirements
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I-R	RBIAS
IO-U	Analog input/output as defined in USB specification

Chapter 7 Configuration Options

7.1 4-Port Hub

SMSC's Automotive Grade USB 2.0 4-Port Hub is fully compliant to the Universal Serial Bus Specification available from the USB Implementer's Forum found at http://www.usb.org/developers/docs/ (Revision 2.0 from April 27, 2000 and the 12/7/2000 and 5/28/2002 Errata). Please refer to Chapter 11 (Hub Specification) for general details regarding hub operation and functionality.

For performance reasons, the 4-Port Hub provides 1 Transaction Translator (TT) per port (defined as Multi-TT configuration), and each TT has 1512 bytes of periodic buffer space and 272 bytes of non-periodic buffer space (divided into 4 non-periodic buffers per TT), for a total of 1784 bytes of buffer space for each Transaction Translator.

7.1.1 Hub Configuration Options

The SMSC hub supports a large number of features (some are mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. There are three principal ways to configure the hub: SMBus, EEPROM, or by internal default settings (with or without pin strapping option overrides). In all cases, the configuration method will be determined by the CFG_SEL1 and CFG_SEL0 pins immediately after RESET_N negation.

If the SMBus or EEPROM is selected using the CFG_SEL pins, then the data read in from the EEPROM/SMBus will take precedence over the pin strapping options. If the internal default setting is selected, the options come from the internal ROM. These values can be selectively overridden using the pin strapping options.

7.1.2 SMBus or EEPROM Interface

Table 7.1 Hub Configuration Options

CFG_SEL1	CFG_SEL0	SMBUS OR EEPROM INTERFACE BEHAVIOR
0	0	Internal default configuration ▪ Strap options enabled ▪ Self-powered operation enabled
0	1	Configured as an SMBus slave for external download of user-defined descriptors. ▪ SMBus slave address 58 (0101100x) ▪ Strap options disabled ▪ All settings controlled by registers
1	0	Internal default configuration ▪ Strap options enabled ▪ Bus power operation
1	1	2-Wire I^2C EEPROMS are supported ▪ Strap options disabled ▪ All settings controlled by registers

7.1.2.1 Power Switching Polarity

The hub will only support active high power controllers.

7.1.3 VBus Detect

According to section 7.2.1 of the USB 2.0 Specification, a downstream port can never provide power to its D+ or D- pull up resistors unless the upstream port's VBUS is in the asserted (powered) state. The VBUS_DET pin on the hub monitors the state of the upstream VBUS signal and will not pull up the D+ resistor if VBUS is not active. If VBUS goes from an active to an inactive state (not powered), the hub will remove power from the D+ pull-up resistor within 10 seconds.

7.2 EEPROM Interface

The SMSC hub can be configured via a 2-wire (I^2C) EEPROM (256x8). (Please see Table 7.1, "Hub Configuration Options" for specific details on how to enable configuration via an I^2C EEPROM).

When configured for EEPROM support, the internal state machine will read the external EEPROM for configuration data. The hub will then "attach" to the upstream USB host.

Note: The hub does not have the capacity to write, or "Program," an external EEPROM. The hub only has the capability to read external EEPROMs. The external EEPROM will be read (even if it is blank or non-populated), and the hub will be "configured" with the values that are read.

Each register has R/W capability. SMBUS and EEPROM Reset Values are 0x00. Reserved registers should be written to '0' unless otherwise specified.

7.2.1 Internal Register Set (Common to EEPROM and SMBus)

REG ADDR	REGISTER NAME	INTERNAL DEFAULT ROM
00h	Vendor ID (LSB)	24h
01h	Vendor ID (MSB)	04h
02h	Product ID (LSB)	14h
03h	Product ID (MSB)	25h
04h	Device ID (LSB)	A0h
05h	Device ID (MSB)	80h
06h	Configuration Data Byte 1	9Bh
07h	Configuration Data Byte 2	20h
08h	Configuration Data Byte 3	02h
09h	Non-Removable Device	00h
0Ah	Port Disable for Self-Powered Operation	00h
0Bh	Port Disable for Bus-Powered Operation	00h
0Ch	Max Power for Self-Powered Operation	01h
0Dh	Max Power for Bus-Powered Operation	32h
0Eh	Hub Controller Max Current for Self-Powered Operation	01h
0Fh	Hub Controller Max Current for Bus-Powered Operation	32h
10h	Power-on Time	32h
11h	Language ID High	00h

REG ADDR	REGISTER NAME	INTERNAL DEFAULT ROM
12h	Language ID Low	00h
13h	Manufacturer String Length	00h
14h	Product String Length	00h
15h	Serial String Length	00h
16h-53h	Manufacturer String	00h
54h-91h	Product String	00h
92h-Cfh	Serial String	00h
D0h-F5h	Reserved	00h
F6h	Boost_Up	00h
F7h	Reserved	00h
F8h	Boost_4:0	00h
F9h	Reserved	00h
FAh	PortSwap	00h
FBh	PortMap 12	00h
FCh	PortMap 34	00h
FDh	Reserved	00h
FFh	Status/Command **Note:**SMBus register only	00h

7.2.1.1 Register 00h: Vendor ID (LSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	VID_LSB	Least Significant Byte of the Vendor ID: This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the OEM using either the SMBus or EEPROM interface options.

7.2.1.2 Register 01h: Vendor ID (MSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	VID_MSB	Most Significant Byte of the Vendor ID: This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the OEM using either the SMBus or EEPROM interface options.

7.2.1.3 Register 02h: Product ID (LSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PID_LSB	Least Significant Byte of the Product ID: This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options.

7.2.1.4 Register 03h: Product ID (MSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PID_MSB	Most Significant Byte of the Product ID: This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options.

7.2.1.5 Register 04h: Device ID (LSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	DID_LSB	Least Significant Byte of the Device ID: This is a 16-bit device release number in BCD format (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options.

7.2.1.6 Register 05h: Device ID (MSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	DID_MSB	Most Significant Byte of the Device ID: This is a 16-bit device release number in BCD format (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options.

7.2.1.7 Register 06h: Configuration Data Byte 1

BIT NUMBER	BIT NAME	DESCRIPTION
7	SELF_BUS_PWR	Self or Bus-Power: Selects between self and bus-powered operation. The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller). When configured as a bus-powered device, the SMSC hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered SMSC hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 specifications are not violated. When configured as a self-powered device, <1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current. This field is set by the OEM using either the SMBus or EEPROM interface options. See description of the DYNAMIC bit (reg 07h, bit 7) for the self-/bus-power functionality when dynamic power switching is enabled. ‘0’ = Bus-powered operation ‘1’ = Self-powered operation **Note:** If dynamic power switching is enabled, this bit is ignored and the LOCAL_PWR pin is used to determine if the hub is operating from self or bus power.
6	Reserved	Reserved
5	HS_DISABLE	Hi-Speed Disable: Disables the capability to attach as either a Hi-/Full-speed device, and forces attachment as Full-speed only (i.e., no Hi-Speed support). ‘0’ = Hi-/Full-Speed ‘1’ = Full-Speed-Only (Hi-Speed is disabled!)
4	MTT_ENABLE	Multi-TT enable: Enables one Transaction Translator per port operation. Selects between a mode where only one Transaction Translator is available for all ports (Single-TT), or each port gets a dedicated Transaction Translator (Multi-TT) {Note: The host may force Single-TT mode only}. ‘0’ = Single TT for all ports ‘1’ = One TT per port (multiple TT’s supported)
3	EOP_DISABLE	EOP Disable: Disables EOP generation of EOF1 when in Full-Speed mode. During FS operation only, this permits the hub to send EOP if no downstream traffic is detected at EOF1. See Section 11.3.1 of the USB 2.0 Specification for additional details. Note: generation of an EOP at the EOF1 point may prevent a host controller (operating in FS mode) from placing the USB bus in suspend. ‘0’ = EOP generation is normal ‘1’ = EOP generation is disabled

BIT NUMBER	BIT NAME	DESCRIPTION
2:1	CURRENT_SNS	Over-current Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs). The ability to support current sensing on a port or ganged basis is hardware implementation dependent. ‘00’ = Ganged sensing (all ports together) ‘01’ = Individual port-by-port ‘1x’ = Over-current sensing not supported (must only be used with bus-powered configurations!)
0	PORT_PWR	Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port-by-port basis (individual). The ability to support power enabling on a port or ganged basis is hardware implementation dependent. ‘0’ = Ganged switching (all ports together) ‘1’ = Individual port-by-port switching

7.2.1.8 Register 07h: Configuration Data Byte 2

BIT NUMBER	BIT NAME	DESCRIPTION
7	DYNAMIC	Dynamic Power Switching Enable: Controls the ability of the hub to automatically change from self-powered operation to bus-powered operation if the local power source is removed or is unavailable (and from bus-powered to self-powered if the local power source is restored). {Note: If the local power source is available, the hub will always switch to self-powered operation.} When dynamic power switching is enabled, the hub detects the availability of a local power source by monitoring the external LOCAL_PWR pin. If the hub detects a change in power source availability, the hub immediately disconnects and removes power from all downstream devices and disconnects the upstream port. The hub will then re-attach to the upstream port as either a bus-powered hub (if local-power is unavailable) or a self-powered hub (if local power is available). ‘0’ = No dynamic auto-switching ‘1’ = Dynamic auto-switching capable
6	Reserved	Reserved
5:4	OC_TIMER	Over-Current Timer: Over-current timer delay ‘00’ = 0.1 ms ‘01’ = 4.0 ms ‘10’ = 8.0 ms ‘11’ = 16.0 ms
3	COMPOUND	Compound Device: Allows the OEM to indicate that the hub is part of a compound device (see the USB Specification for definition) . The applicable port(s) must also be defined as having a "non-removable device". **Note:** When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. ‘0’ = No ‘1’ = Yes, the hub is part of a compound device
2:0	Reserved	Reserved

7.2.1.9 Register 08h: Configuration Data Byte 3

BIT NUMBER	BIT NAME	DESCRIPTION
7:4	Reserved	Reserved
3	PRTMAP_EN	Port Re-mapping Enable: Selects the method used by the hub to assign port numbers and disable ports. ‘0’ = Standard mode ‘1’ = Port re-map mode
2:1	Reserved	Reserved
0	STRING_EN	Enables string descriptor support ‘0’ = String support disabled ‘1’ = String support enabled

7.2.1.10 Register 09h: Non-Removable Device

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	NR_DEVICE	Non-Removable Device: Indicates which port(s) include non-removable devices. ‘0’ = port is removable ‘1’ = port is non-removable Informs the host if one of the active ports has a permanent device that is undetachable from the hub. (Note: The device must provide its own descriptor data.) When using the internal default option, the NON_REM[1:0] pins will designate the appropriate ports as being non-removable. Bit 7 = Reserved Bit 6 = Reserved Bit 5 = Reserved Bit 4 = Controls physical port 4 Bit 3 = Controls physical port 3 Bit 2 = Controls physical port 2 Bit 1 = Controls physical port 1 Bit 0 = Reserved

7.2.1.11 Register 0Ah: Port Disable for Self-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PORT_DIS_SP	Port Disable Self-Powered: Disables 1 or more contiguous ports. ‘0’ = port is available ‘1’ = port is disabled During self-powered operation when remapping mode is disabled (PRTMAP_EN = '0'), this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a host controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB host, and will reorder the active ports in order to ensure proper function. Bit 7 = Reserved Bit 6 = Reserved Bit 5 = Reserved Bit 4 = Controls physical port 4 Bit 3 = Controls physical port 3 Bit 2 = Controls physical port 2 Bit 1 = Controls physical port 1 Bit 0 = Reserved

7.2.1.12 Register 0Bh: Port Disable for Bus-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PORT_DIS_BP	Port Disable Bus-Powered: Disables 1 or more contiguous ports. ‘0’ = port is available ‘1’ = port is disabled During self-Powered operation when remapping mode is disabled (PRTMAP_EN = '0'), this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a host controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB host, and will reorder the active ports in order to ensure proper function. When using the internal default option, the PRT_DIS_P[4:1] and PRT_DIS_M[4:1] pins will disable the appropriate ports. Bit 7 = Reserved Bit 6 = Reserved Bit 5 = Reserved Bit 4 = Controls physical port 4 Bit 3 = Controls physical port 3 Bit 2 = Controls physical port 2 Bit 1 = Controls physical port 1 Bit 0 = Reserved

7.2.1.13 Register 0Ch: Max Power for Self-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	MAX_PWR_SP	Max Power Self_Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors. **Note:** The USB 2.0 Specification does not permit this value to exceed 100 mA.

7.2.1.14 Register 0Dh: Max Power for Bus-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	MAX_PWR_BP	Max Power Bus_Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors.

7.2.1.15 Register 0Eh: Hub Controller Max Current for Self-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	HC_MAX_C_SP	Hub Controller Max Current Self-Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. **Note:** The USB 2.0 Specification does not permit this value to exceed 100 mA. A value of 50 (decimal) indicates 100 mA, which is the default value.

7.2.1.16 Register 0Fh: Hub Controller Max Current for Bus-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	HC_MAX_C_BP	Hub Controller Max Current Bus-Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value will include the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value will NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. A value of 50 (decimal) would indicate 100 mA, which is the default value.

7.2.1.17 Register 10h: Power-On Time

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	POWER_ON_TIME	Power-On Time: The length of time that it takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is stable on that port.

7.2.1.18 Register 11h: Language ID High

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	LANG_ID_H	USB LANGUAGE ID (Upper 8 bits of a 16-bit ID field)

7.2.1.19 Register 12h: Language ID Low

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	LANG_ID_L	USB LANGUAGE ID (Lower 8 bits of a 16-bit ID field)

7.2.1.20 Register 13h: Manufacturer String Length

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	MFR_STR_LEN	Manufacturer String Length Maximum string length is 31 characters.

7.2.1.21 Register 14h: Product String Length

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PRD_STR_LEN	Product String Length Maximum string length is 31 characters.

7.2.1.22 Register 15h: Serial String Length

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	SER_STR_LEN	Serial String Length Maximum string length is 31 characters.

7.2.1.23 Register 16h-53h: Manufacturer String

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	MFR_STR	Manufacturer String, UNICODE UTF-16LE per USB 2.0 Specification Maximum string length is 31 characters (62 bytes). **Note:** The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Some EEPROM programmers may transpose the MSB and LSB, thus reversing the byte order. Please pay careful attention to the byte ordering for your selected programming tools.

7.2.1.24 Register 54h-91h: Product String

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PRD_STR	Product String, UNICODE UTF-16LE per USB 2.0 Specification Maximum string length is 31 characters (62 bytes). **Note:** The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Some EEPROM programmers may transpose the MSB and LSB, thus reversing the byte order. Please pay careful attention to the byte ordering for your selected programming tools.

7.2.1.25 Register 92h-CFh: Serial String

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	SER_STR	Serial String, UNICODE UTF16LE per USB 2.0 Specification Maximum string length is 31 characters (62 bytes). **Note:** The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Some EEPROM programmers may transpose the MSB and LSB, thus reversing the byte order. Please pay careful attention to the byte ordering for your selected programming tools.

7.2.1.26 Register F6h: Boost_Up

BIT NUMBER	BIT NAME	DESCRIPTION
7:2	Reserved	Reserved
1:0	BOOST_IOUT	USB electrical signaling drive strength Boost Bit for Upstream Port. ‘00’ = Normal electrical drive strength = No boost ‘01’ = Elevated electrical drive strength = Low (approximately 4% boost) ‘10’ = Elevated electrical drive strength = Medium (approximately 8% boost) ‘11’ = Elevated electrical drive strength = High (approximately 12% boost) **Note:** “Boost” could result in non-USB Compliant parameters, the OEM should use a ‘00’ value unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.

7.2.1.27 Register F8h: Boost_4:0

BIT NUMBER	BIT NAME	DESCRIPTION
7:6	BOOST_IOUT_4	Upstream USB electrical signaling drive strength Boost Bit for Downstream Port ‘4’. ‘00’ = Normal electrical drive strength = No boost ‘01’ = Elevated electrical drive strength = Low (approximately 4% boost) ‘10’ = Elevated electrical drive strength = Medium (approximately 8% boost) ‘11’ = Elevated electrical drive strength = High (approximately 12% boost) **Note:** “Boost” could result in non-USB Compliant parameters, the OEM should use a ‘00’ value unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.

BIT NUMBER	BIT NAME	DESCRIPTION
5:4	BOOST_IOUT_3	USB electrical signaling drive strength Boost Bit for Downstream Port ‘3’. ‘00’ = Normal electrical drive strength = No boost ‘01’ = Elevated electrical drive strength = Low (approximately 4% boost) ‘10’ = Elevated electrical drive strength = Medium (approximately 8% boost) ‘11’ = Elevated electrical drive strength = High (approximately 12% boost) **Note:** “Boost” could result in non-USB Compliant parameters, the OEM should use a ‘00’ value unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.
3:2	BOOST_IOUT_2	USB electrical signaling drive strength Boost Bit for Downstream Port ‘2’. ‘00’ = Normal electrical drive strength = No boost ‘01’ = Elevated electrical drive strength = Low (approximately 4% boost) ‘10’ = Elevated electrical drive strength = Medium (approximately 8% boost) ‘11’ = Elevated electrical drive strength = High (approximately 12% boost) **Note:** “Boost” could result in non-USB Compliant parameters, the OEM should use a ‘00’ value unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.
1:0	BOOST_IOUT_1	USB electrical signaling drive strength Boost Bit for Downstream Port ‘1’. ‘00’ = Normal electrical drive strength = No boost ‘01’ = Elevated electrical drive strength = Low (approximately 4% boost) ‘10’ = Elevated electrical drive strength = Medium (approximately 8% boost) ‘11’ = Elevated electrical drive strength = High (approximately 12% boost) **Note:** “Boost” could result in non-USB Compliant parameters, the OEM should use a ‘00’ value unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.

7.2.1.28 Register FAh: PortSwap

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PRTSP	PortSwap: Swaps the upstream and downstream USB DP and DM Pins for ease of board routing to devices and connectors. ‘0’ = USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin. ‘1’ = USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin. Bit 7 = Reserved Bit 6 = Reserved Bit 5 = Reserved Bit 4 = ‘1’; Port 4 DP/DM is swapped. Bit 3 = ‘1’; Port 3 DP/DM is swapped. Bit 2 = ‘1’; Port 2 DP/DM is swapped. Bit 1 = ‘1’; Port 1 DP/DM is swapped. Bit 0 = ‘1’; Upstream Port DP/DM is swapped.

7.2.1.29 Register FBh: PortMap 12

<table>
<tr><th>BIT NUMBER</th><th>BIT NAME</th><th>DESCRIPTION</th></tr>
<tr><td>7:0</td><td>PRTR12</td><td>PortMap register for ports 1 & 2

When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number '1' up to the number of ports that the hub recognizes.

The host's port number is referred to as "logical port number" and the physical port on the hub is the “physical port number". When the remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).

Note: The OEM must ensure that contiguous logical port numbers are used, starting from #1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.

Table 7.2 PortMap Register for Ports 1 & 2
<table>
<tr><td>Bit [7:4]</td><td>‘0000’</td><td>Physical Port 2 is disabled</td></tr>
<tr><td></td><td>‘0001’</td><td>Physical Port 2 is mapped to Logical Port 1</td></tr>
<tr><td></td><td>‘0010’</td><td>Physical Port 2 is mapped to Logical Port 2</td></tr>
<tr><td></td><td>‘0011’</td><td>Physical Port 2 is mapped to Logical Port 3</td></tr>
<tr><td></td><td>‘0100’</td><td>Physical Port 2 is mapped to Logical Port 4</td></tr>
<tr><td></td><td>‘0101’ to ‘1111’</td><td>Illegal; Do Not Use</td></tr>
<tr><td>Bit [3:0]</td><td>‘0000’</td><td>Physical Port 1 is disabled</td></tr>
<tr><td></td><td>‘0001’</td><td>Physical Port 1 is mapped to Logical Port 1</td></tr>
<tr><td></td><td>‘0010’</td><td>Physical Port 1 is mapped to Logical Port 2</td></tr>
<tr><td></td><td>‘0011’</td><td>Physical Port 1 is mapped to Logical Port 3</td></tr>
<tr><td></td><td>‘0100’</td><td>Physical Port 1 is mapped to Logical Port 4</td></tr>
<tr><td></td><td>‘0101’ to ‘1111’</td><td>Illegal; Do Not Use</td></tr>
</table>
</td></tr>
</table>

7.2.1.30 Register FCh: PortMap 34

<table>
<tr><th>BIT NUMBER</th><th>BIT NAME</th><th>DESCRIPTION</th></tr>
<tr><td>7:0</td><td>PRTR34</td><td>PortMap register for ports 3 & 4

When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number '1’ up to the number of ports that the hub recognizes.

The host's port number is referred to as "logical port number" and the physical port on the hub is the “physical port number". When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).

Note: The OEM must ensure that contiguous logical port numbers are used, starting from #1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.

Table 7.3 PortMap Register for Ports 3 & 4
<table>
<tr><td rowspan="6">Bit [7:4]</td><td>‘0000’</td><td>Physical Port 4 is disabled</td></tr>
<tr><td>‘0001’</td><td>Physical Port 4 is mapped to Logical Port 1</td></tr>
<tr><td>‘0010’</td><td>Physical Port 4 is mapped to Logical Port 2</td></tr>
<tr><td>‘0011’</td><td>Physical Port 4 is mapped to Logical Port 3</td></tr>
<tr><td>‘0100’</td><td>Physical Port 4 is mapped to Logical Port 4</td></tr>
<tr><td>‘0101 to ‘1111’</td><td>Illegal: Do Not Use</td></tr>
<tr><td>Bit [3:0]</td><td>‘0000’</td><td>Physical Port 3 is disabled</td></tr>
<tr><td></td><td>‘0001’</td><td>Physical Port 3 is mapped to Logical Port 1</td></tr>
<tr><td></td><td>‘0010’</td><td>Physical Port 3 is mapped to Logical Port 2</td></tr>
<tr><td></td><td>‘0011’</td><td>Physical Port 3 is mapped to Logical Port 3</td></tr>
<tr><td></td><td>‘0100’</td><td>Physical Port 3 is mapped to Logical Port 4</td></tr>
<tr><td></td><td>‘0101 to ‘1111’</td><td>Illegal; Do Not Use</td></tr>
</table>
</td></tr>
</table>

7.2.1.31 Register FFh: Status/Command

BIT NUMBER	BIT NAME	DESCRIPTION
7:3	Reserved	Reserved
2	INTF_PW_DN	SMBus Interface Power Down ‘0’ = Interface is active ‘1’ = Interface power down after ACK has completed
1	RESET	Reset the SMBus Interface and internal memory back to RESET_N assertion default settings. ‘0’ = Normal Run/Idle State ‘1’ = Force a reset of registers to their default state
0	USB_ATTACH	USB Attach (and write protect) ‘0’ = SMBus slave interface is active ‘1’ = Hub will signal a USB attach event to an upstream device. The internal memory (address range 00h-FEh) is “write-protected” to prevent unintentional data corruption.

7.2.2 I²C EEPROM

The I²C EEPROM interface implements a subset of the I²C Master Specification (Please refer to the Philips Semiconductor Standard I²C-Bus Specification for details on I²C bus protocols). The hub’s I²C EEPROM interface is designed to attach to a single “dedicated” I²C EEPROM, and conforms to the Standard-mode I²C Specification (100 kbit/s transfer rate and 7-bit addressing) for protocol and electrical compatibility.

Note: Extensions to the I²C Specification are not supported. The hub acts as the master and generates the serial clock SCL, controls the bus access (determines which device acts as the transmitter and which device acts as the receiver), and generates the START and STOP conditions.

7.2.2.1 Implementation Characteristics

The hub will only access an EEPROM using the sequential read protocol.

7.2.2.2 Pull-Up Resistor

The circuit board designer is required to place external pull-up resistors (10 kΩ recommended) on the SDA/SMBDATA/NON_REM1 and SCL/SMBCLK/CFG_SEL0 lines (per SMBus 1.0 Specification, and EEPROM manufacturer guidelines) to VDD in order to assure proper operation.

7.2.2.3 I²C EEPROM Slave Address

Slave address is 1010000.

Note: 10-bit addressing is NOT supported.

7.2.3 In-Circuit EEPROM Programming

The EEPROM can be programmed via ATE (Automatic Test Equipment) by pulling RESET_N low (which tri-states the hub’s EEPROM interface and allows an external source to program the EEPROM).

7.3 SMBus Slave Interface

Instead of loading user-defined descriptor data from an external EEPROM, the SMSC hub can be configured to receive a code load from an external processor via an SMBus interface. The SMBus interface shares the same pins as the EEPROM interface; if CFG_SEL1 & CFG_SEL0 activates the SMBus interface, external EEPROM support is no longer available (and the user-defined descriptor data must be downloaded via the SMBus). The SMSC hub waits indefinitely for the SMBus code load to complete and only “appears” as a newly connected device on USB after the code load is completed. The hub’s SMBus implementation is a *slave-only* SMBus device. The implementation only supports read block and write block protocols. The hub responds to other protocols as described in Section 7.3.2, "Invalid Protocol Response Behavior," on page 35. Reference to the System Management Bus Specification, Rev 1.0.

The SMBus interface is used to read and write the registers in the device. The register set is shown in Section 7.2.1, "Internal Register Set (Common to EEPROM and SMBus)," on page 19.

7.3.1 Bus Protocols

Typical write block and read block protocols are shown below. Register accesses are performed using 7-bit slave addressing, an 8-bit register address field, and an 8-bit data field. The shading indicates the hub driving data on the SMBDATA line; otherwise, host data is on the SDA/SMBDATA/NON_REM1 line.

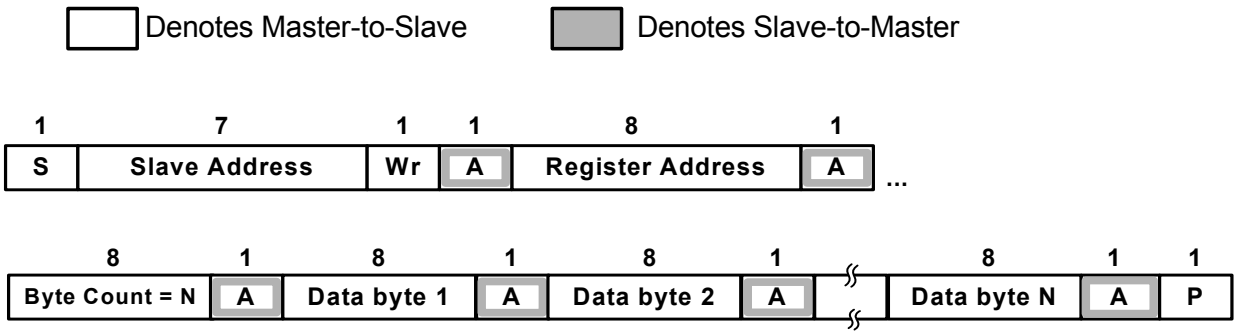
The slave address is the unique SMBus Interface Address for the hub that identifies it on SMBus. The register address field is the internal address of the register to be accessed. The register data field is the data that the host is attempting to write to the register or the contents of the register that the host is attempting to read.

Note: Data bytes are transferred MSB first.

7.3.1.1 Block Read/Write

The block write begins with a slave address and a write condition. After the command code, the host issues a byte count, which describes how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A block read or write is allowed to transfer a maximum of 32 data bytes.

Note: For the following SMBus tables:

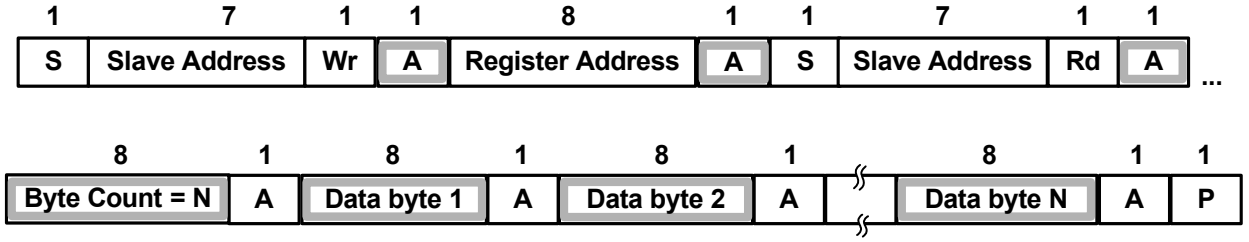


Block Write

Figure 7.1 Block Write

7.3.1.2 Block Read

A block read differs from a block write in that the repeated start condition exists to satisfy the I^2C specification's requirement for a change in the transfer direction.



Block Read

Figure 7.2 Block Read

7.3.2 Invalid Protocol Response Behavior

Registers accessed with an invalid protocol are not updated. A register is only updated following a valid protocol. The only valid protocols are write block and read block, which are described above. The hub only responds to the hardware selected Slave Address (0101100x).

Attempting to communicate with the hub over SMBus with an invalid slave address or invalid protocol results in no response, and the SMBus Slave Interface returns to the idle state.

The only valid registers that are accessible by the SMBus slave address are the registers defined in the Registers Section. The hub does not respond to undefined registers.

7.3.3 General Call Address Response

The hub does not respond to a general call address of 0000_000b.

7.3.4 Slave Device Time-Out

According to the SMBus Specification, version 1.0 devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25 ms ($T_{TIMEOUT, MIN}$). Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than 35 ms ($T_{TIMEOUT, MAX}$).

Note: Some simple devices do not contain a clock low drive circuit; this simple kind of device typically resets its communications port after a start or stop condition. The slave device time-out must be implemented.

7.3.5 Stretching the SCLK Signal

The hub supports stretching of the SCLK by other devices on the SMBus. The hub does not stretch the SCLK.

7.3.6 SMBus/I2C Timing

The SMBus slave interface complies with the SMBus AC Timing Specification.

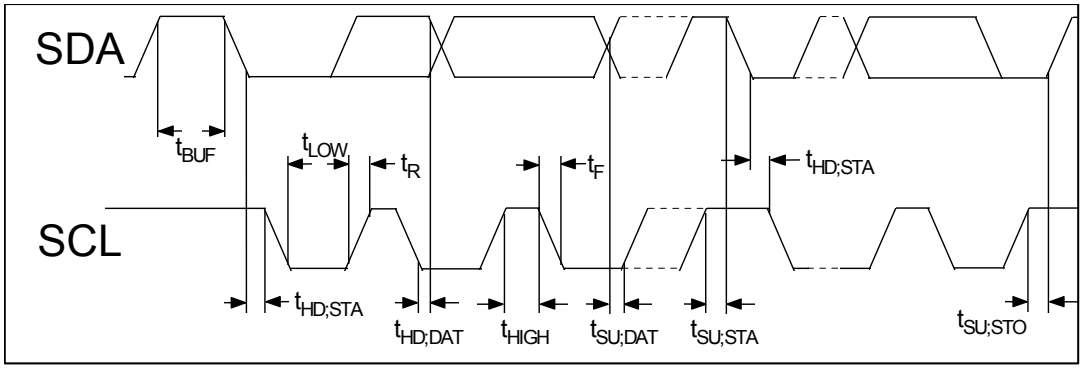


Figure 7.3 SMBus/I2C Timing Parameters

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
fSCL	SCL Clock Frequency	-	-	100	kHz
tBUF	Bus Free Time	4.7	-	-	µs
tSU;STA	START Condition Set-Up Time	4.7	-	-	µs
tHD;STA	START Condition Hold Time	4.0	-	-	µs
tLOW	SCL LOW Time	4.7	-	-	µs
tHIGH	SCL HIGH Time	4.0	-	-	µs
tR	SCL and SDA Rise Time	-	-	1.0	µs
tF	SCL and SDA Fall Time	-	-	0.3	µs
tSU;DAT	Data Set-Up Time	0.25	-	-	µs
tHD;DAT	Data Hold Time	0.25	-	-	µs
tSU;STO	STOP Condition Set-Up Time	4.0	-	-	µs

7.3.7 Bus Reset Sequence

The SMBus slave interface resets and returns to the idle state upon a START field followed immediately by a STOP field.

7.3.7.1 Undefined Registers

The registers shown in Table 7.2 are the defined registers in the hub. Reads to undefined registers return to 00h. Writes to undefined registers have no effect and do not return an error.

7.3.7.2 Reserved Registers

Only a ‘0’ should be written to all reserved registers or bits.

7.4 Default Configuration Option

To configure the hub in its default configuration, strap the CFG_SEL1 to 0 and CFG_SEL0 to 0. This configures the hub to the internal defaults and enables the strapping options. (Please see Section 7.2.1, "Internal Register Set (Common to EEPROM and SMBus)" for the list of the default values.) For specific pin strapping options, please see Chapter 6, Pin Descriptions for instructions on how to modify the default values. Options include port disable and non-removable pin strapping.

7.5 Reset

There are two different resets that the hub experiences. One is a hardware reset via the external RESET_N pin and the second is via the USB Bus Reset.

7.5.1 External Hardware RESET_N

A valid hardware reset is defined as assertion of RESET_N for a minimum of 1µs after all power supplies are within operating range. While reset is asserted, the hub (and its associated external circuitry) consumes less than 500 µA of current from the upstream USB power source.

Assertion of RESET_N (external pin) causes the following:

1. All downstream ports are disabled, and PRTPWR power to downstream devices is removed.
2. The PHYs are disabled, and the differential pairs will be in a high-impedance state.
3. All transactions immediately terminate; no states are saved.
4. All internal registers return to the default state (in most cases, 00(h)).
5. The external crystal oscillator is halted.
6. The PLL is halted.

The hub is “operational” 500 µs after RESET_N is negated. Once operational, the hub configures itself based on the settings of pins CFG_SEL[2:0]. See Table 7.1, “Hub Configuration Options,” on page 18.

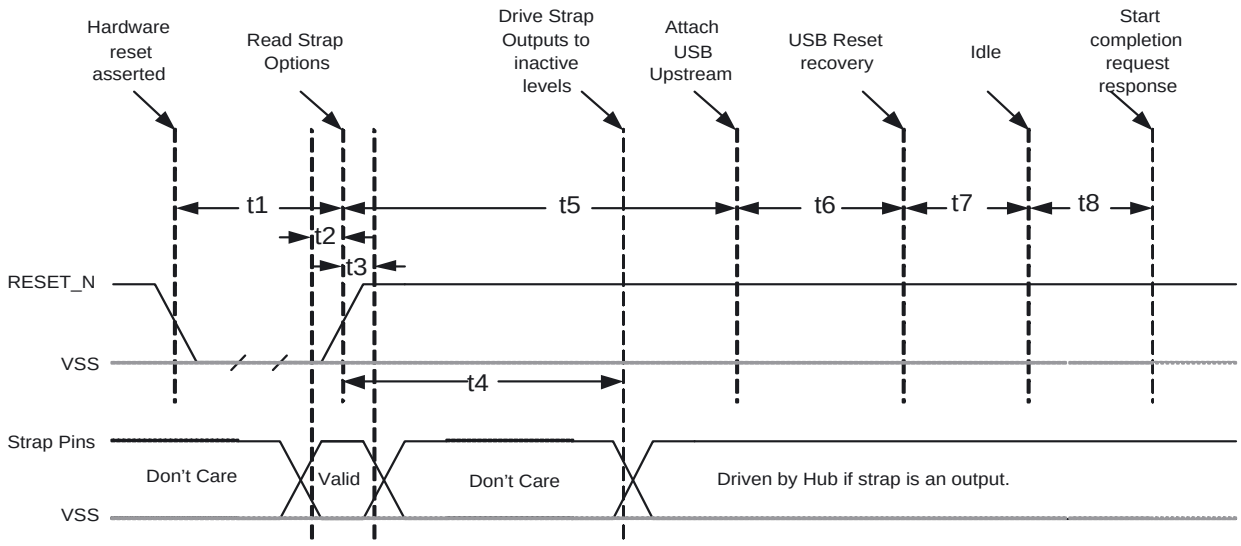


Figure 7.4 Reset_N Timing for Default/Strap Option Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
t1	RESET_N Asserted	1	-	-	µsec
t2	Strap Setup Time	16.7	-	-	nsec
t3	Strap Hold Time	16.7	-	1400	nsec
t4	Hub outputs driven to inactive logic states	-	1.5	2	µsec
t5	USB Attach (see Note 7.1 and Note 7.2)	-	-	100	msec
t6	Host acknowledges attach and signals USB Reset	100	-	-	msec
t7	USB Idle	-	undefined	-	msec
t8	Completion time for requests (with or without data stage)	-	-	5	msec

Note 7.1 In bus-powered mode, the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t1+t5.

Note 7.2 All power supplies must have reached the operating levels mandated in Chapter 8, DC Parameters, prior to (or coincident with) the assertion of RESET_N.

7.5.1.1 RESET_N for EEPROM Configuration

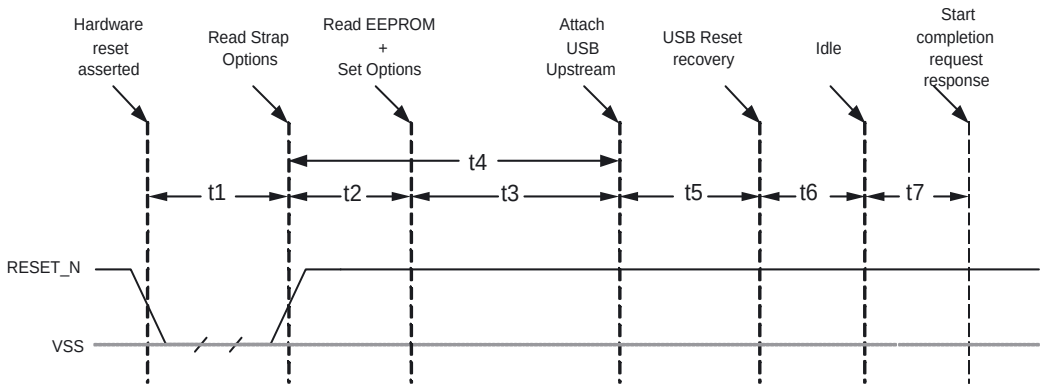


Figure 7.5 Reset_N Timing for EEPROM Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	RESET_N Asserted	1	-	-	µsec
t2	Hub Recovery/Stabilization	-	-	500	µsec
t3	EEPROM Read / Hub Config	-	2.0	99.5	msec
t4	USB Attach (see Note 7.3 and Note 7.4)	-	-	100	msec
t5	Host acknowledges attach and signals USB Reset	100	-	-	msec
t6	USB Idle	-	undefined	-	msec
t7	Completion time for requests (with or without data stage)	-	-	5	msec

Note 7.3 When in bus-powered mode, the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t4+t5+t6+t7.

Note 7.4 All power supplies must have reached the operating levels mandated in Chapter 8, DC Parameters, prior to (or coincident with) the assertion of RESET_N.

7.5.1.2 RESET_N for SMBus Slave Configuration

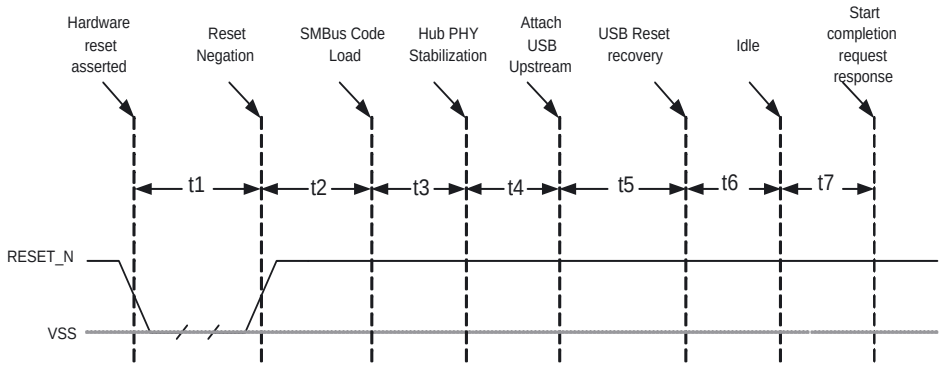


Figure 7.6 Reset_N Timing for SMBus Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	RESET_N Asserted	1	-	-	µsec
t2	Hub Recovery/Stabilization	-	-	500	µsec
t3	SMBus Code Load	-	250	300	msec
t4	Hub Configuration and USB Attach (see Note 7.5 and Note 7.6)	-	-	100	msec
t5	Host acknowledges attach and signals USB Reset	100	-	-	msec
t6	USB Idle	-	Undefined	-	msec
t7	Completion time for requests (with or without data stage)	-	-	5	msec

Note 7.5 For bus-powered configurations the maximum time is 99.5 ms, and the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t2+t3+t4+t5+t6+t7. For Self-Powered configurations, t3 MAX is not applicable and the time to load the configuration is determined by the external SMBus host.

Note 7.6 All power supplies must have reached the operating levels mandated in Chapter 8, DC Parameters, prior to (or coincident with) the assertion of RESET_N.

7.5.2 USB Bus Reset

In response to the upstream port signaling a reset to the hub, the hub does the following:

1. Sets default bus address to ‘0’.
2. Sets configuration to: Unconfigured.
3. Negates PRTPWR[4:1] to all downstream ports.
4. Clears all TT buffers.
5. Moves device from suspended to active (if suspended).
6. Complies with Section 11.10 of the USB 2.0 Specification for behavior after completion of the reset sequence. The host then configures the hub and the hub’s downstream port devices in accordance with the USB Specification.

Note: The hub does not propagate the upstream USB reset to downstream devices.

Chapter 8 DC Parameters

8.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Storage Temperature	T_{STOR}	-55	150	°C	-
3.3 V supply voltage	V_{DDA33}, $V_{DD33PLL}$, V_{DD33}	-	4.0	V	-
Voltage on any I/O pin	-	-0.5	V_{DD33} + 0.3	V	-
Voltage on XTAL1	-	-0.5	3.6	V	-
Voltage on XTAL2	-	-0.5	2.0	V	-

Note 8.1 Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied.

Note 8.2 When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested to use a clamp circuit.

8.2 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
36-pin package Operating Temperature	T_A	-40	85	°C	Ambient temperature in still air. (See Note 8.3)
3.3 V supply voltage	V_{DDA33} $V_{DD33PLL}$ V_{DD33}	3.0	3.6	V	-
3.3 V supply rise time	t_{RT}	-	400	µs	(See Figure 8.1, "Supply Rise Time Models") (See Note 8.4)
Voltage on any I/O pin	-	-0.3	3.6	V	If any 3.3 V supply voltage drops below 3.0 V, then the MAX becomes: (3.3 V supply voltage) + 0.5 V
Voltage on XTAL1	-	-0.3	2.0	V	-
Voltage on XTAL2	-	-0.3	2.0	V	-

Note 8.3 The T_j (junction temperature) must not exceed 125°C.

Note 8.4 The rise time for the 3.3 V supply can be extended to 500 ms max if RESET_N is actively driven low, typically by another IC, until 1 µs after all supplies are within operating range.

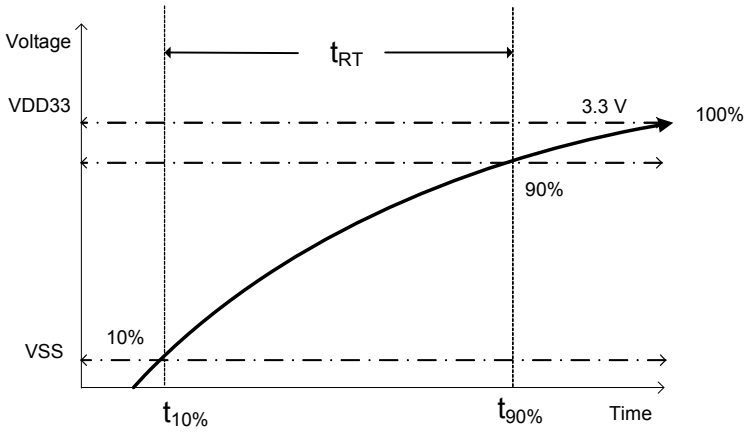


Figure 8.1 Supply Rise Time Models

8.3 Package Thermal Specifications

Table 8.1 36-Pin QFN Package Thermal Parameters

PARAMETER	SYMBOL	VALUE	UNIT	COMMENTS
Thermal Resistance	Θ_{JA}	39	°C/W	Measured from the die to the ambient air.
Junction-to-Top-of-Package	Ψ_{JT}	0.3	°C/W	-

Note 8.5 Thermal parameters are measured or estimated for devices with the exposed pad soldered to thermal vias in a multilayer 2S2P PCB per JESD51.

8.4 DC Electrical Characteristics

Table 8.2 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I, IS Type Input Buffer	-	-	-	-	-	
Low Input Level	V_{ILI}	-	-	0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0	-	-	V	
Input Leakage	I_{IL}	-10	-	+10	µA	V_{IN} = 0 to V_{DD33}
Hysteresis (‘IS’ Only)	V_{HYSI}	250	-	600	mV	
Input Buffer with Pull-Up (IPU)						
Low Input Level	V_{ILI}	-	-	0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0	-	-	V	-
Low Input Leakage	I_{ILL}	+20	-	+110	µA	V_{IN} = 0
High Input Leakage	I_{IHL}	-10	-	+10	µA	V_{IN} = V_{DD33}
IPU Buffer Float Voltage	V_{IPUF}		2.0		V	Voltage at the IPU pin when floated. (Note 8.8)
Input Buffer with Pull-Down (IPD)						
Low Input Level	V_{ILI}	-	-	0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0	-		V	-
Low Input Leakage	I_{ILL}	+10	-	-10	µA	V_{IN} = 0
High Input Leakage	I_{IHL}	-20	-	-100	µA	V_{IN} = V_{DD33}
ICLK Input Buffer						
Low Input Level	V_{ILCK}	-	-	0.5	V	-
High Input Level	V_{IHCK}	1.4	-	-	V	-
Input Leakage	I_{IL}	-10	-	+10	µA	V_{IN} = 0 to V_{DD33}

Table 8.2 DC Electrical Characteristics (continued)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O12, I/O12 & I/OSD12 Type Buffer						
Low Output Level	V_{OL}	-	-	0.4	V	I_{OL} = 12 mA @ V_{DD33} = 3.3 V
High Output Level	V_{OH}	2.4	-	-	V	I_{OH} = -12 mA @ V_{DD33} = 3.3 V
Output Leakage	I_{OL}	-10	-	+10	µA	V_{IN} = 0 to V_{DD33} (Note 8.6)
Hysteresis ('SD' pad only)	V_{HYSC}	250	-	600	mV	
IO-U (Note 8.7)	-	-	-	-	-	-
USB82514						
Supply Current Unconfigured						
Hi-Speed Host Full-Speed Host	$I_{CCINTHS}$ $I_{CCINTFS}$	- -	85 72	100 -	mA mA	No device connected
Supply Current Configured (Hi-Speed Host)						All supplies combined
1 Port @ HS 2 Ports @ HS 3 Ports @ HS 4 Ports @ HS	I_{HCH1} I_{HCH2} I_{HCH3} I_{HCH4}	- - - -	225 255 260 260	- - - 300	mA mA mA mA	 Device connected
Supply Current Configured (Full-Speed Host)						All supplies combined
1 Port @ FS 2 Ports @ FS 3 Ports @ FS 4 Ports @ FS	I_{HCH1} I_{HCH2} I_{HCH3} I_{HCH4}	- - - -	150 160 160 160	- - - -	mA mA mA mA	
Supply Current Suspend	I_{CSBY}	-	325	-	µA	All supplies combined
Supply Current Reset	I_{CRST}	-	115	-	µA	All supplies combined

Note 8.6 Output leakage is measured with the current pins in high impedance.

Note 8.7 See USB 2.0 Specification for USB DC Electrical Characteristics.

Note 8.8 When the IPU type pin is floated, the internal logic will interpret this as logic high. IPU buffer pins include an internal pull up and level shifter. IPU pins float to ~2.0 V with external loads less than 10 µA. This ensures the internal level shifted voltage is above the high level threshold for the internal logic.

8.5 Capacitance

TA = 25°C; fc = 1 MHz; VDD33 = 3.3 V

Table 8.3 Pin Capacitance

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{XTAL}	-	-	2	pF	All pins except USB pins (and pins under test tied to AC ground)
Input Capacitance	C_{IN}	-	-	10	pF	
Output Capacitance	C_{OUT}	-	-	20	pF	

Chapter 9 AC Specifications

9.1 Oscillator/Clock

Crystal: Parallel Resonant, Fundamental Mode, 24 MHz ± 350 ppm.
External Clock: 50% Duty cycle ± 10%, 24 MHz ± 350 ppm, Jitter < 100 ps rms.

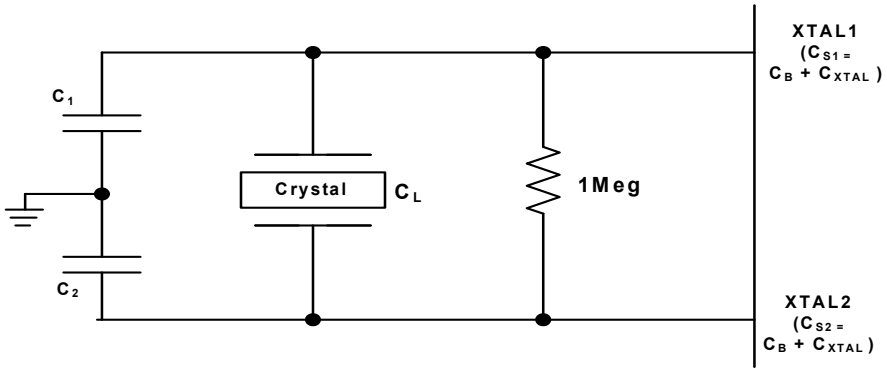


Figure 9.1 Typical Crystal Circuit

Note: C_B equals total board/trace capacitance.

$$C_L = \frac{(C_1 + C_{S1}) \times (C_2 + C_{S2})}{(C_1 + C_{S1} + C_2 + C_{S2})}$$

Figure 9.2 Formula to find value of C_1 and C_2

9.1.1 SMBus Interface

The SMSC hub is designed to meet the specifications as set forth in the SMBus 1.0 Specification for Slave-Only devices (except as noted in Section 7.3, "SMBus Slave Interface").

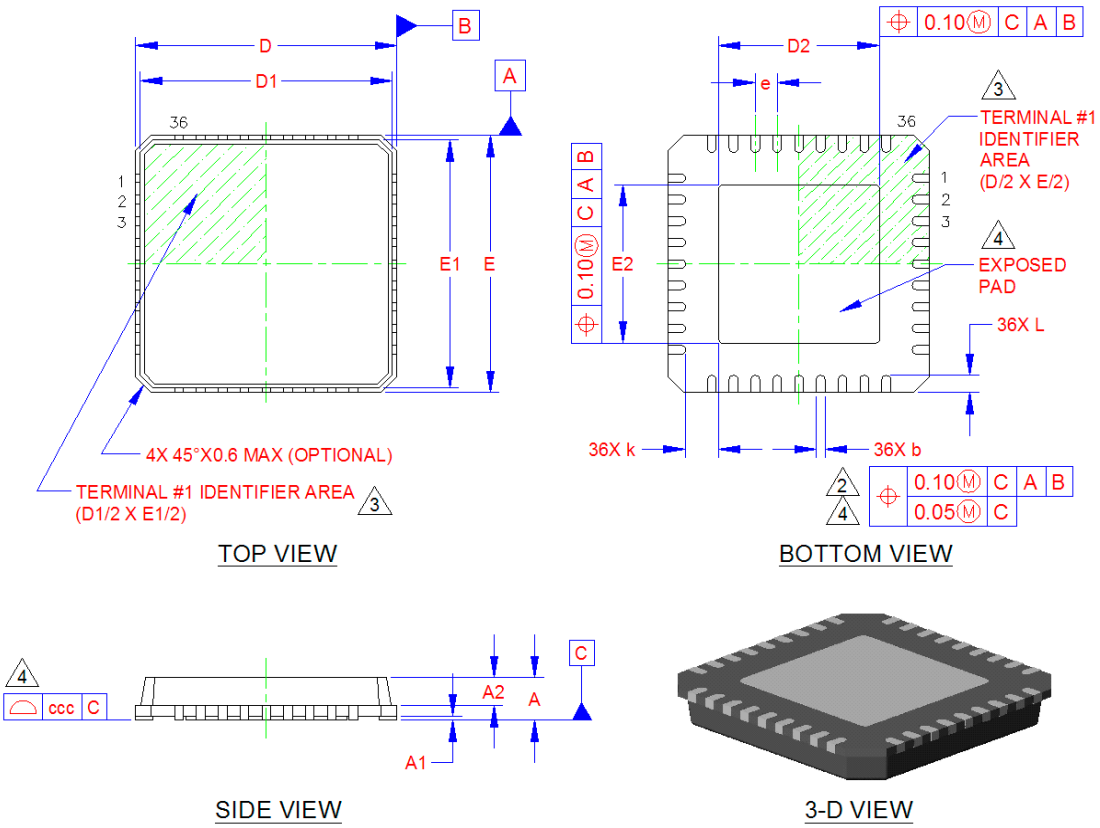
9.1.2 I²C EEPROM

Frequency is fixed at 60 kHz ± 20%.

9.1.3 USB 2.0

The SMSC hub is designed to comply with the USB 2.0 Specification (Revision 2.0 from April 27, 2000 and the 12/7/2000 and 5/28/2002 Errata). Please refer to the USB 2.0 Specification for more information.

Chapter 10 Package Outline



COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.70	-	1.00	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A2	-	-	0.90	-	MOLD CAP THICKNESS
D/E	5.85	6.00	6.15	-	X/Y BODY SIZE
D1/E1	5.55	-	5.95	-	X/Y MOLD CAP SIZE
D2/E2	3.60	3.70	3.80	4	X/Y EXPOSED PAD SIZE
L	0.30	0.40	0.50	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
k	0.52	-	-	-	TERMINAL TO ePAD CLEARANCE
ccc	-	-	0.08	4	COPLANARITY
e	0.50 BSC			-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.
4. COPLANARITY ZONE APPLIES TO EXPOSED PAD AND TERMINALS.

Figure 10.1 36-Pin QFN, 6x6 mm^2 Body, 0.5 mm Pitch

Chapter 11 Revision History

Table 11.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.1 (11-18-11)	Section 8.4, "DC Electrical Characteristics"	V_{IPUF} (IPU Buffer Float Voltage) added in Table 8.2.
Rev. 1.1 (11-17-11)	Chapter 3, Pin Configuration	Figure 3.1 improved:
Rev. 1.1 (11-09-11)	Chapter 3, Pin Configuration	Topmark information added in Figure 3.1. Package designators described.
	Section 8.2, "Operating Conditions"	Max value corrected for 'voltage on any I/O pin': 3.6 V
	Section 8.5, "Capacitance"	VDD18, VDDPLL 0 1.8 V replaced by VDD33 = 3.3 V
Rev. 1.1 (07-19-11)	Section 8.2, "Operating Conditions"	In the table: Added Note 8.4 under Note 8.3. Added reference to Note 8.4 in the comments column for 3.3 V rise time parameter.
Rev. 1.1 (05-30-11)	Chapter 6, Pin Descriptions	VBUS_DET is an input. Buffer type changed from "I/O12" to "I".
Rev. 1.1 (05-04-11)	Section 8.2, "Operating Conditions"	Max value corrected for XTAL1 and XTAL2: 2.0 V
Rev. 1.1 (03-21-11)	Chapter 6, Pin Descriptions	The internal regulator cannot be turned off.
	Section 8.1, "Maximum Guaranteed Ratings"	The chip does not have an external 1.8 V supply. Max value of 3.3 V supply voltages changed from 4.6 V to 4.0 V.
	Section 8.2, "Operating Conditions"	The chip does not have an external 1.8 V supply.
Rev. 1.0 (10-19-10)	Section 8.1, "Maximum Guaranteed Ratings"	Max value corrected for 'voltage on any I/O pin': 5.5 -> V_{DD33} + 0.3
Rev. 1.0 (10-12-10)	Page 2	Order information completed.
Rev. 1.0 (09-02-09)	Section 8.3, "Package Thermal Specifications"	TBD values have been specified.
Rev. 0.8 (08-28-09)	Section 8.4, "DC Electrical Characteristics"	TBD values have been specified.
Rev. 0.7 (03-13-09)	All	Confidential designation removed from document.
Rev. 0.7 (12-01-08)	Initial Release	

Chapter 12 Further Information

For more information on SMSC automotive products, including integrated circuits, software, and MOST® development tools and modules, visit our web site: http://www.smsc-ais.com. Direct contact information is available at: http://www.smsc-ais.com/offices.

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