1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±20V
Operating Ambient Temperature, T_A	–55°C to +150°C
Storage Temperature, T_S	–55°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	–100	—	—	V	V_{GS} = 0V, I_D = –2 mA
Gate Threshold Voltage	$V_{GS(th)}$	–1	—	–2.4	V	V_{GS} = V_{DS}, I_D = –1 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	5	mV/°C	V_{GS} = V_{DS}, I_D = –1 mA (Note 1)
Gate Body Leakage Current	I_{GSS}	—	—	–100	nA	V_{GS} = ± 20V, V_{DS} = 0V
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	–10	µA	V_{GS} = 0V, V_{DS} = Maximum rating
		—	—	–1	mA	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (Note 1)
On-State Drain Current	$I_{D(ON)}$	–0.4	–0.6	—	A	V_{GS} = –5V, V_{DS} = –25V
		–1.5	–2.5	—	A	V_{GS} = –10V, V_{DS} = –25V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	5	7	Ω	V_{GS} = –5V, I_D = –250 mA
		—	2	3.5	Ω	V_{GS} = –10V, I_D = –750 mA
		—	—	1.7	%/°C	V_{GS} = –10V, I_D = –750 mA
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	–100	—	—	V	V_{GS} = 0V, I_D = –2 mA (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G_{FS}	300	360	—	mmho	V_{DS} = –25V, I_D = –750 mA
Input Capacitance	C_{ISS}	—	80	125	pF	V_{GS} = 0V, V_{DS} = –25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	40	70	pF	
Reverse Transfer Capacitance	C_{RSS}	—	10	25	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	—	10	ns	V_{DD} = –25V, I_D = –1A, R_{GEN} = 25Ω
Rise Time	t_r	—	—	15	ns	
Turn-Off Delay Time	$t_{d(OFF)}$	—	—	20	ns	
Fall Time	t_f	—	—	15	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	–1.8	V	V_{GS} = 0V, I_{SD} = –1A (Note 1)
Reverse Recovery Time	t_{rr}	—	300	—	ns	V_{GS} = 0V, I_{SD} = –1A

Note 1: Unless otherwise stated, all DC parameters are 100% tested at 25°C. Pulse test: 300 µs pulse, 2% duty cycle

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–55	—	+150	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
3-lead SOT-89	θ_{JA}	—	133	—	°C/W	

THERMAL CHARACTERISTICS

Package	I_D (Note 1) (Continuous) (mA)	I_D (Pulsed) (A)	Power Dissipation at T_A = 25°C (Note 2) (W)	I_{DR} (Note 1) (mA)	I_{DRM} (A)
3-lead SOT-89	–480	–2.5	1.6	–480	–2.5

Note 1: I_D (continuous) is limited by maximum rated T_J.

2: Mounted on an FR5 board, 25 mm x 25 mm x 1.57 mm

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

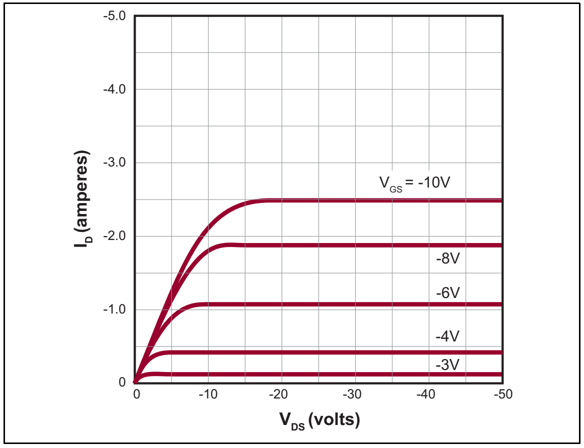


FIGURE 2-1: *Output Characteristics.*

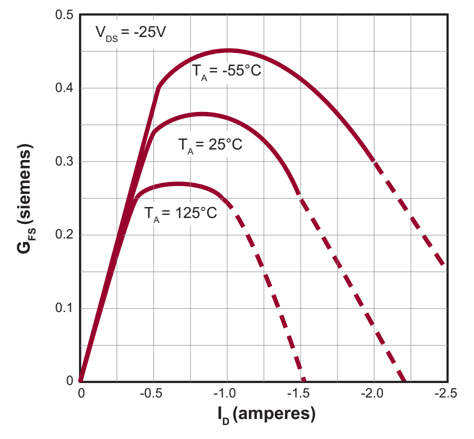


FIGURE 2-2: *Transconductance vs. Drain Current.*

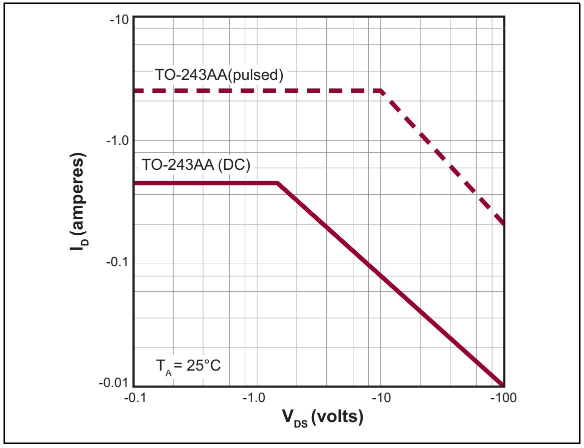


FIGURE 2-3: *Maximum Rated Safe Operating Area.*

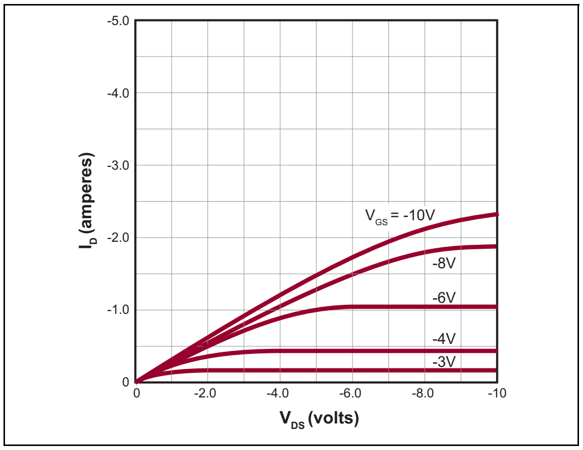


FIGURE 2-4: *Saturation Characteristics.*

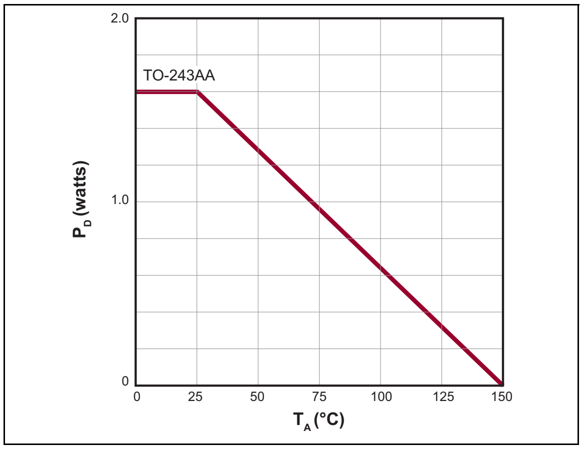


FIGURE 2-5: *Power Dissipation vs. Ambient Temperature.*

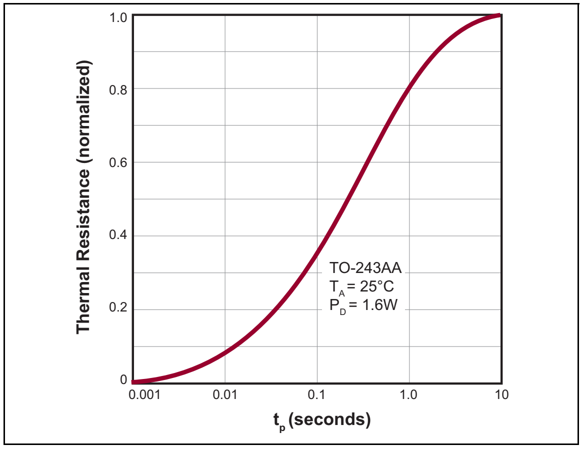


FIGURE 2-6: *Thermal Response Characteristics.*

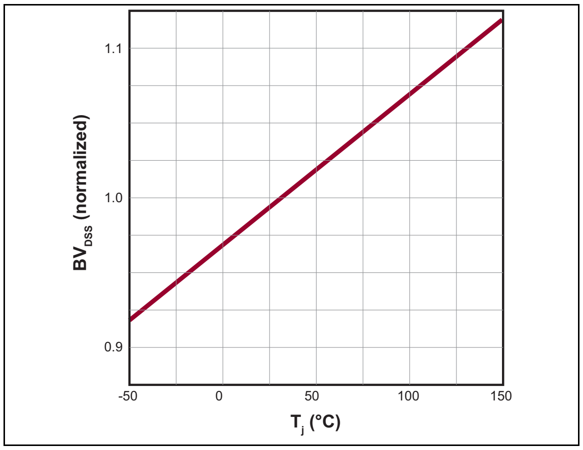


FIGURE 2-7: *BV$_{DSS}$ Variation with Temperature.*

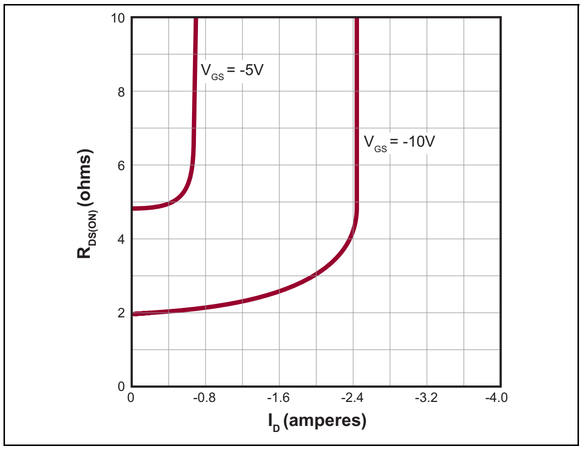


FIGURE 2-10: *On-Resistance vs. Drain Current.*

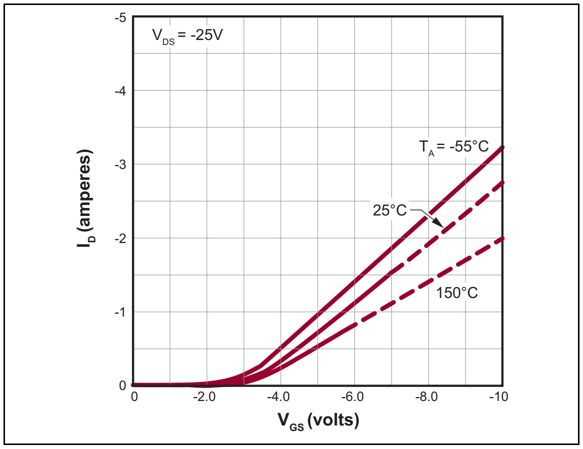


FIGURE 2-8: *Transfer Characteristics.*

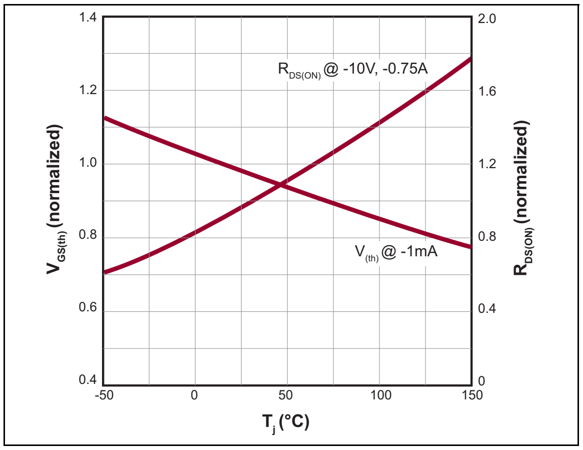


FIGURE 2-11: *V$_{GS(th)}$ and R$_{DS}$ Variation with Temperature.*

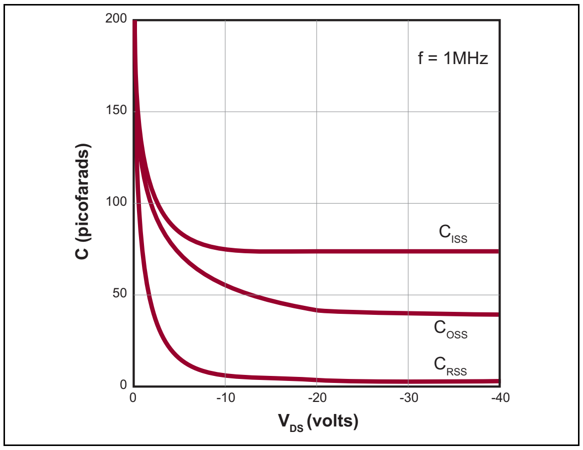


FIGURE 2-9: *Capacitance vs. Drain-to-Source Voltage.*

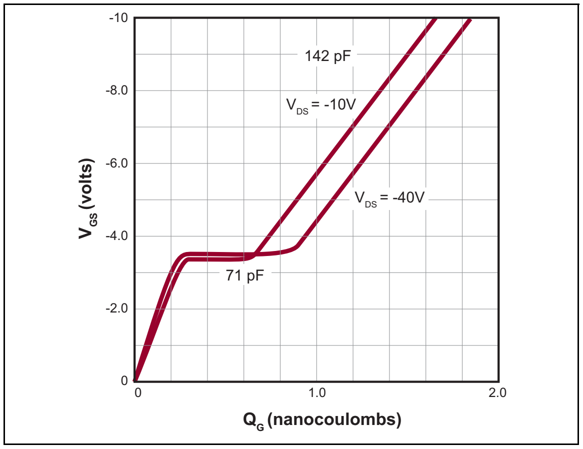


FIGURE 2-12: *Gate Drive Dynamic Characteristics.*

3.0 PIN DESCRIPTION

The details on the pins of TP2510 are listed in Table 3-1. Refer to **Package Type** for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2,4	Drain	Drain
3	Source	Source

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for TP2510.

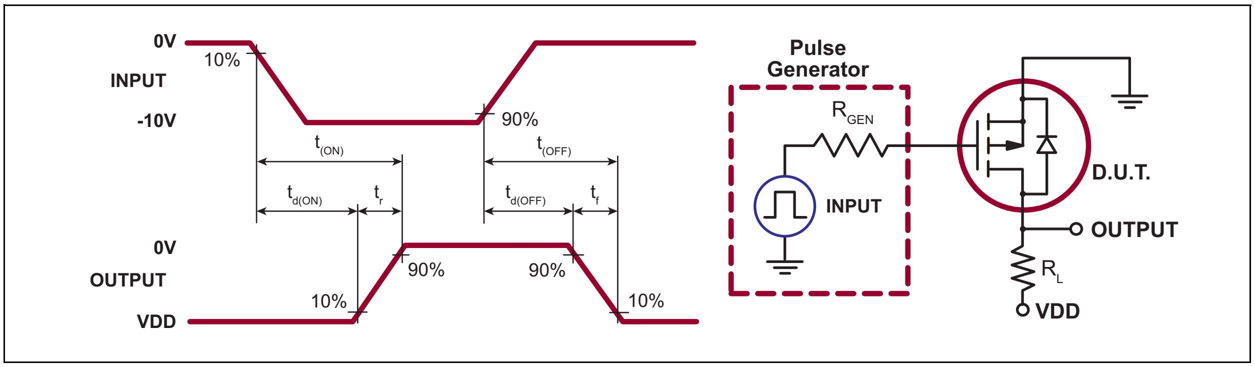


FIGURE 4-1: *Switching Waveforms and Test Circuit.*

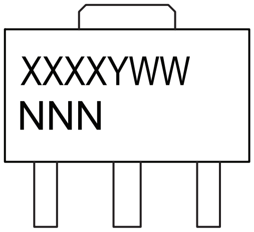
TABLE 4-1: PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$V_{GS(TH)}$ (Maximum) (V)	$I_{D(ON)}$ (Minimum) (A)
–100	3.5	–2.4	–1.5

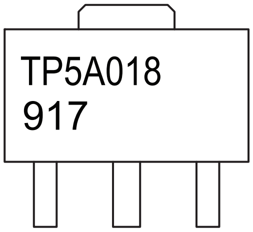
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

3-lead SOT-89



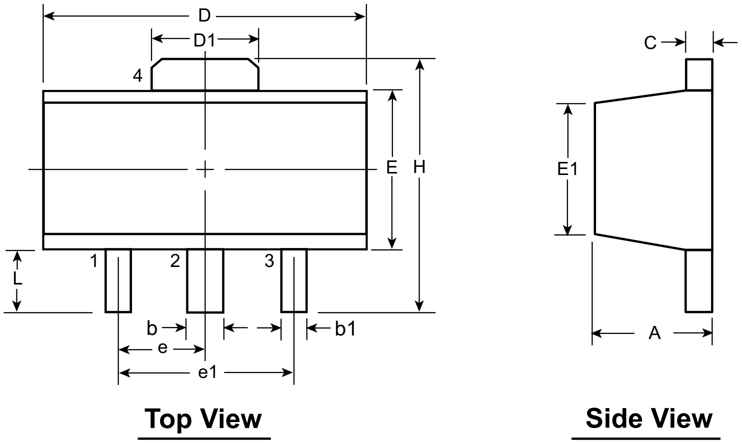
Example



Legend:		
	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Top View

Side View

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00†	1.50 BSC	3.00 BSC	3.94	0.73†
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.
† This dimension differs from the JEDEC drawing
Drawings not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (June 2020)

- Converted Supertex Doc# DSFP-TP2510 to Microchip DS20005965A
- Added a pin function table
- Changed the package marking format
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	**XX**	**-**	**X**	**-**	**X**
Device	**Package Options**		**Environmental**		**Media Type**

Device: TP2510 = P-Channel Enhancement-Mode Vertical DMOS FET

Package: N8 = 3-lead SOT-89

Environmental: G = Lead (Pb)-free/RoHS-compliant Package

Media Type: (blank) = 2000/Reel for an N8 Package

Example:

a) TP2510N8-G:	P-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead SOT-89, 2000/Reel

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