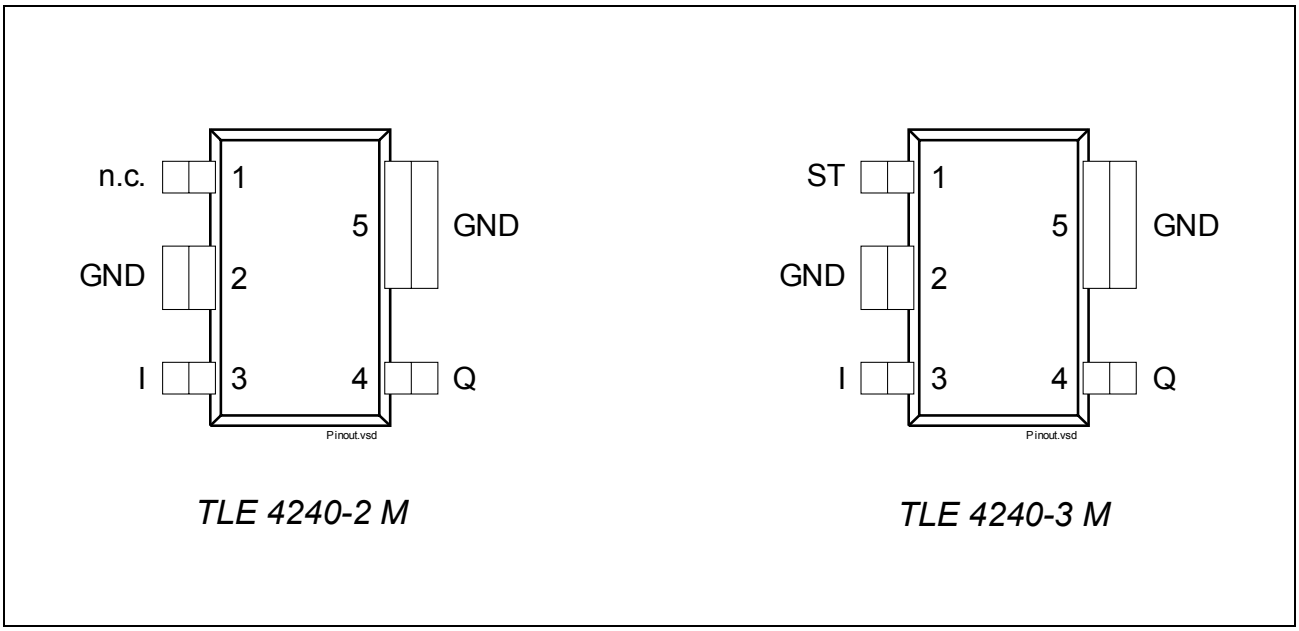


Figure 1 **Pin Configuration** (top view)

Table 1 **Pin Definitions and Functions**

Pin No.	Symbol	Function
1	n.c.	*Version TLE 4240-2 M only:* **Internally not connected.**
1	ST	*Version TLE 4240-3 M only:* **Status output;** open collector output. Low level indicates open load. Connect to a positive voltage rail with an external pull-up resistor. Leave open, if not needed.
2	GND	**Ground;** connect to heatsink area. Interconnect with pin 5.
3	I	**Input;** IC supply
4	Q	**Output;**
5	GND	**Ground;** connect to heatsink area. Interconnect with pin 2.

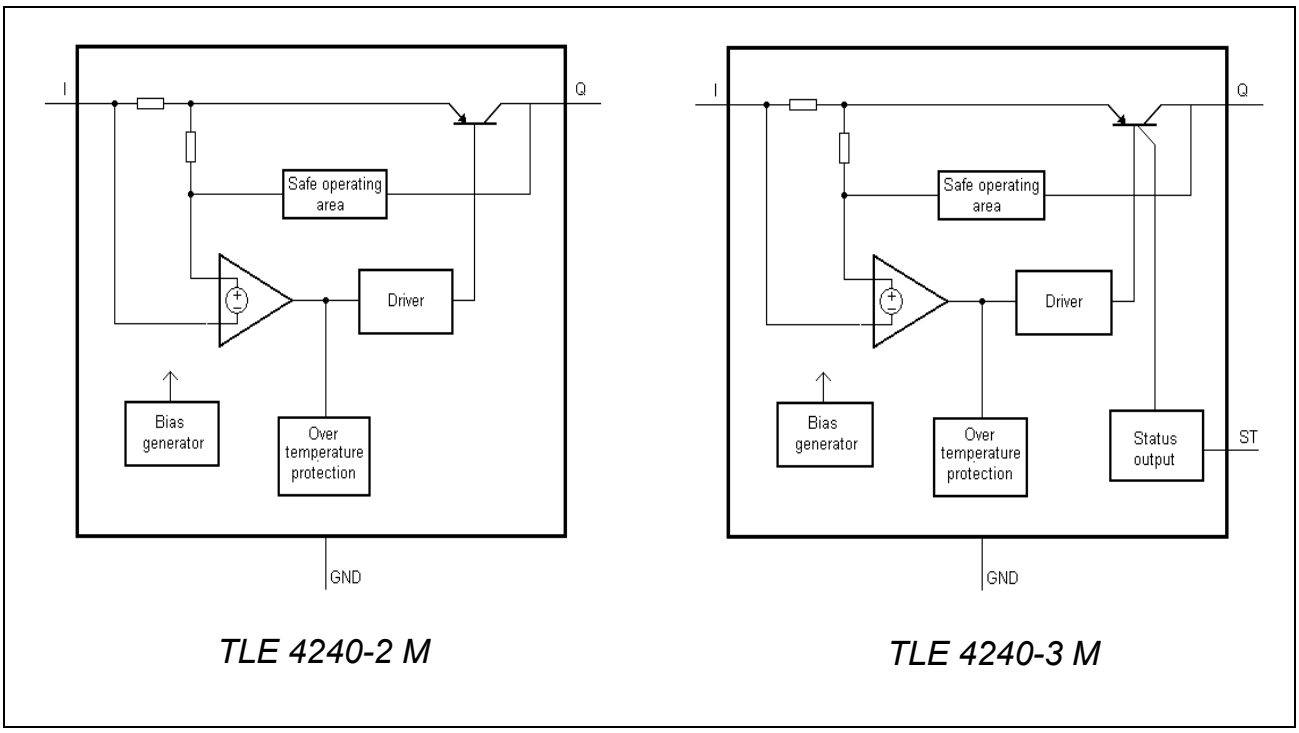


Figure 2 Block Diagram

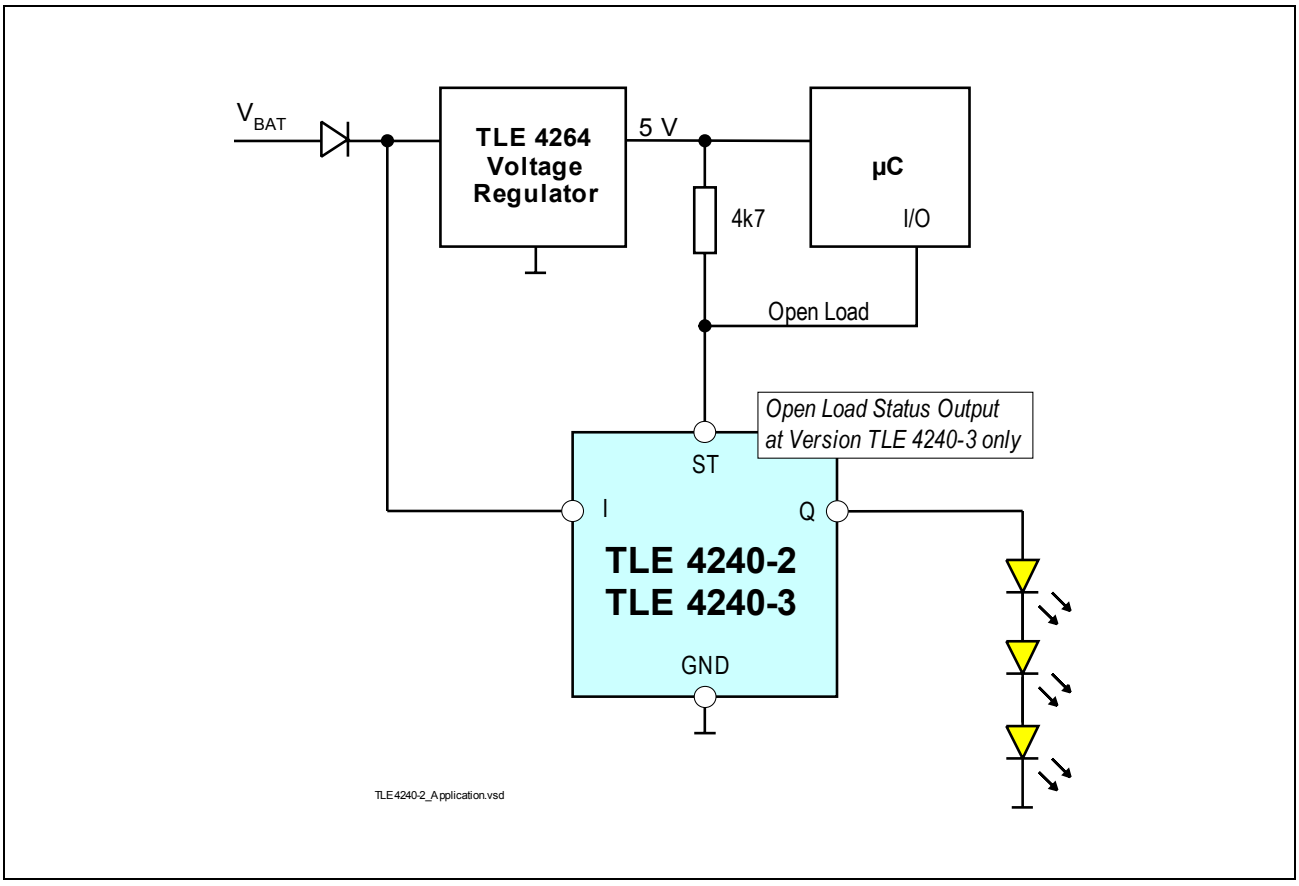


Figure 3 Typical Application Circuit

Table 2 Absolute Maximum Ratings

-40 °C ≤ T_j ≤ 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input I					
Voltage	V_I	-16	45	V	–
Current	I_I	–	–	mA	internally limited
Output Q					
Voltage	V_Q	-1	40	V	–
Current	I_Q	–	–	mA	internally limited
Status ST *(TLE 4240-3 M)*					
Voltage	V_{ST}	-0.3	12	V	–
Current	I_{ST}	–	–	mA	internally limited
ESD Susceptibility					
ESD Resistivity	$V_{ESD,HBM}$	4	–	kV	TLE 4240-2 M; HBM [1]
	$V_{ESD,CDM}$	2	–	kV	TLE 4240-2 M; CDM [2]
ESD Resistivity	$V_{ESD,HBM}$	2	–	kV	TLE 4240-3 M; HBM [1]
	$V_{ESD,CDM}$	2	–	kV	TLE 4240-3 M; CDM [2]
Temperatures					
Junction temperature	T_j	-40	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–

1) ESD susceptibility “human body model (HBM)” according to JESD22-A114.

2) ESD susceptibility “charged device model (CDM)” according to JESD22-C101

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

Table 3 Functional Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input voltage	V_I	3	45	V	–
Status output voltage *(Version TLE 4240-3 M only)*	V_{ST}	–	15	V	–
Junction temperature	T_j	-40	150	°C	–

Table 4 Thermal Resistance

Parameter	Symbol	Typ. Limit Values	Unit	Remarks
Junction ambient	$R_{th,j-a}$	179	K/W	A: footprint only[1)]
		99	K/W	A = 300 mm [1)]
		87	K/W	A = 600 mm [1)]
Junction pin 5	$R_{th,j-pin5}$	26	K/W	measured to pin 5

1) Mounted an a PCB 80 × 80 × 1.5 mm^3, horizontal position, zero airflow.

Table 5 Electrical Characteristics

V_I = 13.5 V; V_Q = 6 V; -40 °C ≤ T_j ≤ 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Regulator:						
Output current	I_Q	51	57	63	mA	T_j = 100 °C
		46	58	70	mA	9 V ≤ V_I ≤ 16 V T_j ≤ 125 °C
Dropout voltage V_{dr} = V_I - V_Q	V_{dr}	–	0.5	0.7	V	I_Q = 40 mA

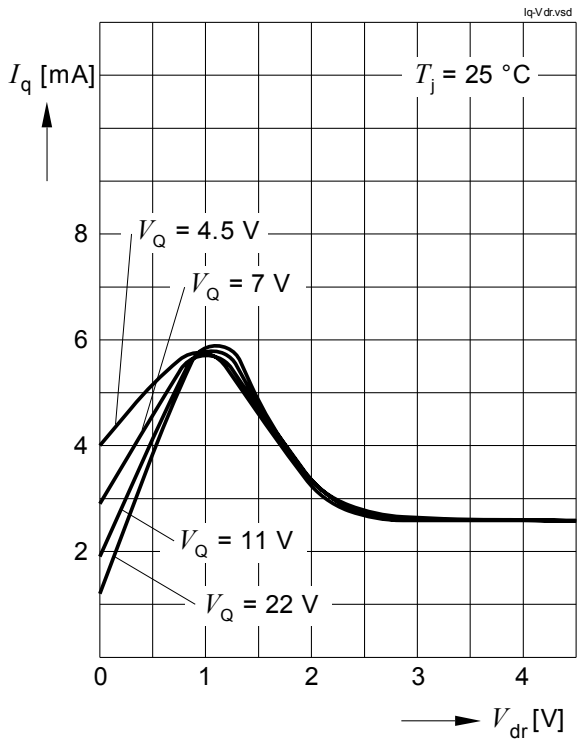
Table 5 Electrical Characteristics (cont'd)

V_I = 13.5 V; V_Q = 6 V; -40 °C ≤ T_j ≤ 150 °C; unless otherwise specified

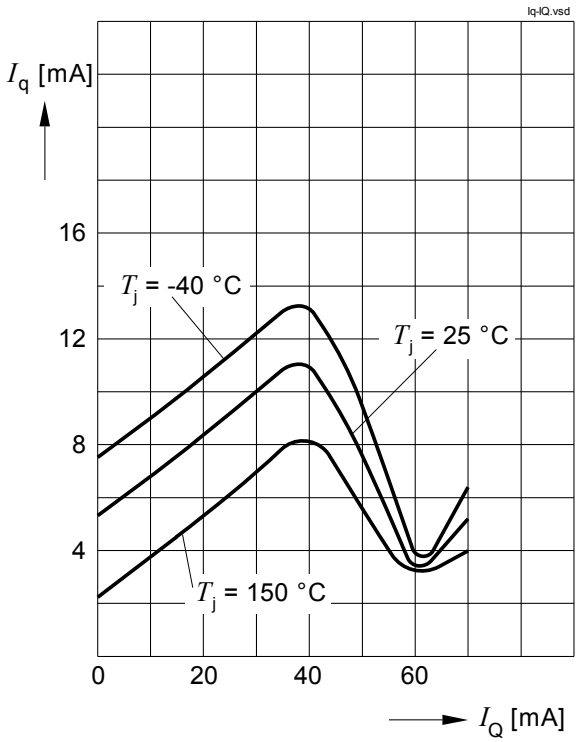
Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Reverse output current	I_Q	-5	–	–	mA	V_I = -16 V V_Q = 0 V
		-5	–	–	mA	V_I = 0 V V_Q = 16 V
Current consumption $I_q = I_I - I_Q$	I_q	–	7	10	mA	V_{dr} = 1 V
Current consumption open load *Version TLE 4240-3 M*	I_q	–	30	40	mA	I_Q = 0 mA
Open Load Detection *(Version TLE 4240-3 M only)*:						
Lower status switching threshold $V_{IQ,L} = V_I - V_Q$	$V_{IQ,L}$	–	–	0.8	V	Ramping down (V_I - V_Q)
Status Output ST *(Version TLE 4240-3 M only)*:						
Status low voltage	$V_{ST,low}$	–	–	0.4	V	I_{ST} = 1 mA I_Q = 5 mA
Status sink current limitation	$I_{ST,MAX}$	1.5	–	–	mA	V_{ST} = 1 V
Status leakage current	$I_{ST,high}$	–	–	2	µA	V_{ST} = 5 V (V_I - V_Q) > 1 V

Typical Performance Characteristics

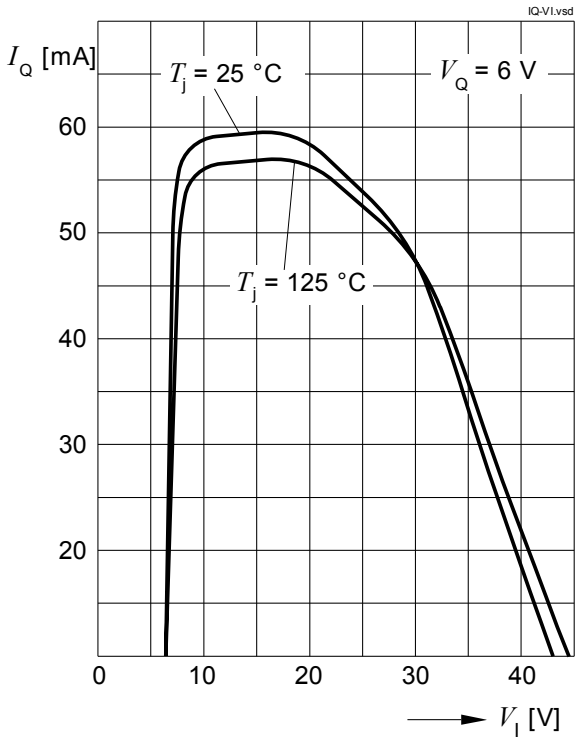
Current Consumption I_q vs. Drop Voltage $V_{dr} = (V_I - V_Q)$



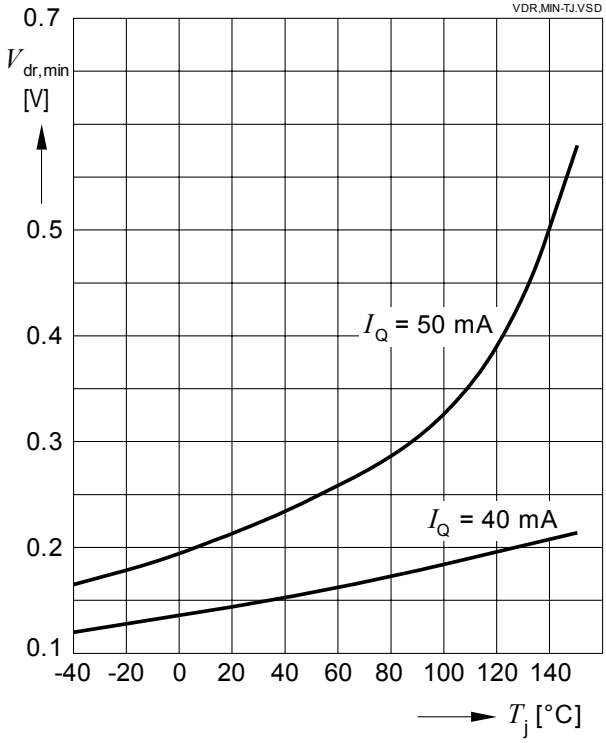
Current Consumption I_q vs. Output Current I_Q



Output Current I_Q vs. Input Voltage V_I; V_Q = 6 V

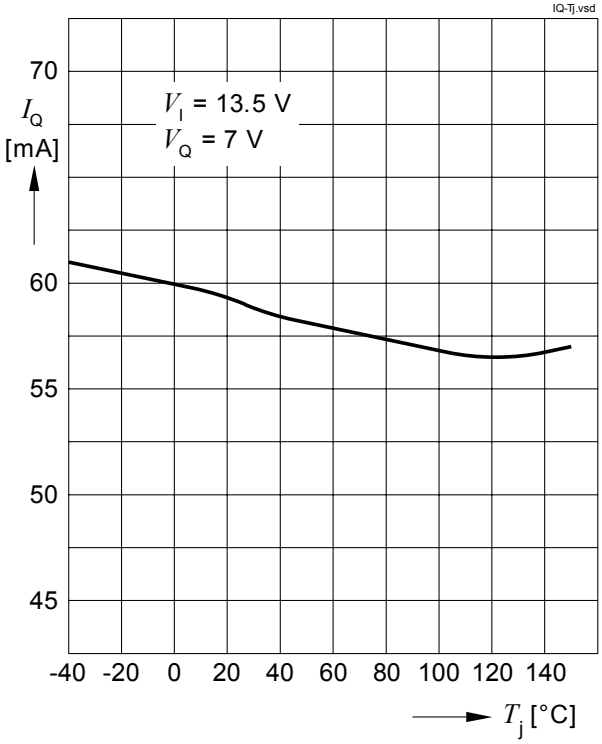


Dropout Voltage V_{dr} vs. Junction Temperature T_j

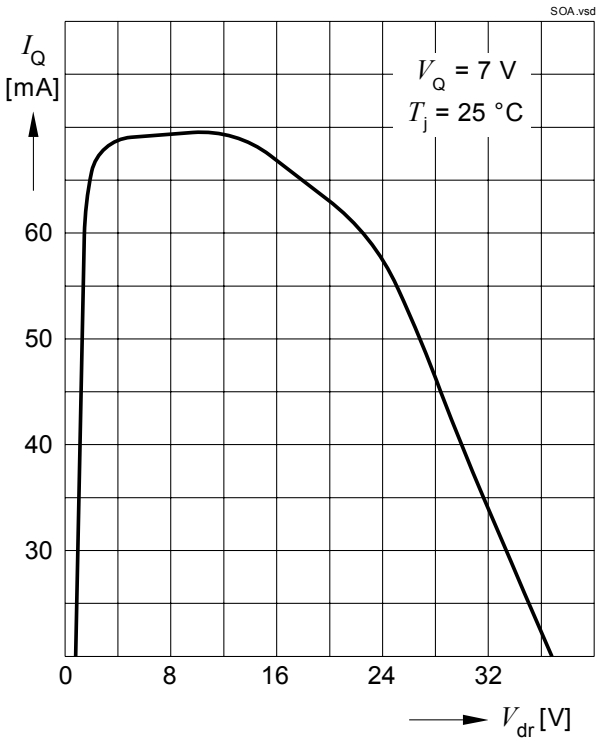


Typical Performance Characteristics

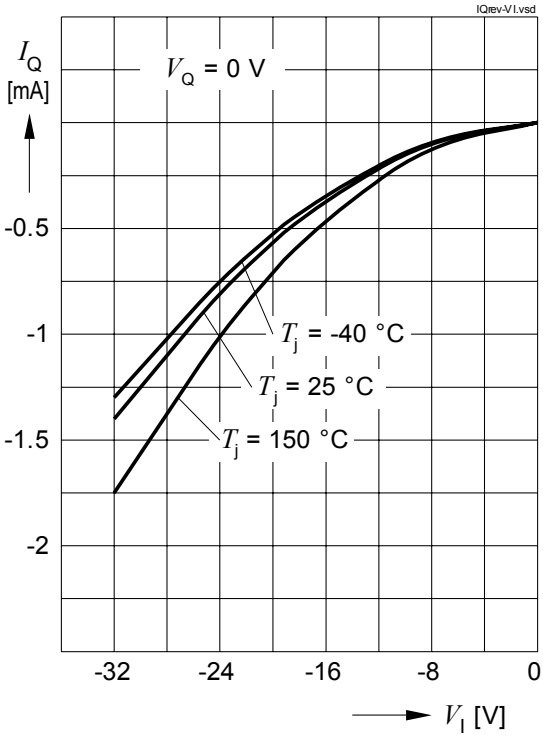
Output Current I_Q vs. Junction Temperature T_j



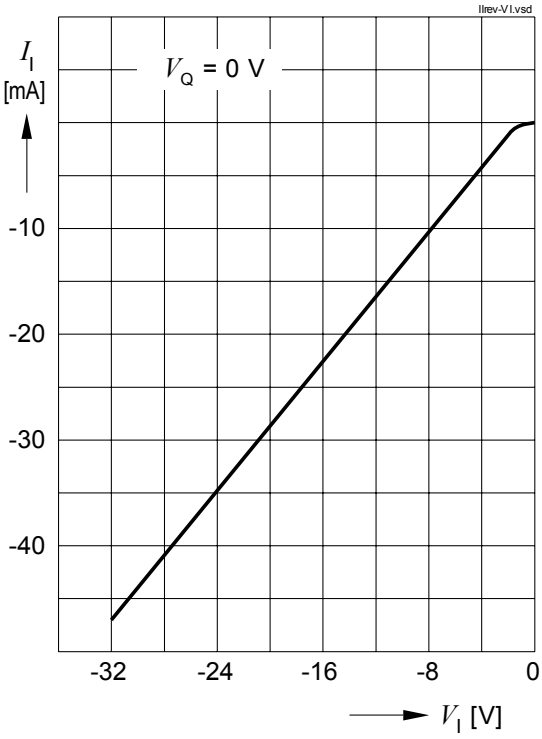
Output Current I_Q vs. Drop Voltage V_{dr} (SOA)



Reverse Current I_Q versus Reverse Input Voltage V_I

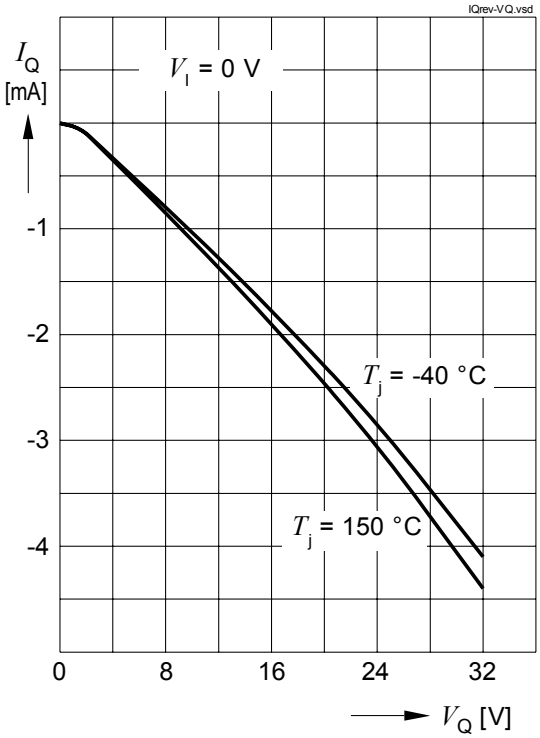


Reverse Current I_I versus Reverse Input Voltage V_I

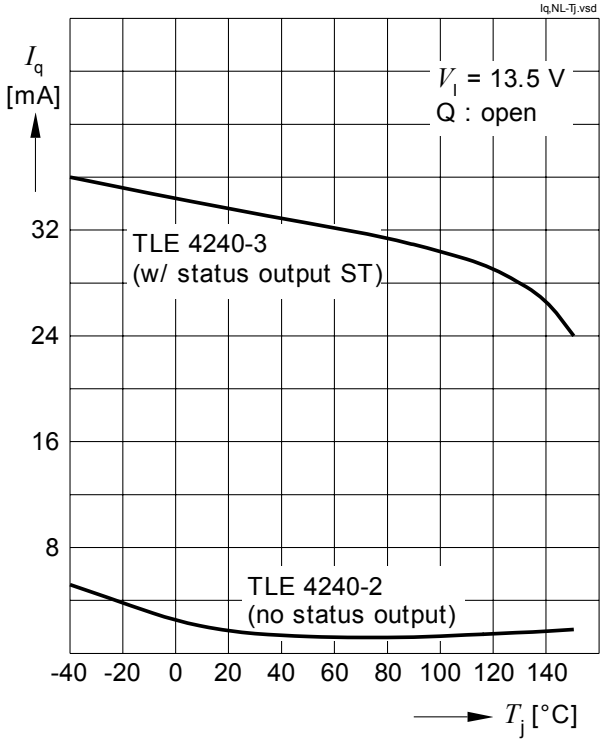


Typical Performance Characteristics

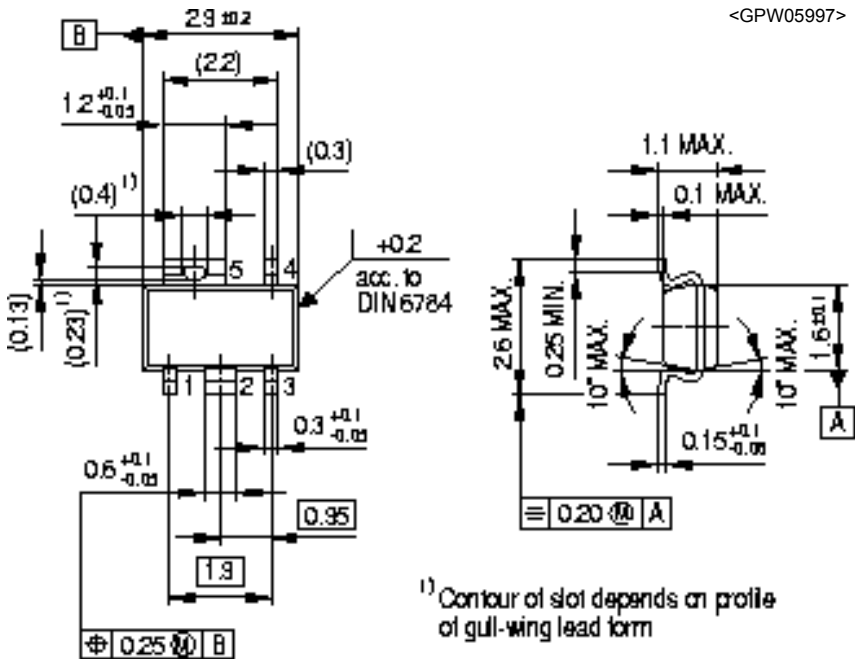
Reverse Output Current I_Q versus Output Voltage V_Q

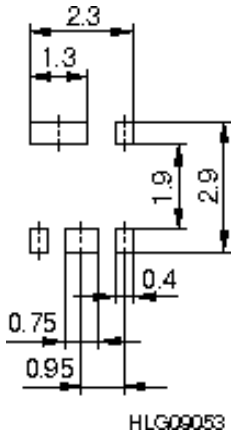


Current Consumption I_q in open load condition vs. T_j

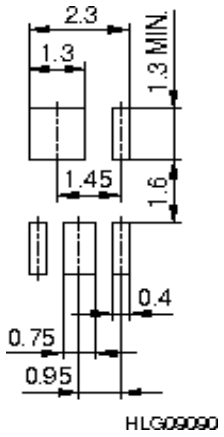


Package Outline





Footprint
Reflow Soldering



Footprint
Wave Soldering

Figure 4 PG-SCT595-5

Find all packages, sorts of packing and others at Infineon Internet Page “Packages”: **http://www.infineon.com/packages**.

SMD = Surface Mounted Device

Dimensions in mm

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