Description (Continued)

The TISP4A265H3BJ is guaranteed to voltage limit and withstand the listed international lightning surges in both polarities. This high (H) current protection device is in a plastic SMBJ package (JEDEC DO-214AA with J-bend leads) and supplied in embossed carrier reel pack. For alternative voltage and holding current values, consult the factory.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, (see Note 1)	V_{DRM}	+100 -200	V
Non-repetitive peak on-state pulse current (see Notes 2, 3 and 4)	I_{TSP}		A
2/10 µs (GR-1089-CORE, 2/10 µs voltage wave shape)		500	
8/20 µs (IEC 61000-4-5, 1.2/50 µs voltage, 8/20 current combination wave generator)		300	
10/160 µs (TIA/EIA-IS-968 (Replaces FCC Part 68), 10/160 µs voltage wave shape)		250	
5/310 µs (ITU-T K.44, 10/700 µs voltage wave shape used in K.20/45/21)		200	
5/320 µs (TIA/EIA-IS-968 (Replaces FCC Part 68), 9/720 µs voltage wave shape)		200	
10/560 µs (TIA/EIA-IS-968 (Replaces FCC Part 68), 10/560 µs voltage wave shape)		160	
10/1000 µs (GR-1089-CORE, 10/1000 µs voltage wave shape)		100	
Non-repetitive peak on-state current (see Notes 2, 3 and 5)	I_{TSM}		A
20 ms (50 Hz) full sine wave		55	
16.7 ms (60 Hz) full sine wave		60	
1000 s 50 Hz/60 Hz a.c.		2.2	
Initial rate of rise of on-state current, Exponential current ramp, Maximum ramp value < 200 A	di_T/dt	400	A/µs
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. See Figure 7 for voltage values at other temperatures.
2. Initially, the TISP4A265H3BJ must be in thermal equilibrium with T_J = 25 °C.
3. The surge may be repeated after the TISP4A265H3BJ returns to its initial conditions.
4. See Figure 8 for current ratings at other temperatures.
5. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 6 for the current ratings at other durations. Derate current values at -0.61 %/°C for ambient temperatures above 25 °C.

Overload Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Maximum overload on-state current without open circuit, 50 Hz/60 Hz a.c. (see Note 6)	$I_{T(OV)M}$		A rms
0.03 s		60	
0.07 s		40	
1.6 s		8	
5.0 s		7	
1000 s		2.2	

NOTE 6: Peak overload on-state current during a.c. power cross tests of GR-1089-CORE and UL 1950/60950. These electrical stress levels may damage the TISP4A265H3BJ silicon chip. After test, the pass criterion is either that the device is functional or, if it is faulty, that it has a short circuit fault mode. In the short circuit fault mode, the following equipment is protected as the device is a permanent short across the line. The equipment would be unprotected if an open circuit fault mode developed.

Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	V_D = +100 V and -200 V	T_A = 25 °C			±5	μA
			T_A = 85 °C			±10	
$V_{(BO)}$	Breakover voltage	dv/dt = 250 V/ms, R_{SOURCE} = 300 Ω				+125	V
						-265	
$I_{(BO)}$	Breakover current	dv/dt = 250 V/ms, R_{SOURCE} = 300 Ω		±0.15		±0.6	A
I_H	Holding current	I_T = ±5 A, di/dt = +/-30 mA/ms		±0.15		±0.6	A
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85V_{DRM}		±5			kV/μs
I_D	Off-state current	V_D = ±50 V	T_A = 85 °C			±10	μA
C_{off}	Off-state capacitance	f = 1 MHz, V_d = 1 V rms, (see Note 7)	V_D = 98 V		25	30	pF
			V_D = 50 V		30	36	
			V_D = 10 V		45	54	
			V_D = 5 V		52	62	
			V_D = 2 V		60	72	
			V_D = 1 V		65	79	
			V_D = 0		71	86	
			V_D = -1 V		65	79	
			V_D = -2 V		58	69	
			V_D = -5 V		48	57	
			V_D = -10 V		40	48	
			V_D = -50 V		26	31	
			V_D = -100 V		20	24	

NOTE 7: To avoid possible voltage clipping, the TISP4A265H3BJ is tested with V_D = +98 V in the positive polarity.

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\Theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, I_T = $I_{TSM(1000)}$, T_A = 25 °C, (see Note 8)			113	°C/W
		265 mm x 210 mm populated line card, 4-layer PCB, I_T = $I_{TSM(1000)}$, T_A = 25 °C		50		

NOTE 8: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

Parameter Measurement Information

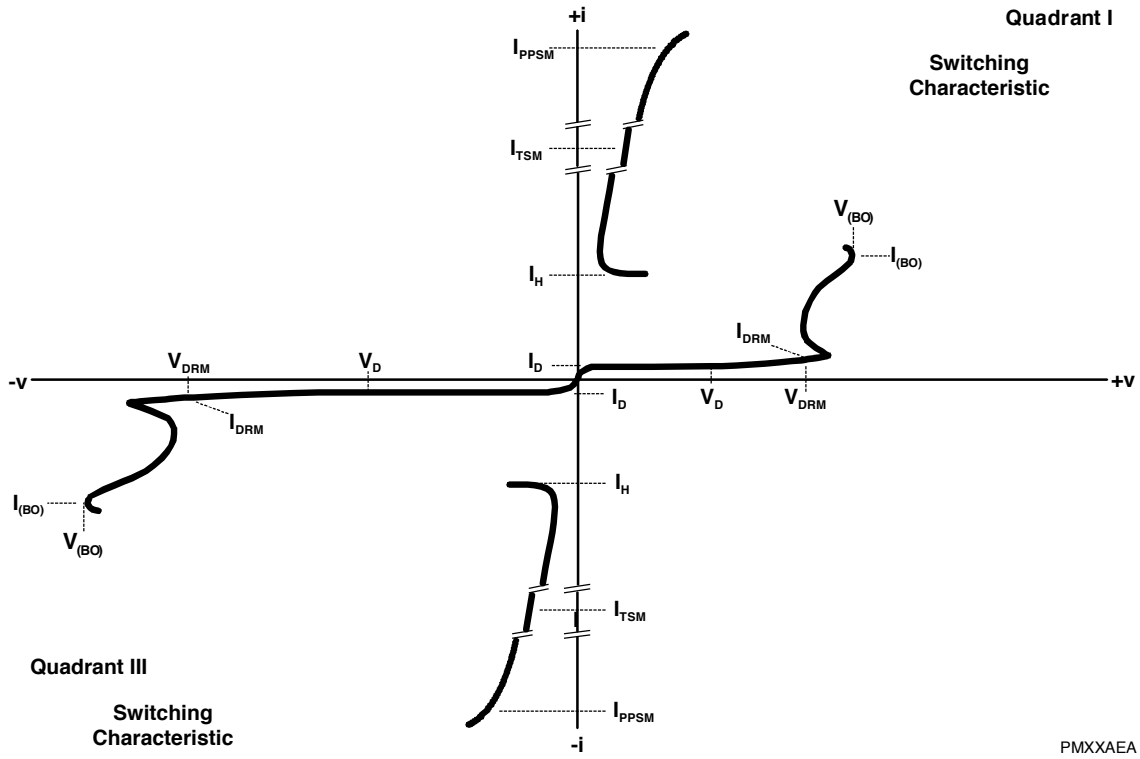


Figure 1. Voltage-Current Characteristic for MT1 and MT2 Terminals
All Measurements are Referenced to the MT1 Terminal

Typical Characteristics

OFF-STATE CURRENT vs JUNCTION TEMPERATURE

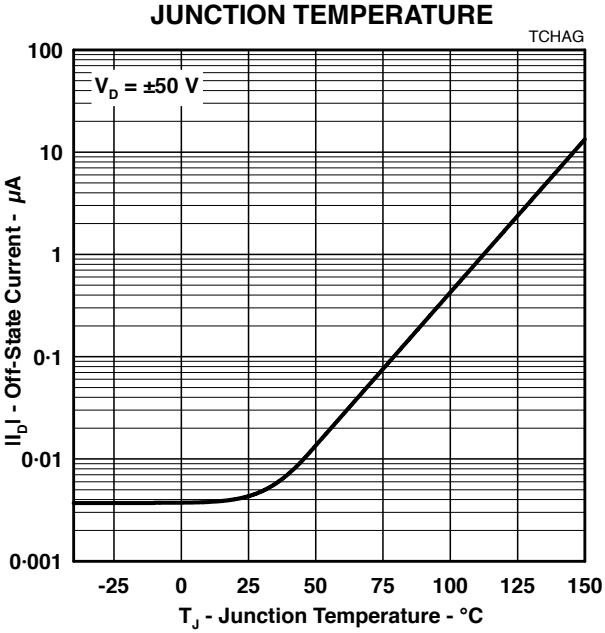


Figure 2.

NORMALIZED BREAKOVER VOLTAGE vs JUNCTION TEMPERATURE

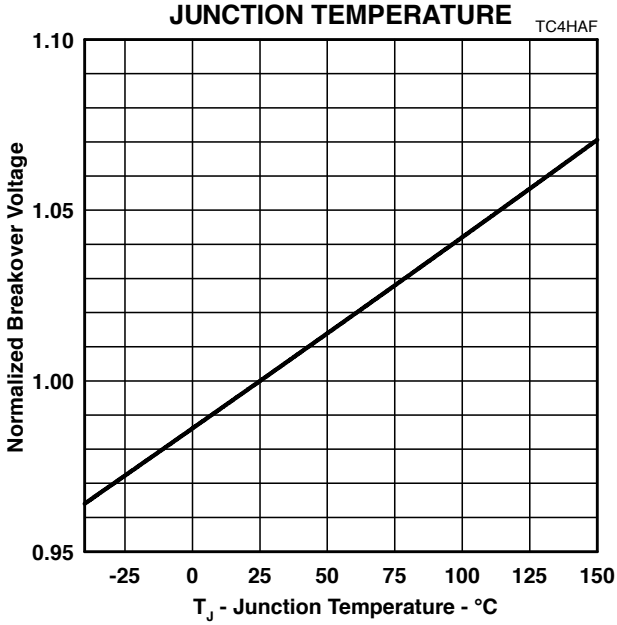


Figure 3.

ON-STATE CURRENT vs ON-STATE VOLTAGE

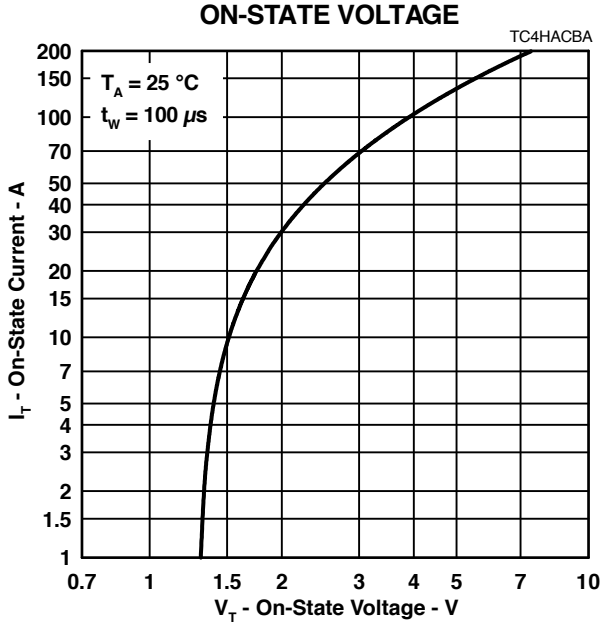


Figure 4.

NORMALIZED HOLDING CURRENT vs JUNCTION TEMPERATURE

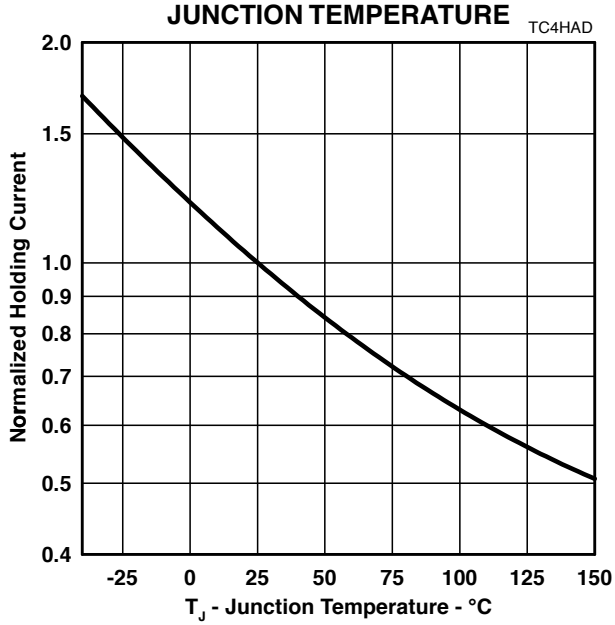


Figure 5.

Rating and Thermal Information

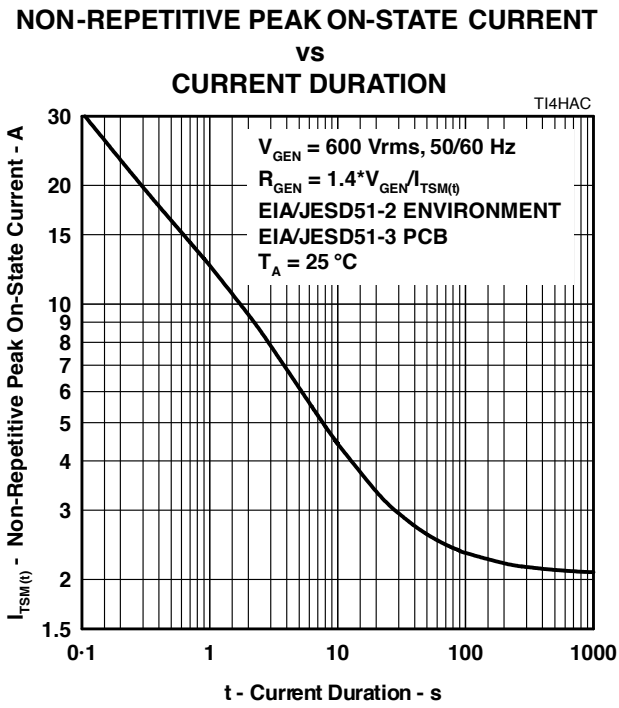


Figure 6.

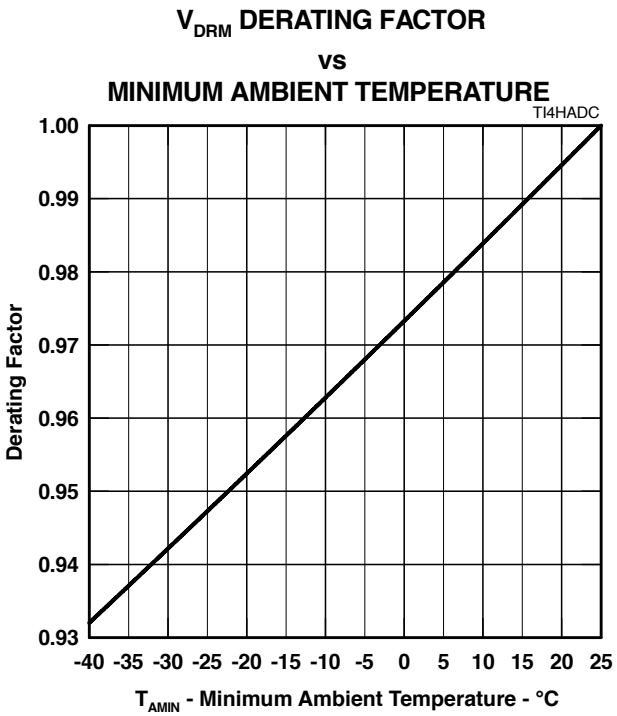


Figure 7.

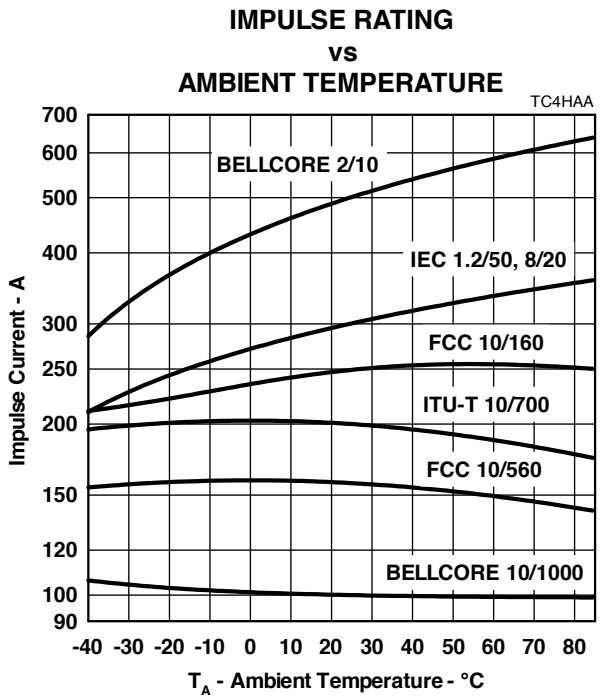


Figure 8.

Typical Circuits

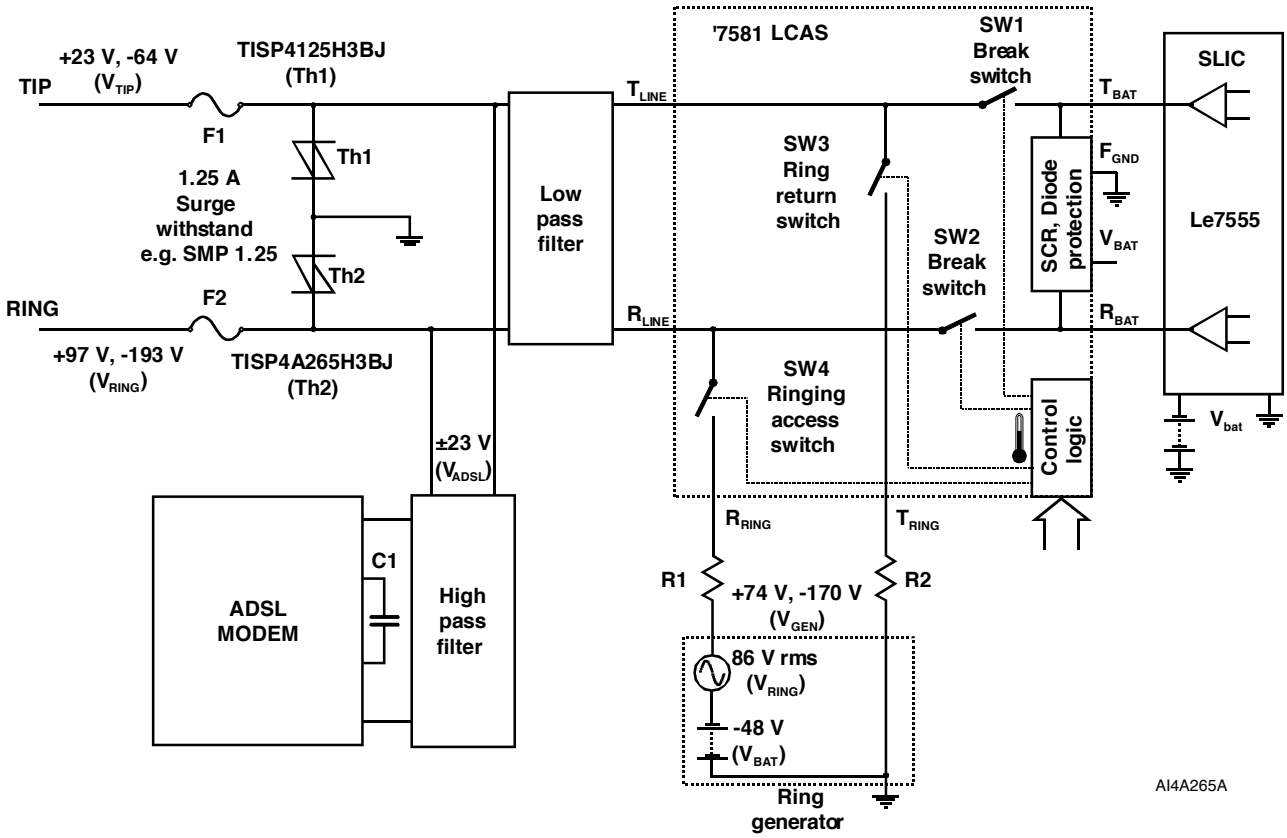
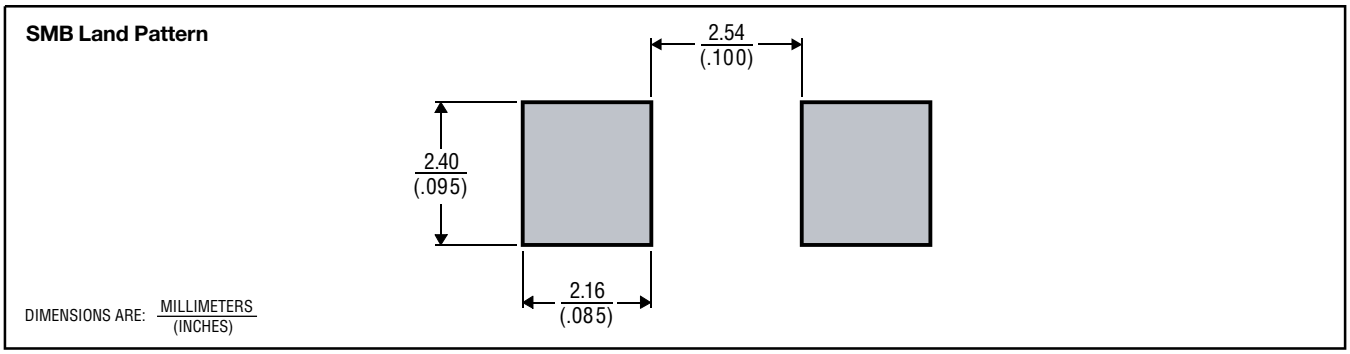


Figure 9. Integrated Voice Data (IVD) System with Typical Operating Voltage Levels Indicated

MECHANICAL DATA

Recommended Printing Wiring Land Pattern Dimensions



MDXXBID

Device Symbolization Code

Devices will be coded as below. Terminal 1 is indicated by an adjacent bar marked on the package body.

Device	Symbolization Code
TISP4A265H3BJ	4A265H

Carrier Information

For production quantities, the carrier will be embossed tape reel pack. Evaluation quantities may be shipped in bulk pack or embossed tape.

Package	Carrier	Standard Quantity
SMB	Embossed Tape Reel Pack	3000

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JANUARY 2002 – REVISED JULY 2019

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