

- Chip Select digital input for parallel operation of several TDA8035 ICs.

### 2.2.1 Other

- HVQFN32 package
- Compliant with ISO 7816, NDS and EMV 4.3 (\*) payment systems

(\*) for C2 version

## 3. Applications

- Pay TV
- Electronic payment
- Identification
- IC card readers for banking

## 4. Quick reference data

**Table 1. Quick reference data**

$V_{DDP} = 3.3\text{ V}$ ;  $V_{DD(INTF)} = 3.3\text{ V}$ ;  $f_{XTAL} = 10\text{ MHz}$ ;  $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V <sub>DDP</sub>	power supply voltage		2.7	3.3	5.5	V
V <sub>DD(INTF)</sub>	interface supply voltage		1.6	3.3	3.6	V
I <sub>DDP</sub>	power supply current	deep shutdown mode; f <sub>XTAL</sub> = stopped;	-	0.1	3	μA
		shutdown mode; f <sub>XTAL</sub> = stopped;	-	300	500	μA
		active mode; V <sub>CC</sub> = +5 V CLK = f <sub>XTAL</sub> /2; no load	-	-	5	mA
		active mode; CLK = f <sub>XTAL</sub> /2; V <sub>CC</sub> = +5 V; I <sub>CC</sub> = 65 mA	-	-	220	mA
		active mode; CLK = f <sub>XTAL</sub> /2; V <sub>CC</sub> = +3 V; I <sub>CC</sub> = 65 mA	-	-	160	mA
		active mode; CLK = f <sub>XTAL</sub> /2; V <sub>CC</sub> = +1.8 V; I <sub>CC</sub> = 35 mA	-	-	120	mA
I <sub>DD(INTF)</sub>	interface supply current	deep shutdown mode; f <sub>XTAL</sub> = stopped; present card	-	-	1	μA
		shutdown mode; f <sub>XTAL</sub> = stopped; present card	-	-	1	μA
Internal supply voltage						
V <sub>DD</sub>	supply voltage		1.62	1.8	1.98	V

**Table 1.** Quick reference data ...continued

$V_{DDP} = 3.3\text{ V}$ ;  $V_{DD(INTF)} = 3.3\text{ V}$ ;  $f_{Xtal} = 10\text{ MHz}$ ;  $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Card supply voltage: pin VCC						
V <sub>CC</sub>	supply voltage	5 V card; DC I <sub>CC</sub> < 65 mA	4.75	5.0	5.25	V
		5 V card; AC current spikes of 40 nA/s	4.65	5.0	5.25	V
		3 V card; DC I <sub>CC</sub> < 65 mA	2.85	-	3.15	V
		3 V card; AC current spikes of 40 nA/s	2.76	-	3.24	V
		1.8 V card; DC I <sub>CC</sub> < 35 mA	1.71	-	1.89	V
		1.8 V card; AC current spikes of 15 nA/s	1.66	-	1.94	V
V <sub>ripple(p-p)</sub>	peak-to-peak ripple voltage	from 20 kHz to 200 MHz	-	-	300	mV
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 5 V or 3 V	-	-	65	mA
		V <sub>CC</sub> = 1.8 V	-	-	35	mA
General						
t <sub>deact</sub>	deactivation time	total sequence	35	90	250	μs
P <sub>tot</sub>	total power dissipation		-	-	0.45	W
T <sub>amb</sub>	ambient temperature		−25	-	+85	°C

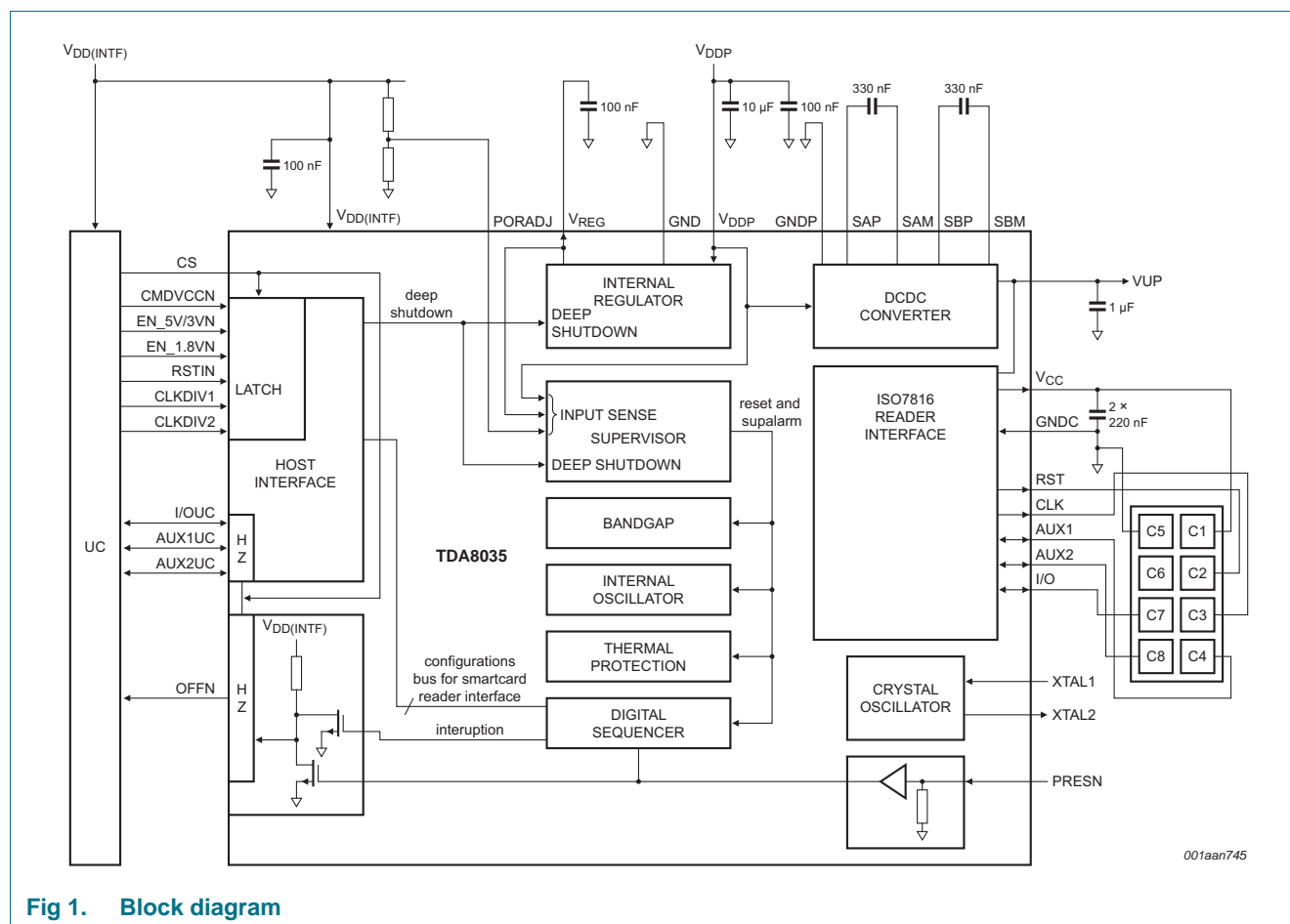
## 5. Ordering information

The TDA8035 is available in 2 versions, which have the same functionalities. The C2 version is compliant with the EMVCO 4.3 standard.

**Table 2.** Ordering information

Type number	Package		
	Name	Description	Version
TDA8035HN/C1	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body $5 \times 5 \times 0.85\text{ mm}$	SOT617-7
TDA8035HN/C1/S1	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body $5 \times 5 \times 0.85\text{ mm}$ ; [1]	SOT617-7
TDA8035HN/C2/S1	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body $5 \times 5 \times 0.85\text{ mm}$ ; [1]	SOT617-7

[1] copper wiring



**Fig 1. Block diagram**

7. Pinning information

7.1 Pinning

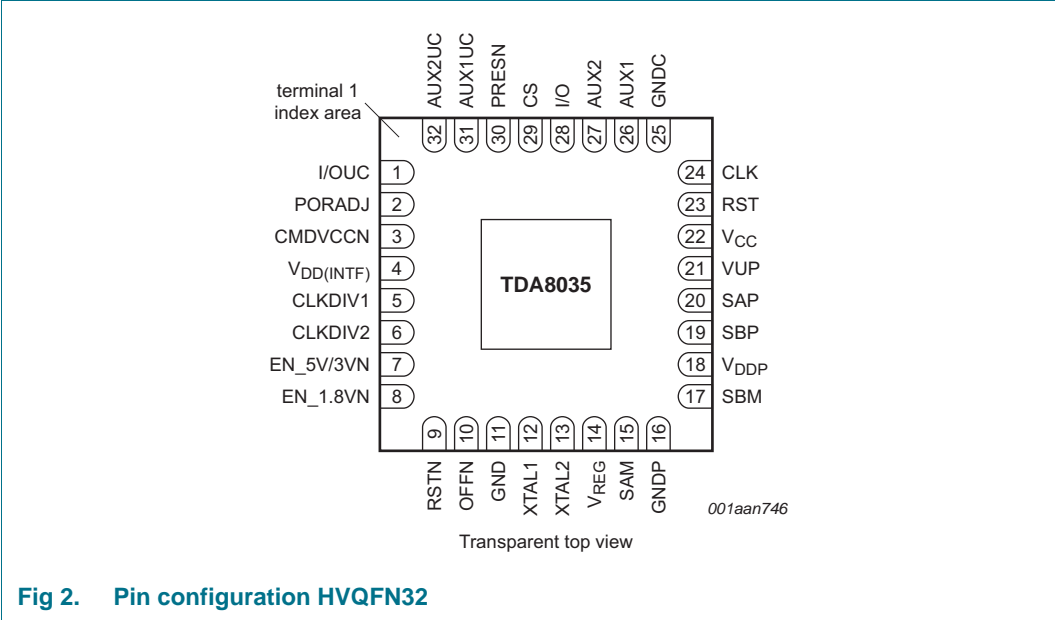


Fig 2. Pin configuration HVQFN32

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Supply	Type	Description
I/OUC	1	V <sub>DD(INTF)</sub>	I/O	host data I/O line (internal 10 kΩ pull-up resistor to V <sub>DD(INTF)</sub> )
PORADJ	2	V <sub>DD(INTF)</sub>	I	Input for V <sub>DD(INTF)</sub> supervisor. PORADJ threshold can be changed with an external R bridge
CMDVCCN	3	V <sub>DD(INTF)</sub>	I	start activation sequence input from the host (active LOW)
V <sub>DD(INTF)</sub>	4	V <sub>DD(INTF)</sub>	supply	interface supply voltage
CLKDIV1	5	V <sub>DD(INTF)</sub>	I	control with CLKDIV2 for choosing CLK frequency (see Table 4)
CLKDIV2	6	V <sub>DD(INTF)</sub>	I	control with CLKDIV1 for choosing CLK frequency (see Table 4)
EN_5V/3VN	7	V <sub>DD(INTF)</sub>	I	control signal for selecting V <sub>CC</sub> = 5 V (HIGH) or V <sub>CC</sub> = 3 V (LOW) if EN_1.8 VN = High
EN_1.8 VN	8	V <sub>DD(INTF)</sub>	I	control signal for selecting V <sub>CC</sub> = 1.8 V (low)
RSTIN	9	V <sub>DD(INTF)</sub>	I	card reset input from the host (active HIGH)
OFFN	10	V <sub>DD(INTF)</sub>	O	NMOS interrupt to the host (active LOW) with 10 kΩ internal pull-up resistor to V <sub>DD(INTF)</sub> (See fault detection)
GND	11	-	supply	ground
XTAL1	12	V <sub>DD(INTF)</sub>	I	crystal connection 1
XTAL2	13	V <sub>DD(INTF)</sub>	O	crystal connection 2
V <sub>REG</sub>	14	V <sub>DDP</sub>	supply	Internal supply voltage
SAM	15	V <sub>DDP</sub>	I/O	DC-to-DC converter capacitor; connected between SAM and SAP; C = 330 nF or 100 nF (see Figure 13) with ESR < 100 mΩ at Freq=100kHz
GNDP	16	-	supply	DC-to-DC converter power supply ground

Table 3. Pin description ...continued

Symbol	Pin	Supply	Type	Description
SBM	17	V <sub>DDP</sub>	I/O	DC-to-DC converter capacitor; connected between SBM and SBP; C = 330 nF or 100nF (see <a href="#">Figure 13</a> ) with ESR < 100 mΩ at Freq=100kHz
V <sub>DDP</sub>	18	V <sub>DDP</sub>	supply	Power supply voltage
SBP	19	V <sub>DDP</sub>	I/O	DC-to-DC converter capacitor; connected between SBM and SBP; C = 330 nF or 100nF (see <a href="#">Figure 13</a> ) with ESR < 100 mΩ at Freq=100kHz
SAP	20	V <sub>DDP</sub>	I/O	DC-to-DC converter capacitor; connected between SAM and SAP; C = 330 nF or 100nF (see <a href="#">Figure 13</a> ) with ESR < 100 mΩ at Freq=100kHz
VUP	21	V <sub>DDP</sub>	I/O	DC-to-DC converter output decoupling capacitor connected between VUP and GNDC; C = 1 μF with ESR < 100 mΩ at Freq=100kHz
V <sub>CC</sub>	22	V <sub>CC</sub>	O	supply for the card (C1), decouple to GND with 2 × 220 nF capacitors with ESR < 100 mΩ
RST	23	V <sub>CC</sub>	O	card reset (C2)
CLK	24	V <sub>CC</sub>	O	clock to the card (C3)
GNDC	25	-	supply	card signal ground
AUX1	26	V <sub>CC</sub>	I/O	auxiliary data line to and from the card (C4), internal 10 kΩ pull-up resistor to V <sub>CC</sub>
AUX2	27	V <sub>CC</sub>	I/O	auxiliary data line to and from the card (C8), internal 10 kΩ pull-up resistor to V <sub>CC</sub>
I/O	28	V <sub>CC</sub>	I/O	data line to and from the card (C7), internal 10 kΩ pull-up resistor to V <sub>CC</sub>
CS	29	V <sub>DD(INTF)</sub>	I	Chip Select input from the host (active High)
PRESN	30	V <sub>DD(INTF)</sub>	I	Card presence contact input (active LOW); if PRESN is true, then the card is considered as present. A debouncing feature of 4.05 ms typical is built in.
AUX1UC	31	V <sub>DD(INTF)</sub>	I/O	auxiliary data line to and from the host, internal 10 kΩ pull-up resistor to V <sub>DD(INTF)</sub>
AUX2UC	32	V <sub>DD(INTF)</sub>	I/O	auxiliary data line to and from the host, internal 10 kΩ pull-up resistor to V <sub>DD(INTF)</sub>

## 8. Functional description

**Remark:** The ISO 7816 terminology convention has been adhered to throughout this document, and it is assumed that the reader is familiar with this convention.

### 8.1 Power supply

Power supply voltage  $V_{DDP}$  is from 2.7 V to 5.5 V

All interface signals with the system controller are referenced to  $V_{DD(INTF)}$ . All card contacts remain inactive during powering up or powering down.

Internal regulator  $V_{REG}$  is 1.8 V

After powering the device, OFFN remains low until CMDVCCN is set high and PRESN is low.

During power off, OFFN falls low when  $V_{DDP}$  is below the threshold voltage falling.

While the card is not activated, CMDVCCN is kept at high level. To save power consumption, the frequency of the internal oscillator ( $f_{osc(int)}$ ) used for the activation sequences is put in low frequency mode.

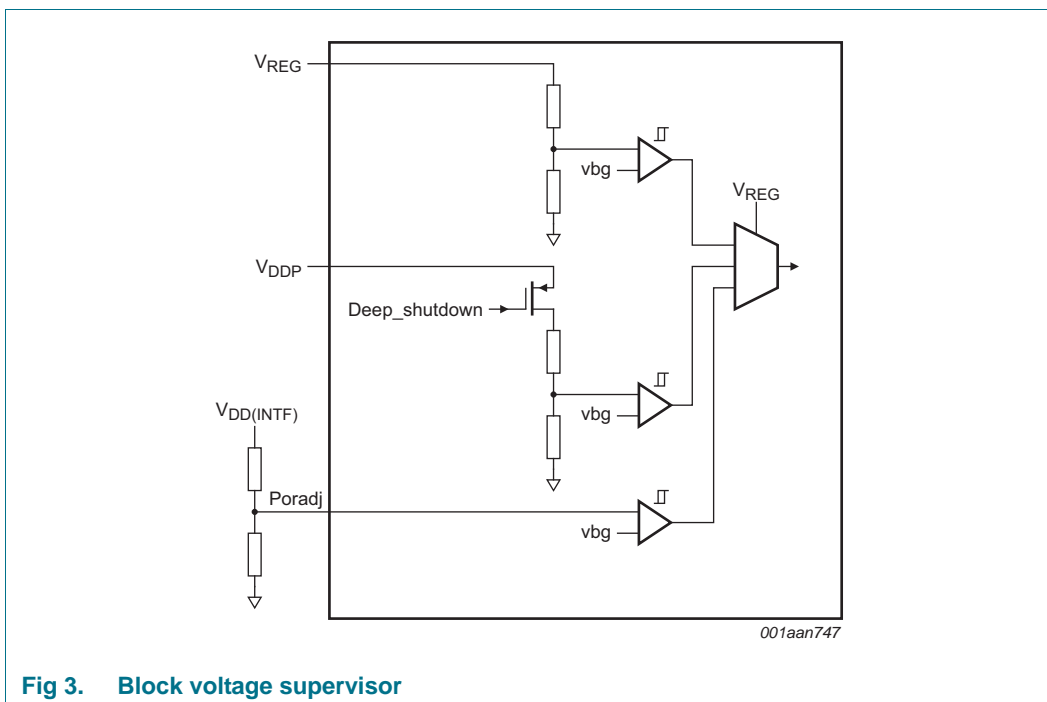
This device includes a DC-to-DC converter to generate the 5 V, 3 V or 1.8 V card supply voltage ( $V_{CC}$ ). The DC-to-DC converter is separately supplied by  $V_{DDP}$  and  $G_{NDP}$ . The DC-to-DC converter operates as a voltage tripler, doubler or follower according to the respective values of  $V_{CC}$  and  $V_{DDP}$ .

Special care has to be made in the selection of the capacitors of the DC/DC converter specially with respect to capacitor value versus voltage and ESR (see [Table 7](#))

The operating mode is as follows (see [Figure 3](#)):

- $V_{CC} = 5\text{ V}$  and  $V_{DDP} > 3.8\text{ V}$ ; voltage doubler
- $V_{CC} = 5\text{ V}$  and  $V_{DDP} < 3.6\text{ V}$ ; voltage tripler
- $V_{CC} = 3\text{ V}$  and  $V_{DDP} > 3.8\text{ V}$ ; voltage follower
- $V_{CC} = 3\text{ V}$  and  $V_{DDP} < 3.6\text{ V}$ ; voltage doubler
- $V_{CC} = 1.8\text{ V}$  and  $V_{DDP} > 3.8\text{ V}$ ; voltage doubler
- $V_{CC} = 1.8\text{ V}$  and  $V_{DDP} < 3.6\text{ V}$ ; voltage tripler

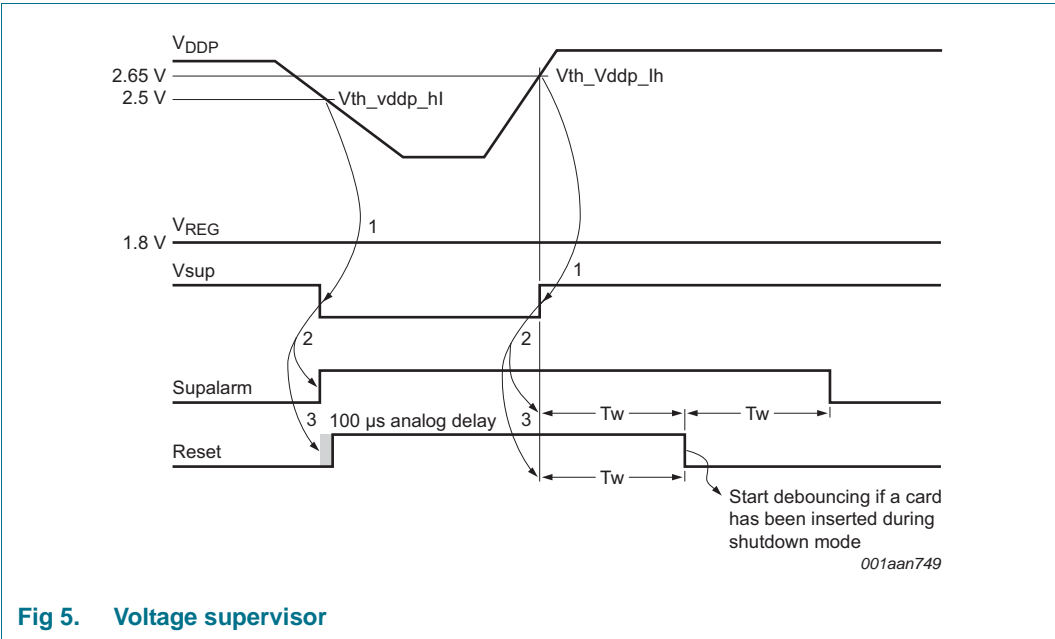
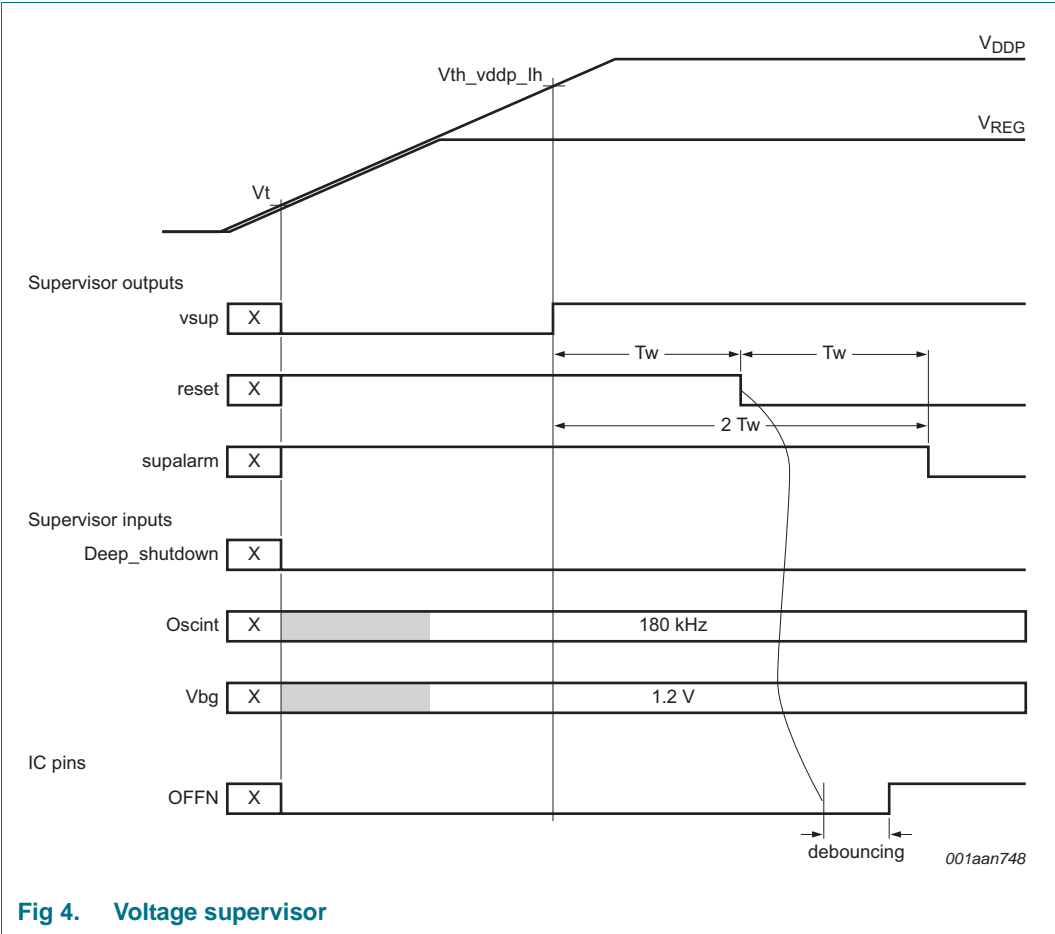
## 8.2 Voltage supervisor



**Fig 3. Block voltage supervisor**

The voltage supervisor is used as a power-on reset, and also as supply drop detection during a card session. The threshold of the voltage supervisor is set internally in the IC for VDDP and VREG. The threshold can be adjusted externally for VDD(INTF) using the PORADJ pin. As long as VREG is less than  $V_{th(VREG)} + V_{hys(VREG)}$ , the IC remains inactive whatever the levels on the command lines are. The inactivity lasts for the duration of  $t_w$  after VREG has reached a level higher than  $V_{th(VREG)} + V_{hys(VREG)}$ . The outputs of the VDDP, VREG and VDD(INTF) supervisors are combined and sent to a digital controller in order to reset the TDA8035. The reset pulse of approximately 5.7 ms ( $t_w = 2048 \times 1/(f_{osc(int\_Low)})$ ) is used internally for maintaining the IC in an inactive mode during the supply voltage power-on (see [Figure 4](#) and [Figure 5](#)). A deactivation sequence is performed when:

- VREG falls below  $V_{th(VREG)}$
- $V_{DD(INTF)}$  falls below  $V_{th(PORADJ)}$
- VDDP falls below  $V_{th(VDDP)}$





8.3 Clock circuitry

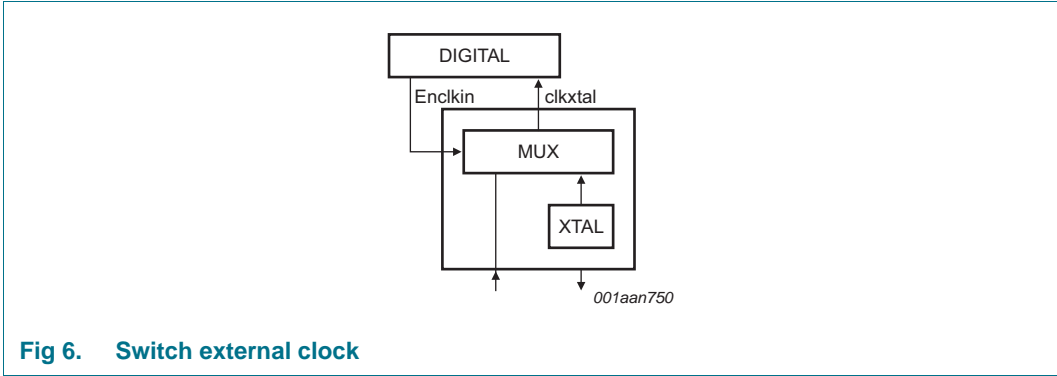


Fig 6. Switch external clock

To generate the card clock CLK, the TDA8035 can either use an external clock provided on XTAL1 pin or a crystal oscillator connected on both XTAL1 and XTAL2 pins. The TDA8035 automatically detects when an external clock is provided on XTAL1. Consequently, there is no need for an extra pin to configure the clock source (external clock or crystal).

The automatic clock source detection is performed on each activation command (CMDVCCN pin falling edge). During a time window defined by the internal oscillator, the presence of an external clock on XTAL1 pin is checked. If a clock is detected, the crystal oscillator is kept stopped, else, the crystal oscillator is started. It is mandatory when an external clock is used, that the clock is applied on XTAL1 before CMDVCCN falling edge signal.

The frequency is chosen as  $f_{XTAL}$ ,  $f_{XTAL/2}$ ,  $f_{XTAL/4}$  or  $f_{XTAL/8}$  via the pins CLKDIV1 and CLKDIV2. Both selection inputs are not changed simultaneously. A minimum of 10 ns is required between changes on CLKDIV1 and CLKDIV2.

The frequency change is synchronous, which means that during transition, no pulse is shorter than 45 % of the smallest period. This ensures that the first and last clock pulse around the change has the correct width. When changing the frequency dynamically, the change is effective for only 10 periods of XTAL1 after the command.

The duty cycle on pin CLK is between 45 % and 55 %:

- When an external clock is used on XTAL1 pin and  $f_{XTAL}$  is used, the duty cycle is between 48 % and 52 %. The subsequent rise and fall times ( $t_{r(i)}$  and  $t_{f(i)}$ ) conform to values listed in [Table 7](#). It has to connect a 56 pF serial capacitor (see [Figure 13](#)).
- CLK frequency is  $f_{XTAL}$ ,  $f_{XTAL/2}$ ,  $f_{XTAL/4}$  or  $f_{XTAL/8}$ :  
It is guaranteed between 45 % and 55 % of the period by the frequency dividers.

Table 4. Clock configuration

CLKDIV1	CLKDIV2	CLK
0	0	$f_{XTAL/8}$
0	1	$f_{XTAL/4}$
1	1	$f_{XTAL/2}$
1	0	$f_{XTAL}$

## 8.4 I/O circuitry

The three data lines I/O, AUX1 and AUX2 are identical.

To enter the idle state, both lines (I/O and I/OUC) are pulled HIGH via a 10 k $\Omega$  resistor (I/O to  $V_{CC}$  and I/OUC to  $V_{DD(INTF)}$ ).

I/O is referenced to  $V_{CC}$ , and I/OUC to  $V_{DD(INTF)}$  which allows operation with  $V_{CC} \neq V_{DD(INTF)}$ .

The first side on which a falling edge occurs becomes the master. An anti-latch circuit disables the detection of falling edges on the other line, which becomes the slave.

After a time delay  $t_{d(edge)}$ , the logic 0 present on the master side is transmitted to the slave side.

When the master side returns to logic 1, the slave side transmits the logic 1 during the time delay  $t_{pu}$  and both sides return to their idle states.

The active pull-up feature ensures fast Low to High transitions. It is able to deliver more than 1 mA to an output voltage of 0.9  $V_{CC}$  on an 80 pF load. At the end of the active pull-up pulse, the output voltage depends on the internal pull-up resistor and on the load current.

The current to and from the cards I/O lines is internally limited to 15 mA.

The maximum frequency on these lines is 1.5 MHz.

## 8.5 CS control

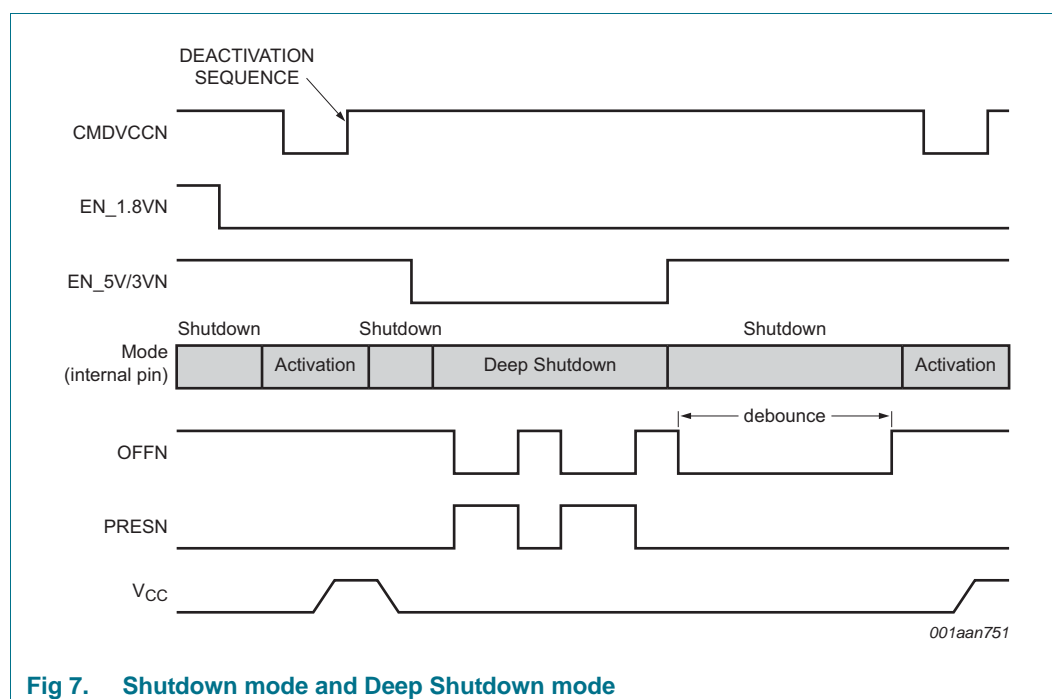
The CS (Chip Select) input allows multiple devices to operate in parallel. When CS is high, the system interface signals operate as described. When CS is low, the signals CMDVCCN, RSTIN, CLKDIV1, CLKDIV2, EN\_5V/3VN and EN\_1.8VN are latched. I/OUC, AUX1UC and AUX2UC are set to high impedance pull-up mode and data is no longer passed to or from the smart card. The OFFN output is a 3-state output.

## 8.6 Shutdown mode and Deep Shutdown mode

After power-on reset, the circuit enters the Shutdown mode if CMDVCCN input pin is set to a logic high. A minimum number of circuits are active while waiting for the microcontroller to start a session.

1. All card contacts are inactive (approximately 200  $\Omega$  to GND).
2. I/OUC, AUX1UC and AUX2UC are high impedance (10 kW pull-up resistor connected to  $V_{DD(INTF)}$ ).
3. Voltage generators are stopped.
4. Voltage supervisor is active.
5. The internal oscillator runs at its low frequency.

A Deep Shutdown mode can be entered by forcing CMDVCCN input pin to a logic-High state and EN\_5V/3VN, EN\_1.8VN input pins to a logic-Low state. Deep Shutdown mode can only be entered when the smart card reader is inactive. In Deep Shutdown mode, all circuits are disabled. The OFFN pin follows the status of PRESN pin. To exit Deep Shutdown mode, change the state of one or more of the three control pins. [Figure 8](#) shows the control sequence for entering and exiting.



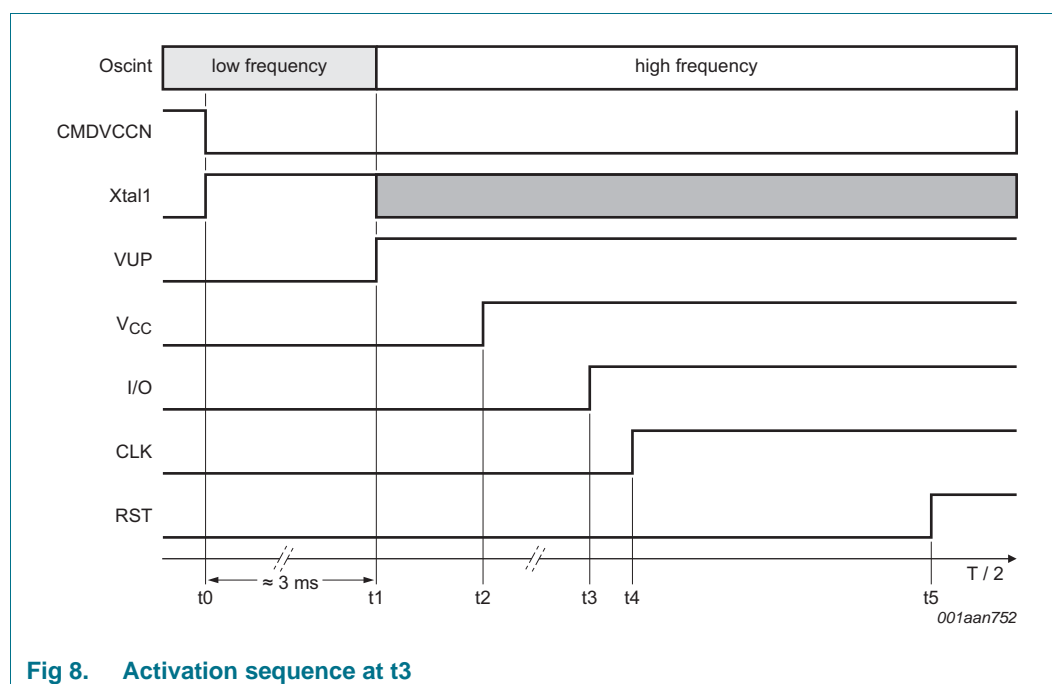
**Fig 7. Shutdown mode and Deep Shutdown mode**

## 8.7 Activation sequence

The following sequence then occurs with crystal oscillator (see [Figure 8](#)):

$$T = 64 \times T_{\text{oscint}} (\text{freq high})$$

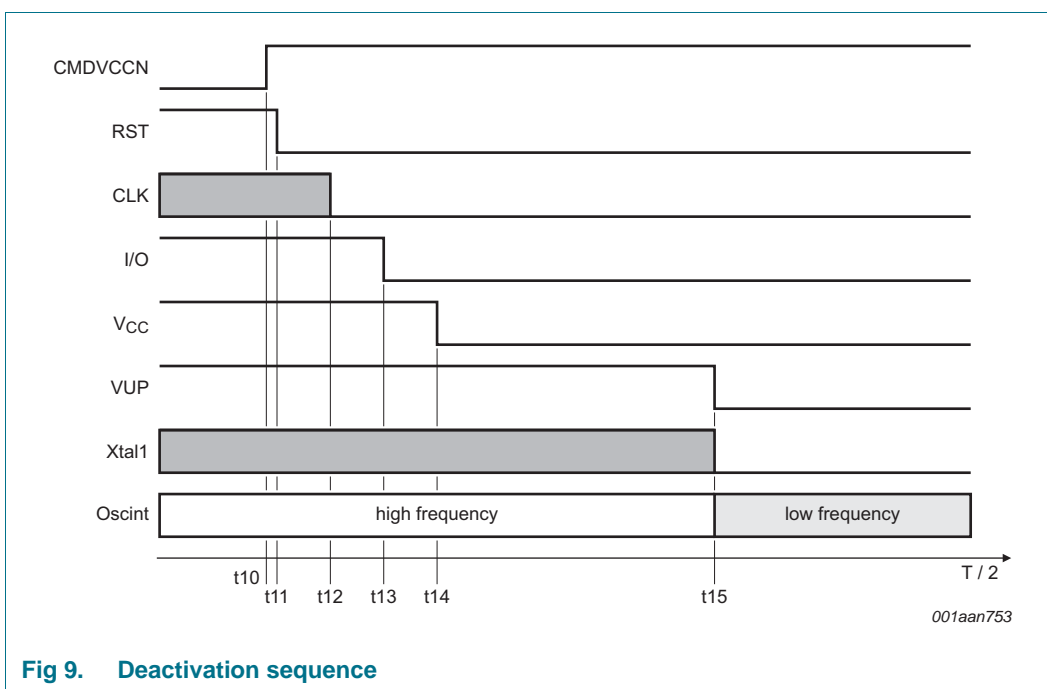
1. CMDVCCN is pulled low ( $t_0$ )
2. Crystal oscillator start-up time ( $t_0$ ).
3. The internal oscillator changes to its high frequency and DC-to-DC starts  
 $t_1 = t_0 + 768 \times T_{\text{osc}} (\text{freq low})$
4.  $V_{\text{CC}}$  rises from 0 to selected  $V_{\text{CC}}$  value (5 V, 3 V, 1.8 V) with a controlled slope  
 $(t_2 = t_1 + 3T/2)$
5. I/O, AUX1 and AUX2 are enabled ( $t_3 = t_1 + 10T$ ), until now, they were pulled LOW
6. CLK is applied to the C3 contact ( $t_4 = t_3 + x$ ) with  $200 \text{ ns} < x < 10 \times 1/f_{\text{Xtal}}$
7. RST is enabled ( $t_5 = t_1 + 13T$ ).



## 8.8 Deactivation sequence

When a session is completed, the microcontroller sets the CMDVCCN line to the HIGH state. The circuit then executes an automatic deactivation sequence by counting the sequencer back and ends in the inactive state (see [Figure 9](#)):

1. RST goes LOW ( $t_{11} = t_{10} + 3T/64$ )
2. CLK is stopped LOW ( $t_{12} = t_{11} + T/2$ )
3. I/O, AUX1 and AUX2 are pulled LOW ( $t_{13} = t_{11} + T$ )
4.  $V_{CC}$  falls to zero ( $t_{14} = t_{11} + 3T/2$ ). The deactivation sequence is completed when  $V_{CC}$  reaches its inactive state
5. VUP falls to zero ( $t_{15} = t_{11} + 7T/2$ )
6.  $V_{CC} < 0.4\text{ V}$  ( $t_{de} = t_{11} + 3T/2 + V_{CC}\text{ fall time}$ )
7. All card contacts become low-impedance to GND. I/OUC, AUX1UC and AUX2UC remain pulled up to  $V_{DD(INTF)}$  via a  $10\text{ k}\Omega$  resistor.
8. The internal oscillator reverts to its lower frequency.



## 8.9 $V_{CC}$ regulator

$V_{CC}$  buffer is able to deliver up to 65 mA continuously at  $V_{CC} = 5\text{ V}$  and  $V_{CC} = 3\text{ V}$ , and 35 mA at  $V_{CC} = 1.8\text{ V}$ .

$V_{CC}$  buffer has an internal overload detection at approximately 125 mA.

This detection is internally filtered, allowing the card to draw spurious current pulses of up to 200 mA for some milliseconds, without causing a deactivation. The average current value must remain below the maximum.

## 8.10 Fault detection

The circuit monitors the following fault conditions:

- short-circuit or high current on  $V_{CC}$
- Card removal during transaction
- $V_{DDP}$  or  $V_{DD(INTF)}$  or  $V_{reg}$  dropping
- overheating.

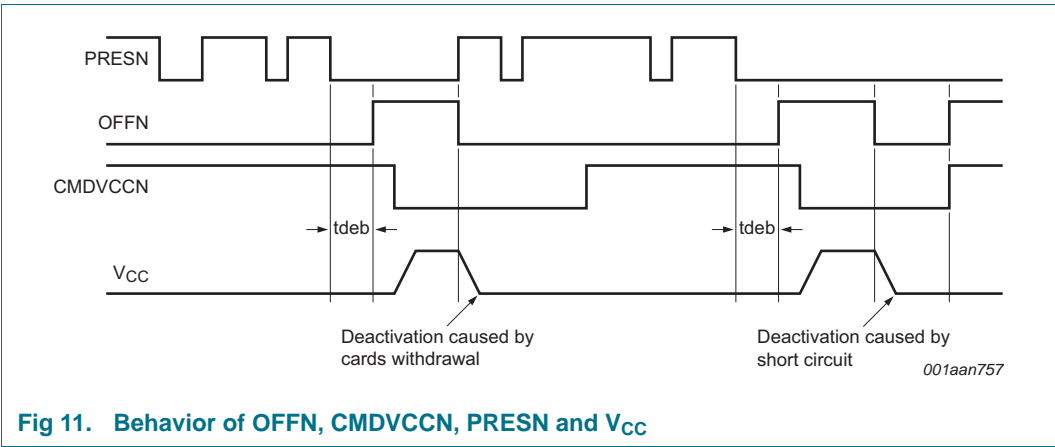
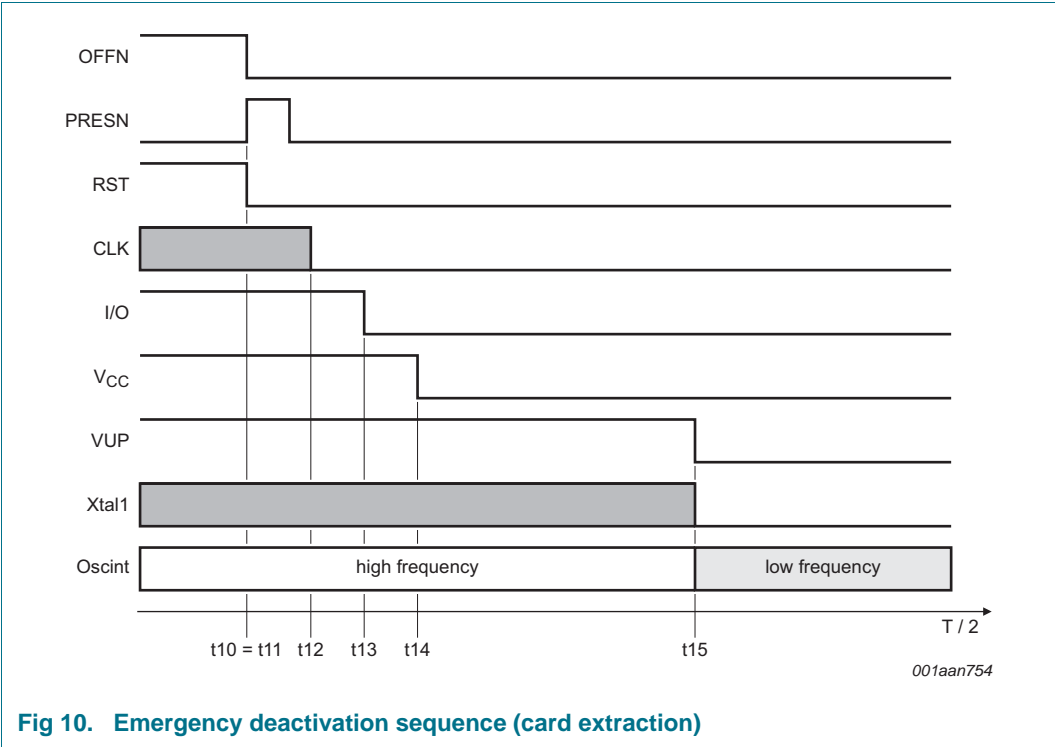
There are two different cases (see [Figure 10 on page 16](#)):

1. CMDVCCN High (outside a card session): OFFN is Low when the card is not in the reader, and High when the card is in the reader. The supply supervisor detects a supply voltage drop on  $V_{DDP}$  and generates an internal power-on reset pulse, but it does not act upon OFFN. The card is not powered-up, so no short-circuit or overheating is detected.
2. CMDVCCN Low (within a card session): OFFN falls Low in any of the previously mentioned cases. As soon as the fault is detected, an emergency deactivation is automatically performed. When the system controller sets CMDVCCN back to High, it senses OFFN again. After a complete deactivation sequence, the system controller sets CMDVCCN back to High and it senses OFFN again. This is to distinguish between a hardware problem or a card extraction. OFFN reverts to High when the card is still present.

A bounce can occur on the PRESN signal during card insertion or withdrawal. The bounce depends on the type of card presence switch within the connector (normally closed or normally open), and on the mechanical characteristics of the switch. To prevent this bounce, a debounce function of approximately 4.05 ms ( $t_{deb} = 1280 \times 1/(f_{osc(int)}_{Low})$ ) is integrated in the device.

When the card is inserted, OFFN goes High only at the end of the debounce time (see [Figure 11 on page 16](#)).

When the card is extracted, an automatic deactivation sequence of the card is performed on the first true/false transition on PRESN. OFFN goes Low.



## 9. Limiting values

All card contacts are protected against a short-circuit with any other card contact.

Stress beyond the limiting values can damage the device permanently. The values are stress ratings only and functional operation of the device under these conditions is not implied.

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DDP</sub>	power supply voltage		−0.3	6	V
V <sub>DD(INTF)</sub>	interface supply voltage		−0.3	4.1	V
V <sub>IH</sub>	HIGH-level input voltage	CS, PRESN, CMDVCCN, CLKDIV2, CLKDIV1, EN_1.8VN, EN_5V/3VN, RSTIN, OFFN, PORADJ, XTAL1, I/OUC, AUX1UC, AUX2UC, VDDP, VDD(INTF)	−0.3	4.1	V
		I/O, RST, AUX1, AUX2 and CLK	−0.3	5.75	V
T <sub>amb</sub>	ambient temperature		−25	+85	°C
T <sub>stg</sub>	storage temperature		−55	+150	°C
T <sub>j</sub>	junction temperature			+125	°C
P <sub>tot</sub>	total power dissipation			0.45	W
V <sub>ESD</sub>	electrostatic discharge voltage	Human Body Model (HBM) on card pins I/O, RST, V <sub>CC</sub> , AUX1, CLK, AUX2, PRESN within typical application	−10	+10	kV
		Human Body Model (HBM) on all other pins	−2	+2	kV
		Machine Model (MM) on all pins	−200	+200	V
		Field Charged Device Model (FCDM) on all pins	−500	+500	V

## 10. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Package name	Parameter	Conditions	Typ	Unit
R <sub>th(j-a)</sub>	HVQFN32	thermal resistance from junction to ambient	in free air with 4 thermal vias on PCB	55	K/W
			in free air without thermal vias on PCB	63	K/W



## 11. Characteristics

**Table 7. Characteristics of IC**
 $V_{DDP} = 3.3\text{ V}$ ;  $V_{DD(INTF)} = 3.3\text{ V}$ ;  $f_{XTAL} = 10\text{ MHz}$ ;  $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply voltage</b>						
$V_{DDP}$	power supply voltage		2.7	3.3	5.5	V
$V_{DD(INTF)}$	interface supply voltage		1.6	3.3	3.6	V
$I_{DDP}$	power supply current	deep Shutdown mode; $f_{XTAL} = \text{stopped}$	-	0.1	3	$\mu\text{A}$
		Shutdown mode; $f_{XTAL} = \text{stopped}$	-	300	500	$\mu\text{A}$
		active mode; $\text{CLK} = f_{XTAL}/2$ ; $V_{CC} = +5\text{ V}$ ; no load	-	-	5	mA
		active mode; $\text{CLK} = f_{XTAL}/2$ ; $V_{CC} = +5\text{ V}$ ; $I_{CC} = 65\text{ mA}$	-	-	220	mA
		active mode; $\text{CLK} = f_{XTAL}/2$ ; $V_{CC} = +3\text{ V}$ ; $I_{CC} = 65\text{ mA}$	-	-	160	mA
		active mode; $\text{CLK} = f_{XTAL}/2$ ; $V_{CC} = +1.8\text{ V}$ ; $I_{CC} = 35\text{ mA}$	-	-	120	mA
$I_{DD(INTF)}$	interface supply current	deep Shutdown mode $f_{XTAL} = \text{stopped}$ ; present card	-	-	1	$\mu\text{A}$
		Shutdown mode $f_{XTAL} = \text{stopped}$ ; present card	-	-	1	$\mu\text{A}$
$V_{th(VREG)}$	threshold voltage on pin $V_{REG}$	internal voltage regulator falling	1.38	1.45	1.52	V
$V_{hys(VREG)}$	hysteresis voltage on pin $V_{REG}$		90	100	110	mV
$V_{th(VDDP)}$	threshold voltage on pin $V_{DDP}$	pin VDDP falling	2.15	2.25	2.35	V
$V_{hys(VDDP)}$	hysteresis voltage on pin $V_{DDP}$		90	100	110	mV
$t_w$	pulse width		3.0	6.5	8.9	ms
$V_{th(L)(PORADJ)}$	LOW-level threshold voltage on pin PORADJ	external resistors on PORADJ	0.81	0.85	0.89	V
$V_{hys(PORADJ)}$	hysteresis voltage on pin PORADJ		30	60	90	mV
$I_L$	leakage current	pin PORADJ	-1	-	+1	$\mu\text{A}$
<b>VREG</b>						
$V_o$	output voltage		1.62	1.80	1.98	V
$t_r$	rise time	exit of deep Shutdown mode	-	-	200	$\mu\text{s}$

**Table 7. Characteristics of IC ...continued** $V_{DDP} = 3.3\text{ V}$ ;  $V_{DD(INTF)} = 3.3\text{ V}$ ;  $f_{XTAL} = 10\text{ MHz}$ ;  $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VUP (DC-to-DC converter)						
V <sub>OH</sub>	HIGH-level output voltage	VDDP=3.3V, VCC = 5 V, ICC < 65 mA DC	5.10	5.60	7.00	V
		VDDP=3.3V, VCC = 3 V, ICC < 65 mA DC	3.50	3.95	5.00	V
		VDDP=3.3V, VCC = 1.8 V, ICC < 35 mA DC	5.10	5.60	7.00	V
		VDDP=5V, VCC = 5 V, ICC < 65 mA DC	5.10	5.80	7.00	V
		VDDP=5V, VCC = 3 V, ICC < 65 mA DC	-	5.00	-	V
		VDDP=5V, VCC = 1.8 V, ICC < 35 mA DC	5.10	5.80	7.00	V
SAP (DC-to-DC converter)						
V <sub>OH</sub>	HIGH-level output voltage	VDDP=3.3V, VCC = 5 V, ICC < 65 mA DC	-	-	8.20	V
		VDDP=3.3V, VCC = 3 V, ICC < 65 mA DC	-	-	6.00	V
		VDDP=3.3V, VCC = 1.8 V, ICC < 35 mA DC	-	-	8.20	V
		VDDP=5V, VCC = 5 V, ICC < 65 mA DC	-	-	8.20	V
		VDDP=5V, VCC = 3 V, ICC < 65 mA DC	-	5.00	-	V
		VDDP=5V, VCC = 1.8 V, ICC < 35 mA DC	-	-	8.20	V
DC-to-DC converter capacitors						
C <sub>SAPSAM</sub>	DC/DC converter capacitance	connected between SAP and SAM (330 nF [4]) with VDDP=3.3v	231	-	429	nF
		connected between SAP and SAM (100 nF [4]) with VDDP=5v	70	-	130	nF
C <sub>SBPSBM</sub>	DC/DC converter capacitance	connected between SBP and SBM (330 nF [4]) with VDDP=3.3v	231	-	429	nF
		connected between SBP and SBM (100 nF [4]) with VDDP=5v	70	-	130	nF
C <sub>VUP</sub>	DC/DC converter capacitance	connected on VUP(1uF [4])	700	-	1300	nF
Card supply voltage (V <sub>CC</sub> )[1]						
C <sub>dec</sub>	decoupling capacitance	connected on V <sub>CC</sub> (220 nF + 220 nF 10 %)	396	-	484	nF
V <sub>o</sub>	output voltage	inactive mode; no load	-0.1	-	+0.1	V
		inactive mode; I <sub>o</sub> = 1 mA	-0.1	-	+0.3	V

**Table 7. Characteristics of IC ...continued** $V_{DDP} = 3.3\text{ V}$ ;  $V_{DD(INTF)} = 3.3\text{ V}$ ;  $f_{XTAL} = 10\text{ MHz}$ ;  $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>o</sub>	output current	inactive mode at grounded pin VCC	-	-	−1	mA
V <sub>CC</sub>	supply voltage	active mode; 5 V card; ICC < 65 mA DC	4.75	5.0	5.25	V
		active mode; 3 V card; ICC < 65 mA DC	2.85	3.05	3.15	V
		active mode; 1.8 V card; ICC < 35 mA DC	1.71	1.83	1.89	V
		active mode; current pulses of 40 nA/s with ICC < 200 mA, t < 400 ns; 5 V card	4.65	5.0	5.25	V
		active mode; current pulses of 40 nA/s with ICC < 200 mA, t < 400 ns; 3 V card	2.76	-	3.20	V
		active mode; current pulses of 15 nA/s with ICC < 200 mA, t < 400 ns; 1.8 V card	1.66	-	1.94	V
V <sub>ripple(p-p)</sub>	peak-to-peak ripple voltage	from 20 kHz to 200 MHz	-	-	350	mV
I <sub>CC</sub>	supply current	VCC = 0 V to 5 V, 3 V	-	-	65	mA
		VCC = 0 V to 1.8 V	-	-	35	mA
SR	slew rate	5 V card	0.055	0.18	0.8	V/μs
		3 V card	0.040	0.18	0.8	V/μs
		1.8 V card	0.025	0.18	0.8	V/μs
Crystal oscillator (XTAL1 and XTAL2)						
C <sub>ext</sub>	external capacitance	connected on pins XTAL1/XTAL2 (depending on specification of crystal or resonator used)	-	-	33	pF
f <sub>xtal</sub>	crystal frequency		2	-	27	MHz
f <sub>xtal(XTAL1)</sub>	crystal frequency on pin XTAL1	with 56 pF serial capacitor	0	-	27	MHz
V <sub>IL</sub>	LOW-level input voltage		-0.3	-	+0.3 V <sub>DD(INTF)</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7 V <sub>DD(INTF)</sub>	-	V <sub>DD(INTF)</sub> + 0.3	V
t <sub>r(i)</sub>	input rise time	f <sub>CLK</sub> = f <sub>XTAL1</sub> = 20 MHz on external clock	-	-	4	ns
		f <sub>CLK</sub> = f <sub>XTAL1</sub> = 10 MHz on external clock	-	-	8	ns
		f <sub>CLK</sub> = f <sub>XTAL1</sub> = 5 MHz on external clock	-	-	16	ns

**Table 7. Characteristics of IC ...continued** $V_{DDP} = 3.3\text{ V}$ ;  $V_{DD(INTF)} = 3.3\text{ V}$ ;  $f_{XTAL} = 10\text{ MHz}$ ;  $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>f(i)</sub>	input fall time	f <sub>CLK</sub> = f <sub>XTAL1</sub> = 20 MHz on external clock	-	-	4	ns
		f <sub>CLK</sub> = f <sub>XTAL1</sub> = 10 MHz on external clock	-	-	8	ns
		f <sub>CLK</sub> = f <sub>XTAL1</sub> = 5 MHz on external clock	-	-	16	ns
Data lines (pins I/O, I/OUC, AUX1, AUX2, AUXIUC, AUX2UC)						
t <sub>d</sub>	delay time	falling edge on pins I/O and I/OUC or I/OUC and I/O	-	-	200	ns
t <sub>w(pu)</sub>	pull-up pulse width		200		400	ns
f <sub>max</sub>	maximum frequency	on data lines	-	-	1	MHz
C <sub>i</sub>	input capacitance	on data lines	-	-	10	pF
Data lines to the card (pins I/O, AUX1, AUX2); (Integrated 10 kΩ pull-up resistor connected to V <sub>CC</sub> )						
V <sub>o</sub>	output voltage	inactive mode; no load	0	-	0.1	V
		inactive mode; I <sub>o</sub> = 1 mA	0	-	0.3	V
I <sub>o</sub>	output current	inactive mode at grounded pin I/O	-	-	−1	mA
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 1 mA - C1 version	0	-	0.3	V
		I <sub>OL</sub> = 1 mA - C2 version	0	-	0.15 V <sub>CC</sub>	V
		I <sub>OL</sub> ≥ 15 mA	V <sub>CC</sub> - 0.4	-	V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	No DC load	0.9 V <sub>CC</sub>	-	V <sub>CC</sub> + 0.1	V
		I <sub>OH</sub> ≥ -15 mA	0	-	0.4	V
		C1 version				
		I <sub>OH</sub> < -40 μA 5 V or 3 V	0.75 V <sub>CC</sub>		V <sub>CC</sub> + 0.1	V
		I <sub>OH</sub> < -20 μA 1.8 V	0.75 V <sub>CC</sub>		V <sub>CC</sub> + 0.1	V
		C2 version				
		I <sub>OH</sub> < -40 μA 5 V or 3 V	0.8 V <sub>CC</sub>		V <sub>CC</sub> + 0.1	V
		I <sub>OH</sub> < -20 μA 1.8 V	1.28		V <sub>CC</sub> + 0.1	V
V <sub>IL</sub>	LOW-level input voltage	C1 version	−0.3	-	+0.8	V
		C2 version	-0.3		0.2 V <sub>CC</sub>	
V <sub>IH</sub>	HIGH-level input voltage	C1 Version				
		V <sub>CC</sub> = +5 V	0.6 V <sub>CC</sub>	-	V <sub>CC</sub> + 0.3	V
		V <sub>CC</sub> = +3 V or 1.8 V	0.7 V <sub>CC</sub>	-	V <sub>CC</sub> + 0.3	V
		C2 Version				
		V <sub>CC</sub> = +5 V or 3V	0.6 V <sub>CC</sub>	-	V <sub>CC</sub> + 0.3	V
	V <sub>CC</sub> =1.8 V	1.4	-	V <sub>CC</sub> + 0.3	V	
V <sub>hys</sub>	hysteresis voltage	on I/O	30	75	120	mV
I <sub>IL</sub>	LOW-level input current	on I/O; V <sub>IL</sub> = 0	-	-	600	μA
I <sub>LH</sub>	HIGH-level leakage current	on I/O; V <sub>IH</sub> = V <sub>CC</sub>	-	-	10	μA
t <sub>r(i)</sub>	input rise time	from V <sub>IL</sub> max to V <sub>IH</sub> min	-	-	1.2	μs

**Table 7. Characteristics of IC ...continued** $V_{DDP} = 3.3\text{ V}$ ;  $V_{DD(INTF)} = 3.3\text{ V}$ ;  $f_{XTAL} = 10\text{ MHz}$ ;  $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>f(i)</sub>	input fall time	from V <sub>IL</sub> max to V <sub>IH</sub> min	-	-	1.2	μs
t <sub>r(o)</sub>	output rise time	C <sub>L</sub> ≤ 80 pF; 10 % to 90 % from 0 to V <sub>CC</sub>	-	-	0.1	μs
t <sub>f(o)</sub>	output fall time	C <sub>L</sub> ≤ 80 pF; 10 % to 90 % from 0 to V <sub>CC</sub>	-	-	0.1	μs
R <sub>pu</sub>	pull-up resistance	connected to VCC	8	10	12	kΩ
I <sub>pu</sub>	pull-up current	V <sub>OH</sub> = 0.9 V <sub>CC</sub> , C = 80 pF	-8	-6	-4	mA
Data lines to the system; pins I/OμC, AUX1μC, AUX2μC (Integrated kΩ pull-up resistor to V <sub>DD(INTF)</sub> )						
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 1 mA	0	-	0.3	V
V <sub>OH</sub>	HIGH-level output voltage	No DC load	0.9 V <sub>DD(INTF)</sub>	-	V <sub>DD(INTF)</sub> + 0.1	V
		I <sub>OH</sub> ≤ 40 μA; V <sub>DD(INTF)</sub> >2 V	0.75 V <sub>DD(INTF)</sub>	-	V <sub>DD(INTF)</sub> + 0.1	V
		I <sub>OH</sub> ≤ 20 μA; V <sub>DD(INTF)</sub> <2 V	0.75 V <sub>DD(INTF)</sub>	-	V <sub>DD(INTF)</sub> + 0.1	V
V <sub>IL</sub>	LOW-level input voltage		−0.3	-	0.3 V <sub>DD(INTF)</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7 V <sub>DD(INTF)</sub>		V <sub>DD(INTF)</sub> + 0.3	V
V <sub>hys</sub>	hysteresis voltage	on I/Ouc	0.05 V <sub>DD(INTF)</sub>	-	0.25 V <sub>DD(INTF)</sub>	V
I <sub>LH</sub>	HIGH-level leakage current	V <sub>IH</sub> = V <sub>DD(INTF)</sub>			10	μA
I <sub>IL</sub>	LOW-level input current	V <sub>IL</sub> = 0			600	μA
R <sub>pu</sub>	pull-up resistance	connected to VDD(INTF)	8	10	12	kΩ
t <sub>r(i)</sub>	input rise time	from V <sub>IL</sub> max to V <sub>IH</sub> min	-	-	1.2	μs
t <sub>f(i)</sub>	input fall time	from V <sub>IL</sub> max to V <sub>IH</sub> min	-	-	1.2	μs
t <sub>r(o)</sub>	output rise time	C <sub>L</sub> ≤ 30 pF; 10 % to 90 % from 0 to V <sub>DD(INTF)</sub>	-	-	0.1	μs
t <sub>f(o)</sub>	output fall time	C <sub>L</sub> ≤ 30 pF; 10 % to 90 % from 0 to V <sub>DD(INTF)</sub>	-	-	0.1	μs
I <sub>pu</sub>	pull-up current	V <sub>OH</sub> = 0.9 V <sub>DD</sub> , C = 30 pF	-1	-	-	mA
Internal oscillator						
f <sub>osc(int)</sub>	internal oscillator frequency	inactive state: osc(int)_Low	230	315	430	kHz
		active state: osc(int)_High	2.0	2.5	3.0	MHz
Reset output to the card (RST)						
V <sub>o</sub>	output voltage	inactive mode; no load	0	-	0.1	V
		inactive mode; I <sub>o</sub> = 1 mA	0	-	0.3	V
I <sub>o</sub>	output current	inactive mode at grounded pin RST	-	-	−1	mA
t <sub>d</sub>	delay time	between RSTIN and RST, RST enabled	-	-	200	ns
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 200 μA, VCC = +5 V	0	-	0.3	V
		I <sub>OL</sub> = 200 μA, VCC = +3 V or 1.8 V	0	-	0.2	V
		I <sub>OL</sub> = 20 mA (current limit)	V <sub>CC</sub> - 0.4	-	V <sub>CC</sub>	V

**Table 7. Characteristics of IC ...continued** $V_{DDP} = 3.3\text{ V}$ ;  $V_{DD(INTF)} = 3.3\text{ V}$ ;  $f_{XTAL} = 10\text{ MHz}$ ;  $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified

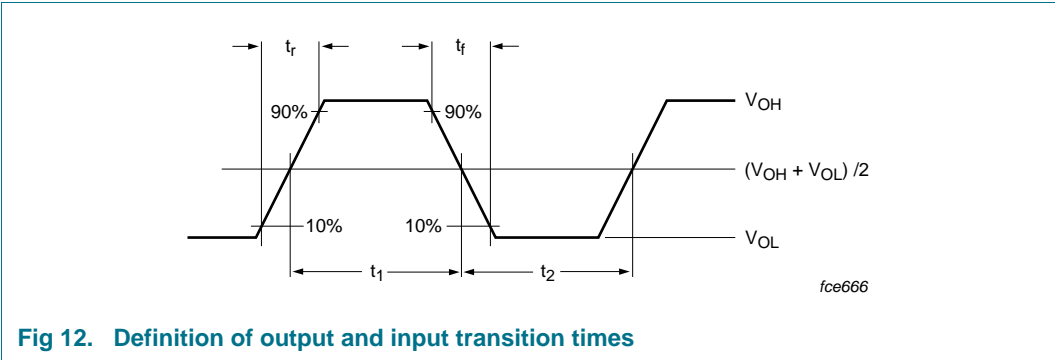
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = -200 μA	0.9 V <sub>CC</sub>	-	V <sub>CC</sub>	V	
		I <sub>OH</sub> = -20 mA (current limit)	0	-	0.4	V	
t <sub>r</sub>	rise time	C <sub>L</sub> = 100 pF V <sub>CC</sub> = +5 V and +3 V	-	-	0.1	μs	
		C <sub>L</sub> = 100 pF V <sub>CC</sub> = +18 V	-	-	0.2	μs	
t <sub>f</sub>	fall time	C <sub>L</sub> = 100 pF V <sub>CC</sub> = +5 V and +3 V	-	-	0.1	μs	
		C <sub>L</sub> = 100 pF V <sub>CC</sub> = +18 V	-	-	0.2	μs	
Clock output to the card (CLK)							
V <sub>o</sub>	output voltage	inactive mode; no load	0	-	0.1	V	
		inactive mode; I <sub>o</sub> = 1 mA	0	-	0.3	V	
I <sub>o</sub>	output current	inactive mode at grounded pin CLK	-	-	−1	mA	
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 70 mA (current limit)	V <sub>CC</sub> - 0.4	-	V <sub>CC</sub>	V	
		C1 version					
		I <sub>OL</sub> = 200 μA	0	-	0.3	V	
		C2 Version					
		I <sub>OL</sub> = 200 μA	0	-	0.15 V <sub>CC</sub>	V	
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = -200 μA	0.9 V <sub>CC</sub>	-	V <sub>CC</sub>	V	
		I <sub>OH</sub> = -70 mA (current limit)	0	-	0.4	V	
t <sub>r</sub>	rise time	C <sub>L</sub> = 30 pF [2]	-	-	16	ns	
t <sub>f</sub>	fall time	C <sub>L</sub> = 30 pF [2]	-	-	16	ns	
f <sub>CLK</sub>	frequency on pin CLK	operational	0	-	20	MHz	
	duty cycle	C <sub>L</sub> = 30 pF [2]	45	-	55	%	
SR	slew rate	rise and fall; C <sub>L</sub> = 30 pF; V <sub>CC</sub> = +5 V	0.2	-	-	V/ns	
		rise and fall; C <sub>L</sub> = 30 pF; V <sub>CC</sub> = +3 V	0.12	-	-	V/ns	
		rise and fall; C <sub>L</sub> = 30 pF; V <sub>CC</sub> = +1.8 V	0.072	-	-	V/ns	
Control inputs (pins CS, CMDVCCN, CLKDIV1, CLKDIV2, RSTIN, EN_5V/ 3VN, EN_1.8VN)[3]							
V <sub>IL</sub>	LOW-level input voltage		−0.3	-	+0.3 V <sub>DD(INTF)</sub>	V	
V <sub>IH</sub>	HIGH-level input voltage		0.7 V <sub>DD(INTF)</sub>	-	V <sub>DD(INTF)</sub> + 0.3	V	
V <sub>hys</sub>	hysteresis voltage	on control input	0.05 V <sub>DD(INTF)</sub>	-	0.25 V <sub>DD(INTF)</sub>	V	
I <sub>LL</sub>	LOW-level leakage current	V <sub>IL</sub> = 0	-	-	1	μA	
I <sub>LH</sub>	HIGH-level leakage current	V <sub>IH</sub> = V <sub>DD(INTF)</sub>	-	-	1	μA	
Card presence input (PRESN); PRESN has an integrated pull down resistor[3]							
V <sub>IL</sub>	LOW-level input voltage		−0.3	-	+0.3 V <sub>DD(INTF)</sub>	V	
V <sub>IH</sub>	HIGH-level input voltage		0.7 V <sub>DD(INTF)</sub>	-	V <sub>DD(INTF)</sub> + 0.3	V	

**Table 7. Characteristics of IC ...continued**

$V_{DDP} = 3.3\text{ V}$ ;  $V_{DD(INTF)} = 3.3\text{ V}$ ;  $f_{XTAL} = 10\text{ MHz}$ ;  $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified

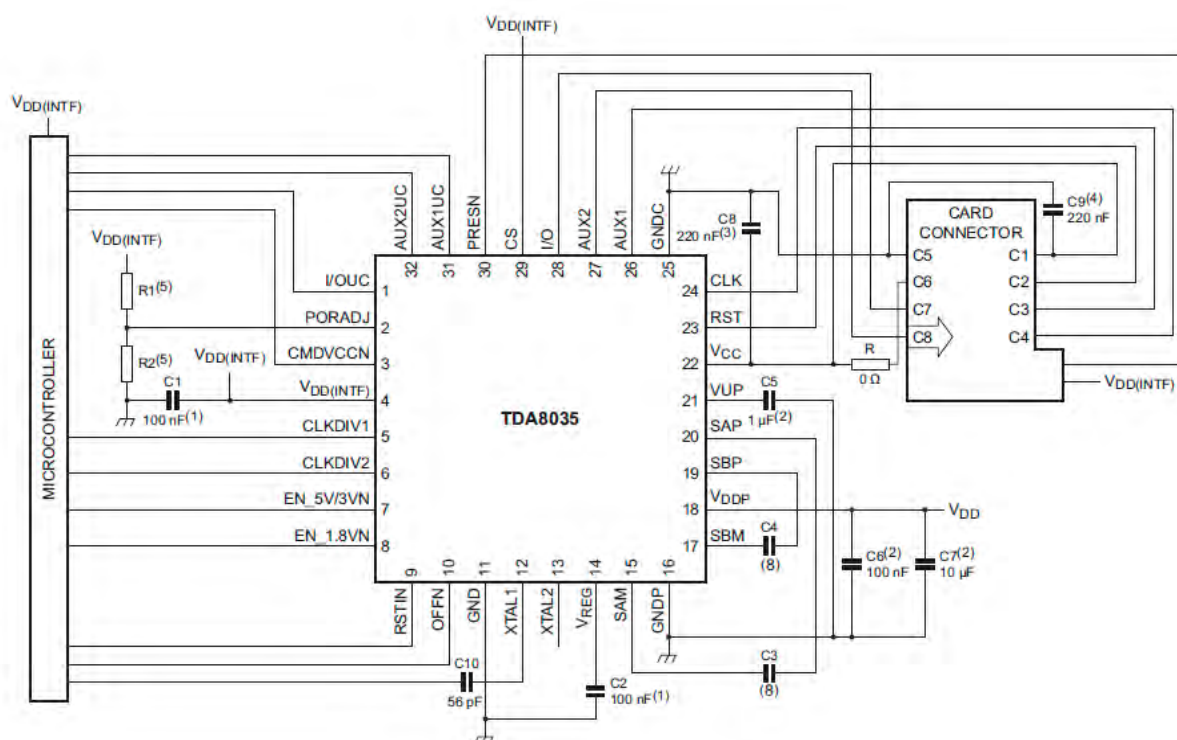
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>hys</sub>	hysteresis voltage		0.05 V <sub>DD(INTF)</sub>	-	0.10 V <sub>DD(INTF)</sub>	V
I <sub>LL</sub>	LOW-level leakage current	V <sub>IL</sub> = 0	-	-	1	μA
I <sub>LH</sub>	HIGH-level leakage current	V <sub>IH</sub> = V <sub>DD(INTF)</sub>	-	-	5	μA
OFFN output (pin OFFN is an NMOS drain with a kΩ pull-up resistor to V <sub>DD(INTF)</sub> )						
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 2 mA	0	-	0.3	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = -15 μA	0.75 V <sub>DD(INTF)</sub>	-		V
R <sub>pu</sub>	pull-up resistance		8	10	12	kΩ
Protections and limitations						
T <sub>sd</sub>	shutdown temperature	at die	-	150	-	°C
I <sub>Olim</sub>	output current limit	on pin I/O	-15	-	+15	mA
		on pin CLK	-70	-	+70	mA
		on pin RST	-20	-	+20	mA
		on pin VCC = 5 V or 1.8 V	90	125	160	mA
		on pin VCC = 3 V	90	160	260	mA
I <sub>sd</sub>	shutdown current	on pin VCC = 5 V or 1.8 V	80	115	150	mA
		on pin VCC = 3 V	80	150	250	mA
Timing						
t <sub>act</sub>	activation time	see <a href="#">Figure 8 on page 13</a>	1847	-	3390	μs
t <sub>deact</sub>	deactivation time	see <a href="#">Figure 9 on page 14</a>	35	90	250	μs
t <sub>act</sub>	activation time	time of the window for sending CLK to the card with XTAL1	1992	2690	3653	μs
		t <sub>act(start)</sub> = t3; see <a href="#">Figure 8 on page 13</a> t <sub>act(end)</sub> = t5; see <a href="#">Figure 8 on page 13</a>	2055	2766	3749	μs
t <sub>deb</sub>	debounce time	on pin PRESN	2.96	4.05	5.55	ms

- [1] To meet these specifications, VCC is decoupled to CGND using two ceramic multilayer capacitors of low ESR with both capacitors having a value of 220 nF.
- [2] The transition time and the duty factor definitions are shown in [Figure 12 on page 25](#);  $d = t1/(t1 + t2)$
- [3] PRESN and CMDVCCN are active LOW; RSTIN is active HIGH; for CLKDIV1 and CLKDIV2 see [Table 4](#).
- [4] Capacitance should not vary more than  $\pm 30\%$  compared to nominal value, taking all parameters into account (temperature, process variation, biasing voltage, etc. Non exhaustive list)





## 12. Application information



- (1) Place close to the protected pin with good (low resistive) and straight connection to the main ground
- (2) Place close to the supply pin with good (low resistive) and straight connection to GNDP
- (3) Place close to TDA8035's VCC pin with good connection to GNDC
- (4) Place close to card connector's C1 (VCC) pin with good connection to GNDC
- (5) Optional bridge. If not used, R1 must be 0  $\Omega$  and R2 absent (direct connection to  $V_{DD(INTF)}$ )
- (6) GNDP and GNDC are connected to the main ground with a straight and low resistive connection
- (7) The card connector represented here has a normally closed presence switch
- (8) DC/DC converter capacitance value:  
 If  $VDDP=3.3V$ ,  $C3=C4= 330nF$  &  $C5=1\mu F$   
 If  $VDDP=5.0V$ ,  $C3=C4= 100nF$  &  $C5=1\mu F$

**Fig 13. Application diagram**

13. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads;  
 32 terminals; body 5 x 5 x 0.85 mm

SOT617-7

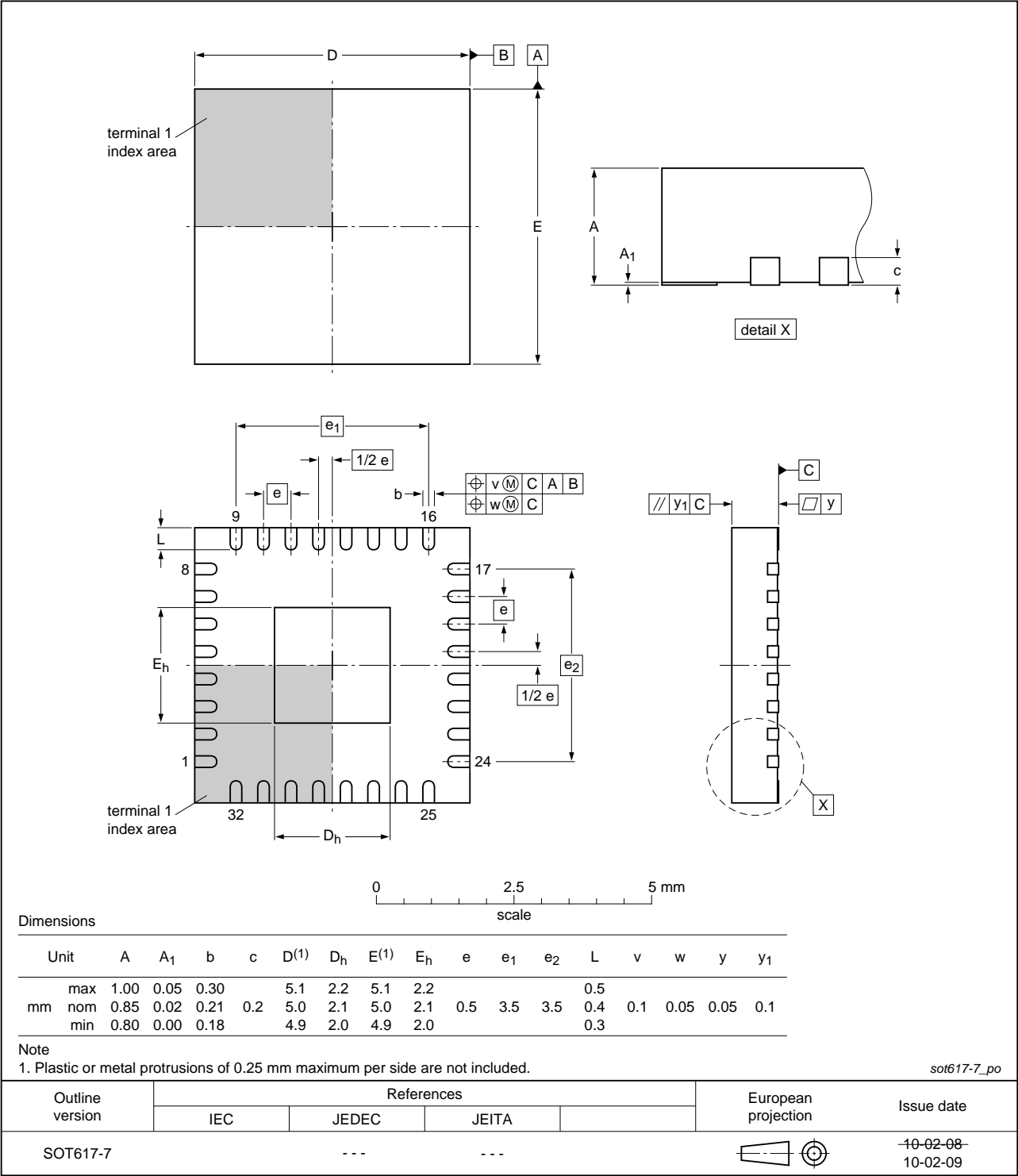


Fig 14. Package outline SOT617-7

## 14. Soldering

For all "Surface mount reflow soldering" information for the SOT617 packaging, utilize the following NXP Semiconductors documentation link:

[http://www.nxp.com/documents/application\\_note/AN10365.pdf](http://www.nxp.com/documents/application_note/AN10365.pdf)

## 15. Abbreviations

Table 8. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge

## 16. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8035HN v. 3.1	20160630	Product data sheet	-	TDA8035HN v. 3.0
Modifications:	<ul style="list-style-type: none"> <li>Addition of C2 Version - EMVCo 4.3 compliant</li> <li><a href="#">Table 7 "Characteristics of IC"</a>: updated</li> </ul>			
TDA8035HN v. 3.0	20140625	Product data sheet	-	TDA8035HN v. 2.1
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 5 "Ordering information"</a>: type TDA8035HN/C1/S1 added</li> <li>Descriptive title changed</li> </ul>			
TDA8035HN v. 2.1	20121203	Product data sheet	-	TDA8035HN v. 2.0
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 3 "Pin description"</a>: updated</li> <li><a href="#">Section 8.1 "Power supply"</a>: updated</li> <li><a href="#">Table 7 "Characteristics of IC"</a>: updated</li> <li><a href="#">Figure 13 "Application diagram"</a>: Table note (7) added</li> </ul>			
TDA8035HN v. 2.0	20111220	Product data sheet	-	TDA8035HN v. 1.1
Modifications:	<ul style="list-style-type: none"> <li>All text updated to NXP standards</li> </ul>			
TDA8035HN v. 1.1	20110706	Product data sheet	-	TDA8035HN v. 1.0
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 7 "Characteristics of IC"</a>: <math>V_{th(L)(PORADJ)}</math> values updated</li> </ul>			
TDA8035HN v. 1.0	20110419	Product data sheet	-	-

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 17.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 17.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the

product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 18. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 19. Tables

Table 1.	Quick reference data	2	Table 6.	Thermal characteristics	17
Table 2.	Ordering information	3	Table 7.	Characteristics of IC	18
Table 3.	Pin description	5	Table 8.	Abbreviations	28
Table 4.	Clock configuration	10	Table 9.	Revision history	28
Table 5.	Limiting values	17			

## 20. Figures

Fig 1.	Block diagram	4
Fig 2.	Pin configuration HVQFN32	5
Fig 3.	Block voltage supervisor	8
Fig 4.	Voltage supervisor	9
Fig 5.	Voltage supervisor	9
Fig 6.	Switch external clock	10
Fig 7.	Shutdown mode and Deep Shutdown mode	12
Fig 8.	Activation sequence at t3	13
Fig 9.	Deactivation sequence	14
Fig 10.	Emergency deactivation sequence (card extraction)	16
Fig 11.	Behavior of OFFN, CMDVCCN, PRESN and V <sub>CC</sub>	16
Fig 12.	Definition of output and input transition times	25
Fig 13.	Application diagram	26
Fig 14.	Package outline SOT617-7	27

## 21. Contents

<b>1</b>	<b>General description</b> . . . . .	<b>1</b>
<b>2</b>	<b>Features and benefits</b> . . . . .	<b>1</b>
2.1	Protection of the contact smart card . . . . .	1
2.2	Easy integration into your contact reader . . . . .	1
2.2.1	Other . . . . .	2
<b>3</b>	<b>Applications</b> . . . . .	<b>2</b>
<b>4</b>	<b>Quick reference data</b> . . . . .	<b>2</b>
<b>5</b>	<b>Ordering information</b> . . . . .	<b>3</b>
<b>6</b>	<b>Block diagram</b> . . . . .	<b>4</b>
<b>7</b>	<b>Pinning information</b> . . . . .	<b>5</b>
7.1	Pinning . . . . .	5
7.2	Pin description . . . . .	5
<b>8</b>	<b>Functional description</b> . . . . .	<b>7</b>
8.1	Power supply . . . . .	7
8.2	Voltage supervisor . . . . .	8
8.3	Clock circuitry . . . . .	10
8.4	I/O circuitry . . . . .	11
8.5	CS control . . . . .	12
8.6	Shutdown mode and Deep Shutdown mode . . . . .	12
8.7	Activation sequence . . . . .	13
8.8	Deactivation sequence . . . . .	14
8.9	V <sub>CC</sub> regulator . . . . .	14
8.10	Fault detection . . . . .	15
<b>9</b>	<b>Limiting values</b> . . . . .	<b>17</b>
<b>10</b>	<b>Thermal characteristics</b> . . . . .	<b>17</b>
<b>11</b>	<b>Characteristics</b> . . . . .	<b>18</b>
<b>12</b>	<b>Application information</b> . . . . .	<b>26</b>
<b>13</b>	<b>Package outline</b> . . . . .	<b>27</b>
<b>14</b>	<b>Soldering</b> . . . . .	<b>28</b>
<b>15</b>	<b>Abbreviations</b> . . . . .	<b>28</b>
<b>16</b>	<b>Revision history</b> . . . . .	<b>28</b>
<b>17</b>	<b>Legal information</b> . . . . .	<b>29</b>
17.1	Data sheet status . . . . .	29
17.2	Definitions . . . . .	29
17.3	Disclaimers . . . . .	29
17.4	Trademarks . . . . .	30
<b>18</b>	<b>Contact information</b> . . . . .	<b>30</b>
<b>19</b>	<b>Tables</b> . . . . .	<b>31</b>
<b>20</b>	<b>Figures</b> . . . . .	<b>31</b>
<b>21</b>	<b>Contents</b> . . . . .	<b>32</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2016.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 30 June 2016

Document identifier: TDA8035