



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only, and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Input Voltage.....-0.3V to 30V
 LX.....-2V to 30V
 FB.....-0.3V to 5.5V
 Storage Temperature.....-65 °C to 150 °C
 Junction Temperature.....-40°C to 125°C
 Lead Temperature (Soldering, 10 sec).....300 °C
 ESD Rating.....1kV LX, 2kV all other nodes, HBM

ELECTRICAL SPECIFICATIONS

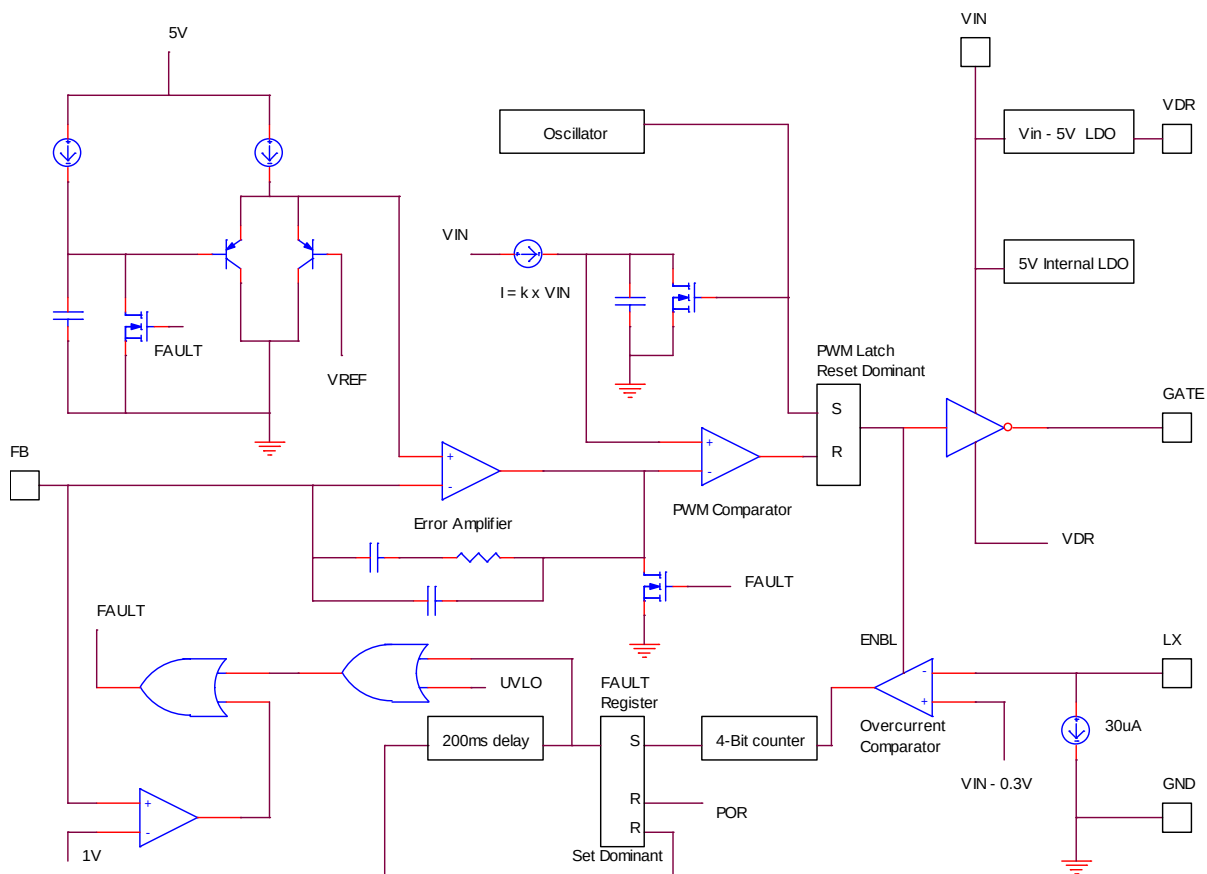
Specifications are for $T_{AMB}=T_J=25^{\circ}\text{C}$, and those denoted by ♦ apply over the full operating range, $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$. Unless otherwise specified: $V_{IN}=4.5\text{V}$ to 29V , $C_{IN}=4.7\mu\text{F}$.

PARAMETER	MIN	TYP	MAX	UNITS	♦	CONDITIONS
UVLO Turn-On Threshold	4.2	4.35	4.5	V		$0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$
UVLO Turn-Off Threshold	4.0	4.2	4.4	V		$0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$
UVLO Hysteresis		0.2		V		
Operating Input Voltage Range	4.5		29	V		$0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$
Operating Input Voltage Range	7		29	V	♦	
Operating VCC Current		0.3	3	mA		$V_{FB}=1.2\text{V}$
Reference Voltage Accuracy		0.5		%		
Reference Voltage Accuracy		0.5	2	%	♦	
Reference Voltage		0.6		V		
Reference Voltage	0.588	0.6	0.612	V	♦	
Switching Frequency	510	600	690	kHz		
Peak-to-peak ramp Modulator		$V_{IN}/5$		V		
Minimum ON-Time Duration		40	100	ns	♦	
Minimum Duty Cycle			0	%		
Maximum Duty Cycle	100			%		
Gate Driver Turn-Off Resistance		50	60	kΩ		Internal resistor between GATE and V_{IN}
Gate Driver Pull-Down Resistance		4	8	Ω		$V_{IN}=12\text{V}$, $V_{FB}=0.5\text{V}$, Measure resistance between GATE and VDR
Gate Driver Pull-up Resistance		3	6	Ω		$V_{IN}=12\text{V}$, $V_{FB}=0.7\text{V}$, Measure resistance between GATE and V_{IN}
V_{IN} - VDR voltage difference	4.5		5.5	V	♦	Measure V_{IN} - VDR, $V_{IN}>7\text{V}$
Overcurrent Threshold	270	300	330	mV		Measure V_{IN} - LX
LX pin Input Current	25	30	35	uA		$V_{LX} = V_{IN}$
OFF interval during hiccup		100		ms		
Soft start time	3	5	9	ms		$V_{FB}=0.58\text{V}$, measure between $V_{IN}=4.5\text{V}$ and first GATE pulse
SHDN Threshold	0.9	1.0	1.1	V	♦	Apply voltage to FB
SHDN Threshold Hysteresis		100		mV		

PIN DESCRIPTION

PIN #	PIN NAME	DESCRIPTION
1	V _{IN}	Input power supply for the controller. Place input decoupling capacitor as close as possible to this pin.
2	GATE	Connect to the gate terminal of the external P-channel MOSFET.
3	V _{DR}	Power supply for the internal driver. This voltage is internally regulated to about 5V below V _{IN} . Place a 0.1uF decoupling capacitor between V _{DR} and V _{IN} as close as possible to the IC.
4	FB	Regulator feedback input. Connect to a resistive voltage-divider network to set the output voltage. This pin can be also used for ON/OFF control. If this pin is pulled above 1V the P-channel driver is disabled and controller resets internal soft start circuit.
5	GND	Ground pin.
6	LX	This pin is used as a current limit input for the internal current limit comparator. Connect to the drain pin of the external MOSFET through an optional resistor. Internal threshold is pre-set to 300mV nominal and can be decreased by changing the external resistor based on the following formula: $V_{TRSHLD} = 300\text{mV} - 30\mu\text{A} \times R$

BLOCK DIAGRAM



The SP6126 is a fixed frequency, voltage-mode, non-synchronous PWM controller optimized for minimum component, small form factor and cost effectiveness. It has been designed for single-supply operation ranging from 4.5V to 29V. SP6126 has Type-II internal compensation for use with Electrolytic/Tantalum output capacitors. For ceramic capacitors Type-III compensation can be implemented by simply adding an R and C between output and Feedback. A precision 0.6V reference, present on the positive terminal of the Error Amplifier, permits programming of the output voltage down to 0.6V via the FB pin. The output of the Error Amplifier is internally compared to a feed-forward ($V_{IN}/5$ peak-to-peak) ramp and generates the PWM control. Timing is governed by an internal oscillator that sets the PWM frequency at 600kHz.

SP6126 contains useful protection features. Over-current protection is based on high-side MOSFET's $R_{ds(on)}$ and is programmable via a resistor placed at LX node. Under-Voltage Lock-Out (UVLO) ensures that the controller starts functioning only when sufficient voltage exists for powering IC's internal circuitry.

SP6126 Loop Compensation

The SP6126 includes Type-II internal compensation components for loop compensation. External compensation components are not required for systems with tantalum or aluminum electrolytic output capacitors with sufficiently high ESR. Use the condition below as a guideline to determine whether or not the internal compensation is sufficient for your design.

Type-II internal compensation is sufficient if the following condition is met:

$$f_{ESRZERO} < f_{DBPOLE} \dots\dots\dots (1)$$

where:

$$f_{ESRZERO} = \frac{1}{2\pi \cdot R_{ESR} \cdot C_{OUT}} \dots\dots\dots (2)$$

$$f_{DBPOLE} = \frac{1}{2\pi \cdot \sqrt{L} \cdot C_{OUT}} \dots\dots\dots (3)$$

Creating a Type-III compensation Network

The above condition requires the ESR zero to be at a lower frequency than the double-pole from the LC filter. If this condition is not met, Type-III compensation should be used and can be accomplished by placing a series RC combination in parallel with R1 as shown below. The value of CZ can be calculated as follows and RZ selected from table 1.

$$CZ = \frac{\sqrt{L \cdot C}}{R1} \dots\dots\dots (4)$$

$f_{ESRZERO} \div f_{DBPOLE}$	RZ
1X	50KΩ
2X	40KΩ
3X	30KΩ
5X	10KΩ
$\geq 10X$	2KΩ

Table1- Selection of RZ

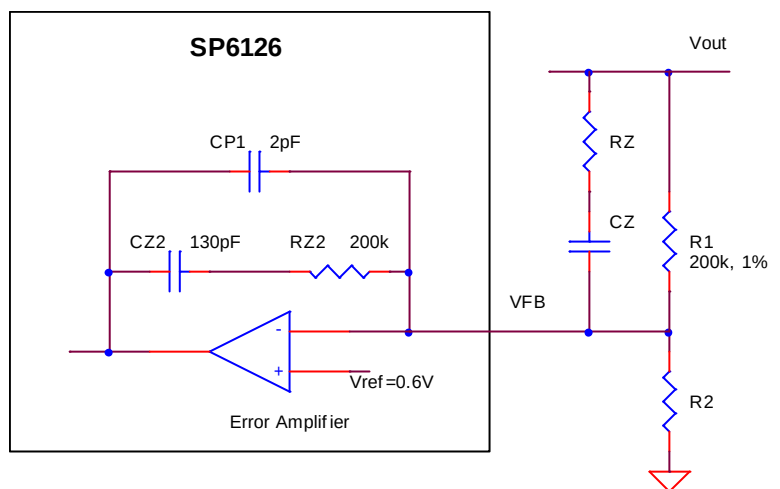


Figure 1- RZ and CZ in conjunction with internal compensation components form a Type-III compensation

Loop Compensation Example 1- A converter utilizing a SP6126 has a 6.8uH inductor and a 22uF/5mΩ ceramic capacitor. Determine whether Type-III compensation is needed.

From equation (2) $f_{\text{ESRZERO}} = 1.45\text{MHz}$. From equation (3) $f_{\text{DBPOLE}} = 13\text{ kHz}$. Since the condition specified in (1) is not met, Type-III compensation has to be used by adding external components RZ and CZ. Using equation (4) CZ is calculated 61.2pF (use 62 pF). Following the guideline given in table 1, a 2kΩ RZ should be used.

The steps followed in example 1 were used to compensate the typical application circuit shown on page 1. Satisfactory frequency response of the circuit, seen in figure 2, validates the above procedure.

Loop Compensation Example 2- A converter utilizing a SP6126 has a 6.8uH inductor and a 150uF, 82mΩ Aluminum Electrolytic capacitor. Determine whether Type-III compensation is needed.

From equation (2) $f_{\text{ESRZERO}} = 13\text{kHz}$. From equation (3) $f_{\text{DBPOLE}} = 5\text{ kHz}$. Since the condition specified in (1) is not met, Type-III compensation has to be used by adding external components RZ and CZ. Using equation (4) CZ is calculated 160pF (use 150 pF). Since $f_{\text{ESRZERO}} \div f_{\text{DBPOLE}}$ is approximately 3, RZ has to be set at 30kΩ.

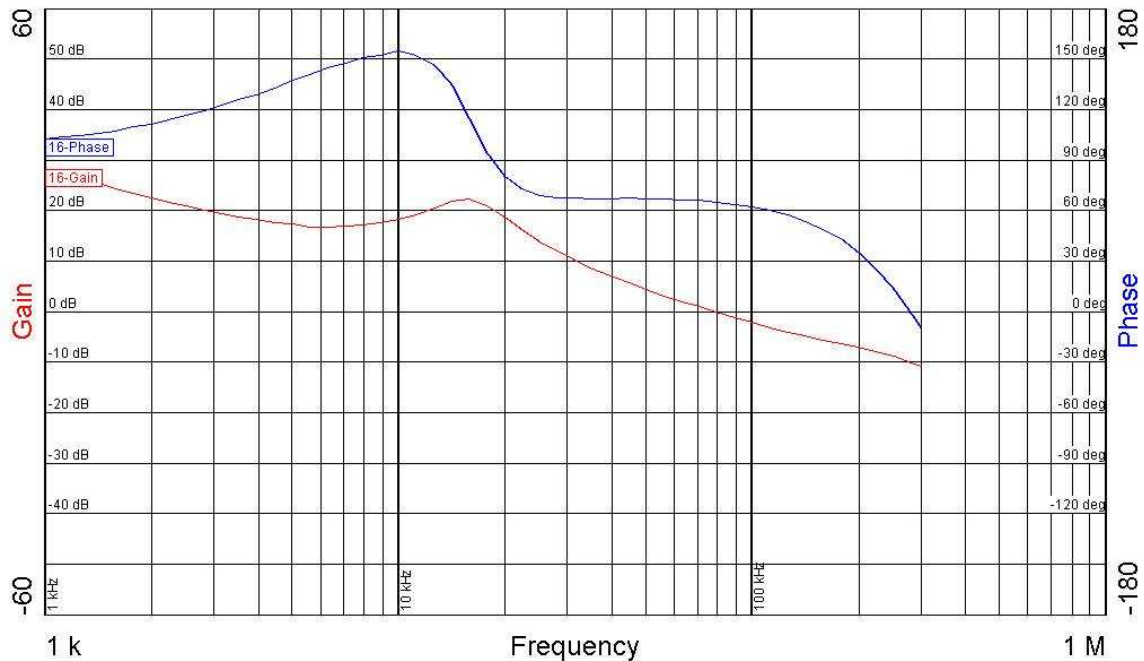


Figure 2- Satisfactory frequency response of typical application circuit shown on page 1. Crossover frequency f_c is 80kHz with a corresponding phase margin of 65 degrees.

Overcurrent Protection

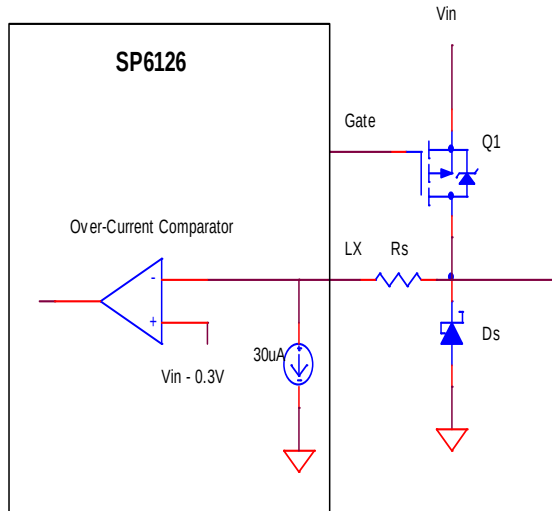


Figure 3- Overcurrent protection circuit

The overcurrent protection circuit functions by monitoring the voltage across the high-side FET Q1. When this voltage exceeds 0.3V, the overcurrent comparator triggers and the controller enters hiccup mode. For example if Q1 has $R_{ds(on)}=0.1\Omega$, then the overcurrent will trigger at $I = 0.3V/0.1\Omega=3A$. To program a lower overcurrent use a resistor R_s as shown in figure 1. Calculate R_s from:

$$R_s = \frac{0.3 - (1.15 \times I_{out} \times R_{ds(on)})}{30\mu A} \dots\dots\dots (5)$$

The overcurrent circuit triggers at peak current through Q1 which is usually about 15% higher than average output current. Hence the multiplier 1.15 is used in (5).

Example: A switching MOSFET used with SP6126 has $R_{ds(on)}$ of 0.1Ω . Program the over-current circuit so that maximum output is 2A.

$$R_s = \frac{0.3 - (1.15 \times 1A \times 0.1\Omega)}{30\mu A}$$

$$R_s = 2333\Omega$$

Using the above equation there is good agreement between calculated and test results when an R_s in the range of 0.5k to 3k is used. For R_s larger than 3k test results are lower than those predicted by (5), due to circuit parasitics.

Using the ON/OFF Function

Feedback pin serves a dual role of ON/OFF control. The MOSFET driver is disabled when a voltage greater than 1V is applied at FB pin. Maximum voltage rating of this pin is 5.5V. The controlling signal should be applied through a small signal diode as shown on page 1. *Please note that an optional 10k Ω bleeding resistor across the output helps keep the output capacitor discharged under no load condition.*

Programming the Output Voltage

To program the output voltage, calculate R_2 using the following equation:

$$R_2 = \frac{R_1}{\left(\frac{V_{out}}{V_{ref}} - 1\right)}$$

Where: $V_{ref}=0.6$ is the reference voltage of the SP6126

$R_1=200k\Omega$ is a fixed-value resistor that, in addition to being a voltage divider, it is part of the compensation network. In order to simplify compensation calculations, R_1 is fixed at 200k Ω .

Soft Start

Soft Start is preset internally to 5ms (nominal). Internal Soft Start eliminates the need for the external capacitor C_{SS} that is commonly used to program this function.

MOSFET Gate Drive

P-channel drive is derived through an internal regulator that generates $V_{IN}=5V$. This pin (VDR) has to be connected to V_{IN} with a 0.1 μF decoupling capacitor. The gate drive circuit swings between V_{IN} and $V_{IN}-5$ and employs powerful drivers for efficient switching of the P-channel MOSFET.

Power MOSFET Selection

Select the Power MOSFET for Voltage rating BV_{DSS} , On resistance $R_{DS(ON)}$, and thermal resistance R_{thja} . BV_{DSS} should be about twice as high as V_{IN} in order to guard against switching transients. Recommended MOSFET voltage rating for V_{IN} of 5V, 12V and 24V is 12V, 30V and 40V respectively. $R_{DS(ON)}$ has to be selected such that when operating at peak current and junction temperature the Overcurrent threshold of the SP6126 is not exceeded. Allowing 50% for temperature coefficient of $R_{DS(ON)}$ and 15% for inductor current ripple, the following expression can be used:

$$R_{DS(ON)} \leq \left(\frac{300mV}{1.5 \times 1.15 \times I_{out}} \right)$$

Within this constraint, selecting MOSFETs with lower $R_{DS(ON)}$ will reduce conduction losses at the expense of increased switching losses. As a rule of thumb select the highest $R_{DS(ON)}$ MOSFET that meets the above criteria. Switching losses can be assumed to roughly equal the conduction losses. A simplified expression for conduction losses is given by:

$$P_{cond} = I_{out} \times R_{DS(ON)} \times \left(\frac{V_{out}}{V_{in}} \right)$$

MOSFET's junction temperature can be estimated from:

$$T = (2 \times P_c \times R_{thja}) + T_{ambient}$$

Schottky Rectifier selection

Select the Schottky for Voltage rating V_R , Forward voltage V_f , and thermal resistance R_{thja} . Voltage rating should be selected using the same guidelines outlined for MOSFET voltage selection. For a low duty cycle application such as the circuit shown on first page, the Schottky is conducting most of the time and its conduction losses are the largest component of losses in the converter. Conduction losses can be estimated from:

$$P_c = V_f \times I_{out} \times \left(1 - \frac{V_{out}}{V_{in}} \right)$$

where:

V_f is diode forward voltage at I_{OUT}

Schottky's AC losses due to its switching capacitance are negligible.

Inductor Selection

Select the Inductor for inductance L and saturation current I_{SAT} . Select an inductor with I_{SAT} higher than the programmed overcurrent. Calculate inductance from:

$$L = (V_{in} - V_{out}) \times \left(\frac{V_{out}}{V_{in}} \right) \times \left(\frac{1}{f} \right) \times \left(\frac{1}{I_{rip}} \right)$$

where:

V_{IN} is converter input voltage

V_{OUT} is converter output voltage

f is switching frequency

I_{RIP} is inductor peak-to-peak current ripple (nominally set to 30% of I_{OUT})

Keep in mind that a higher I_{RIP} results in a smaller inductor which has the advantages of small size, low DC equivalent resistance DCR, high saturation current I_{SAT} and allows the use of a lower output capacitance to meet a given step load transient. A higher I_{RIP} , however, increases the output voltage ripple and increases the current at which converter enters Discontinuous Conduction Mode. The output current at which converter enters DCM is $\frac{1}{2}$ of I_{RIP} . Note that a negative current step load that drives the converter into DCM will result in a large output voltage transient. Therefore the lowest current for a step load should be larger than $\frac{1}{2}$ of I_{RIP} .

Output Capacitor Selection

Select the output capacitor for voltage rating, capacitance and Equivalent Series Resistance (ESR). Nominally the voltage rating is selected to be twice as large as the output voltage. Select the capacitance to satisfy the specification for output voltage overshoot/undershoot caused by current step load. A steady-state output current I_{OUT} corresponds to inductor stored energy of $\frac{1}{2} L I_{OUT}^2$.

A sudden decrease in I_{OUT} forces the energy surplus in L to be absorbed by C_{OUT} . This causes an overshoot in output voltage that is corrected by power switch reduced duty cycle. Use the following equation to calculate C_{OUT} :

$$C_{out} = L \times \left(\frac{I_2^2 - I_1^2}{V_{os}^2 - V_{out}^2} \right)$$

Where:

L is the output inductance

I_2 is the step load high current

I_1 is the step load low current

V_{os} is output voltage including overshoot

V_{OUT} is steady state output voltage

Output voltage undershoot calculation is more complicated. Test results for SP6126 buck circuits show that undershoot is approximately equal to overshoot. Therefore above equation provides a satisfactory method for calculating C_{OUT} .

Select ESR such that output voltage ripple (VRIP) specification is met. There are two components to VRIP: First component arises from charge transferred to and from C_{OUT} during each cycle. The second component of VRIP is due to inductor ripple current flowing through output capacitor's ESR. It can be calculated from:

$$V_{rip} = I_{rip} \times \sqrt{ESR^2 + \left(\frac{1}{8 \times C_{out} \times f_s} \right)^2}$$

Where:

I_{RIP} is inductor ripple current

f_s is switching frequency

C_{OUT} is output capacitor calculated above

Note that a smaller inductor results in a higher I_{RIP} , therefore requiring a larger C_{OUT} and/or lower ESR in order to meet VRIP.

Input Capacitor Selection

Select the input capacitor for Voltage, Capacitance, ripple current, ESR and ESL. Voltage rating is nominally selected to be twice the input voltage. The RMS value of input capacitor current, assuming a low inductor ripple current (I_{RIP}), can be calculated from:

$$I_{cin} = I_{out} \times \sqrt{D(1-D)}$$

In general total input voltage ripple should be kept below 1.5% of V_{IN} (not to exceed 180mV). Input voltage ripple has three components: ESR and ESL cause a step voltage drop upon turn on of the MOSFET. During on time capacitor discharges linearly as it supplies $I_{OUT-lin}$. The contribution to Input voltage ripple by each term can be calculated from:

$$\Delta V, Cin = \frac{I_{out} \times V_{out} \times (V_{in} - V_{out})}{f_s \times C_{in} \times V_{in}^2}$$

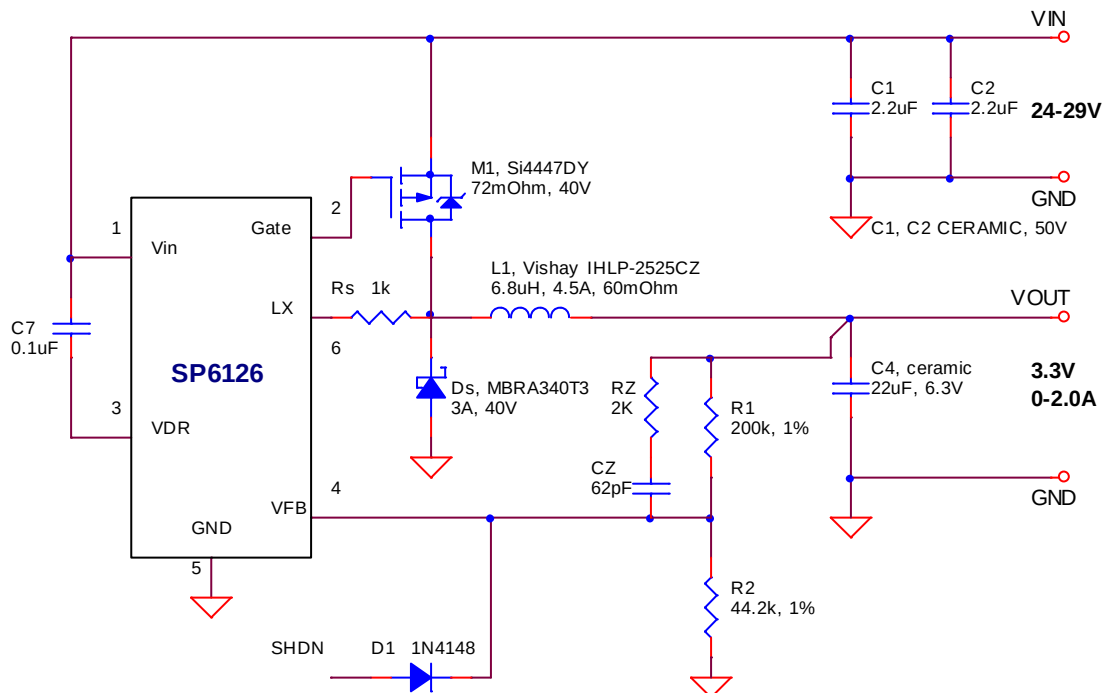
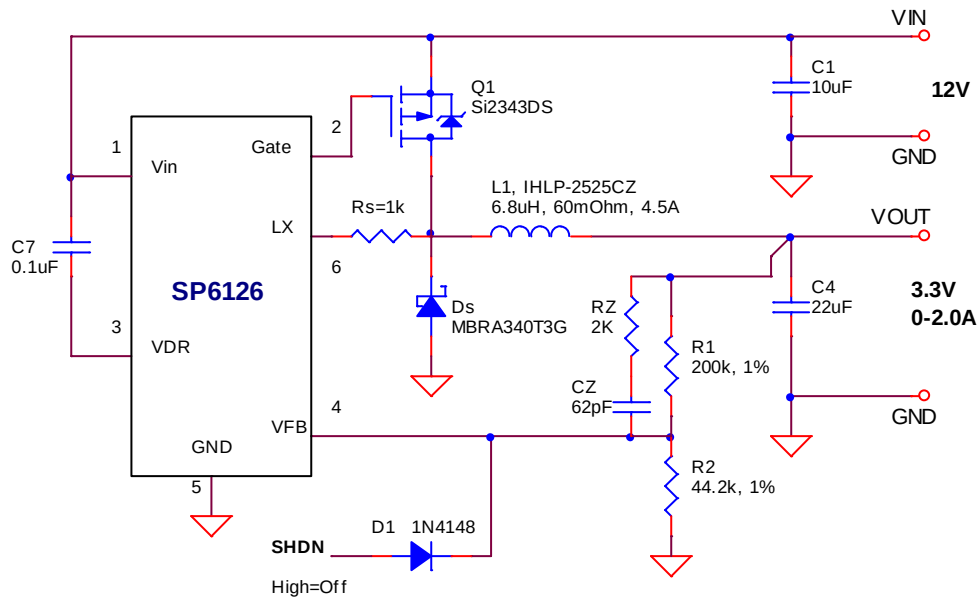
$$\Delta V, ESR = ESR(I_{out} - 0.5I_{rip})$$

$$\Delta V, ESL = ESL \frac{(I_{out} - 0.5I_{rip})}{Trise}$$

Where $Trise$ is the rise time of current through capacitor

Total input voltage ripple is sum of the above:

$$\Delta V, Tot = \Delta V, Cin + \Delta V, ESR + \Delta V, ESL$$



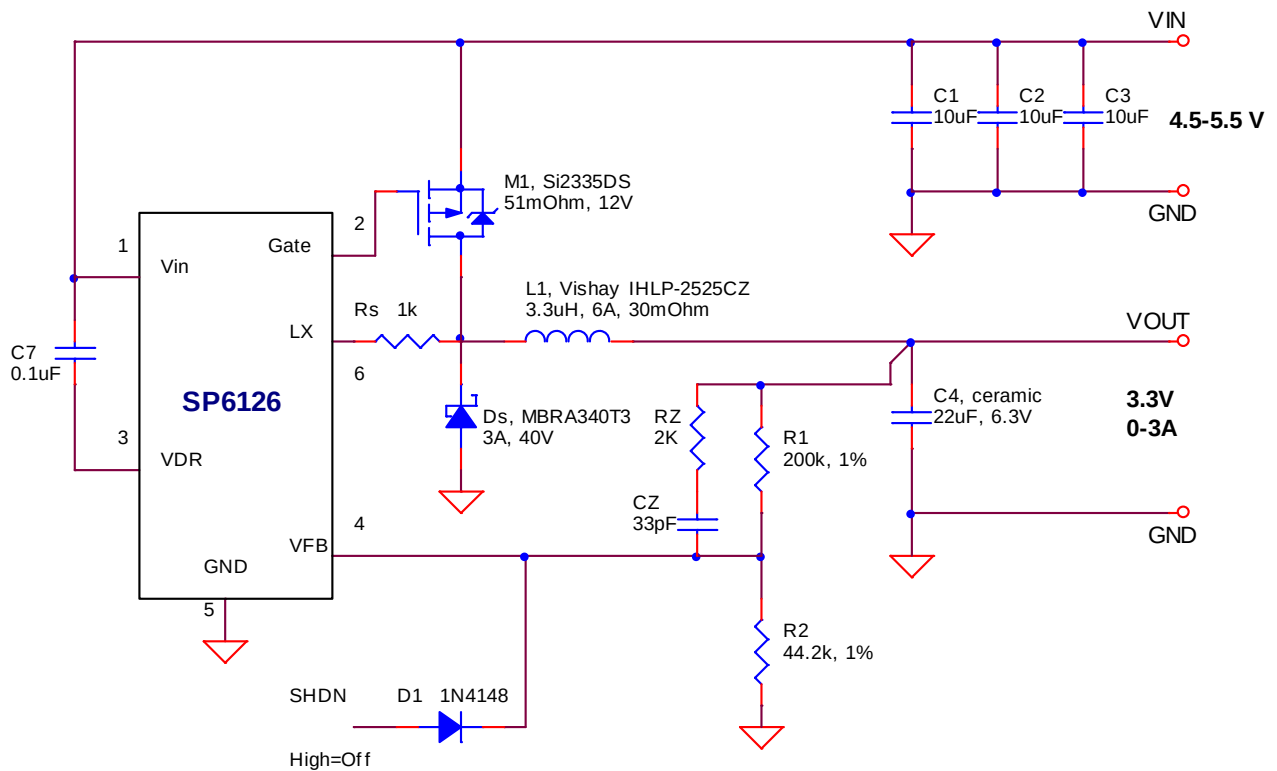


Figure 6- Application circuit for $V_{OUT} = 4.5-5.5\text{ V}$

TYPICAL PERFORMANCE CHARACTERISTICS

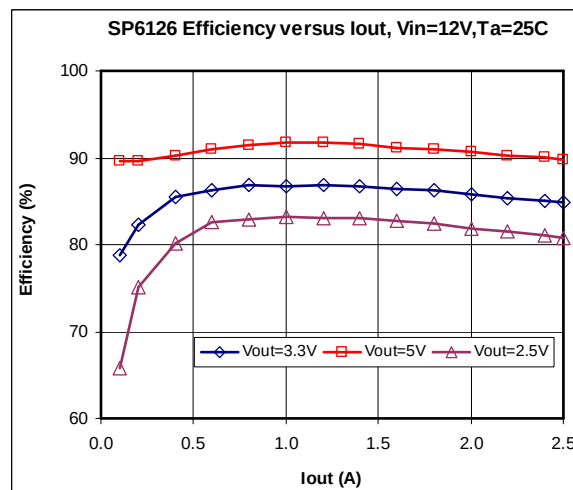


Figure 7- Efficiency at $V_{IN} = 12\text{ V}$

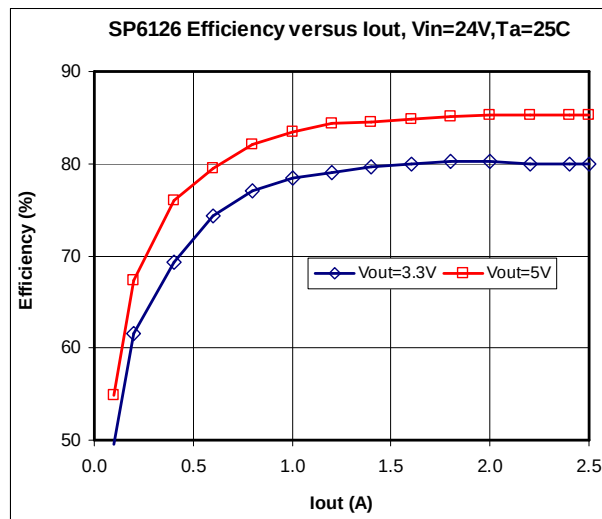


Figure 8- Efficiency at VIN = 24 V

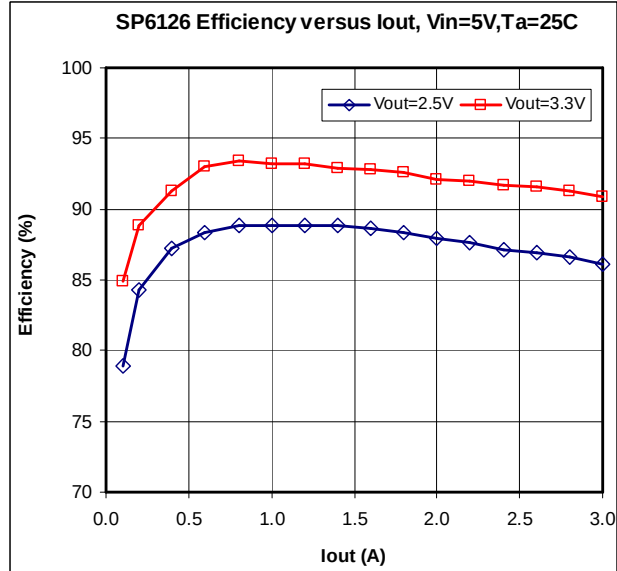
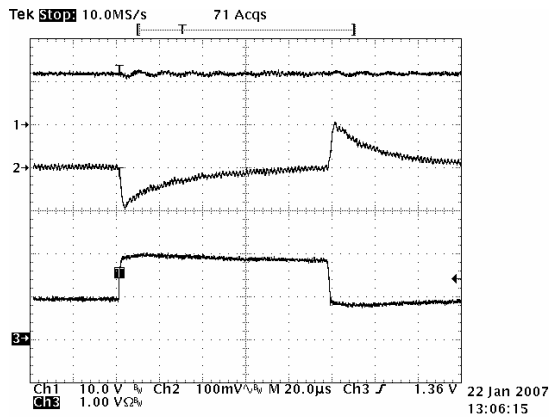


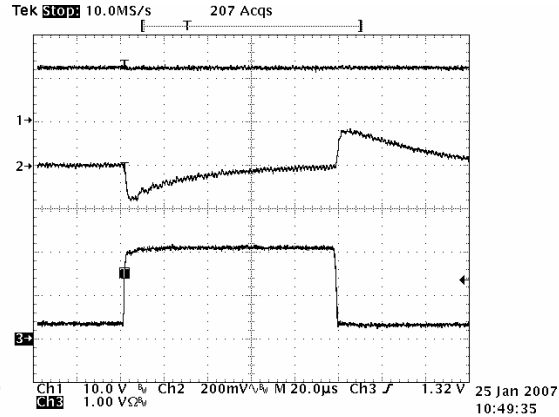
Figure 9- Efficiency at VIN = 5 V



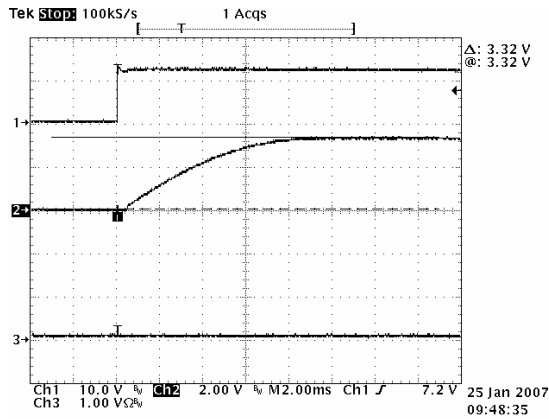
TYPICAL PERFORMANCE CHARACTERISTICS



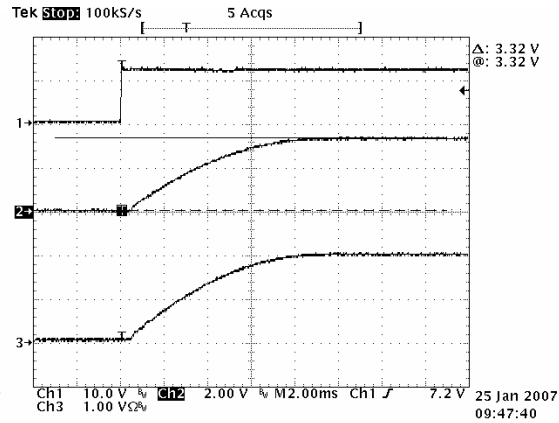
**Figure 10- Step load 1-2A,
ch1: VIN; ch2: VOUT; ch3: IOUT**



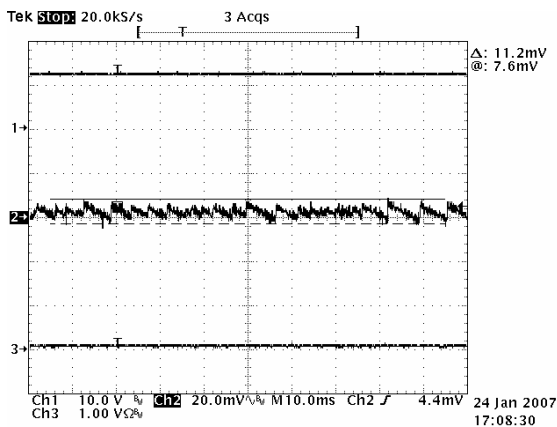
**Figure 11- Step load 0.3-2A,
ch1: VIN; ch2: VOUT; ch3: IOUT**



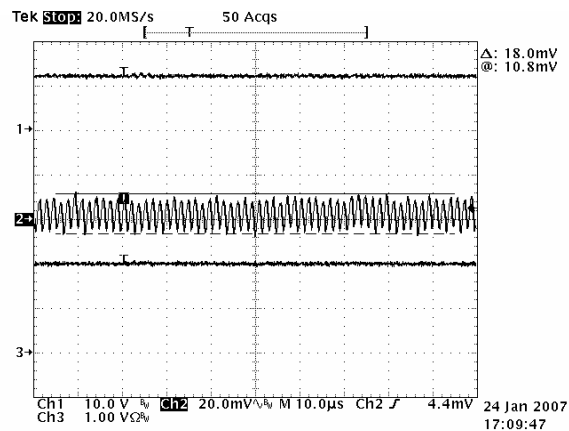
**Figure 12- Startup no load,
ch1: VIN ch2: VOUT, ch3: IOUT**



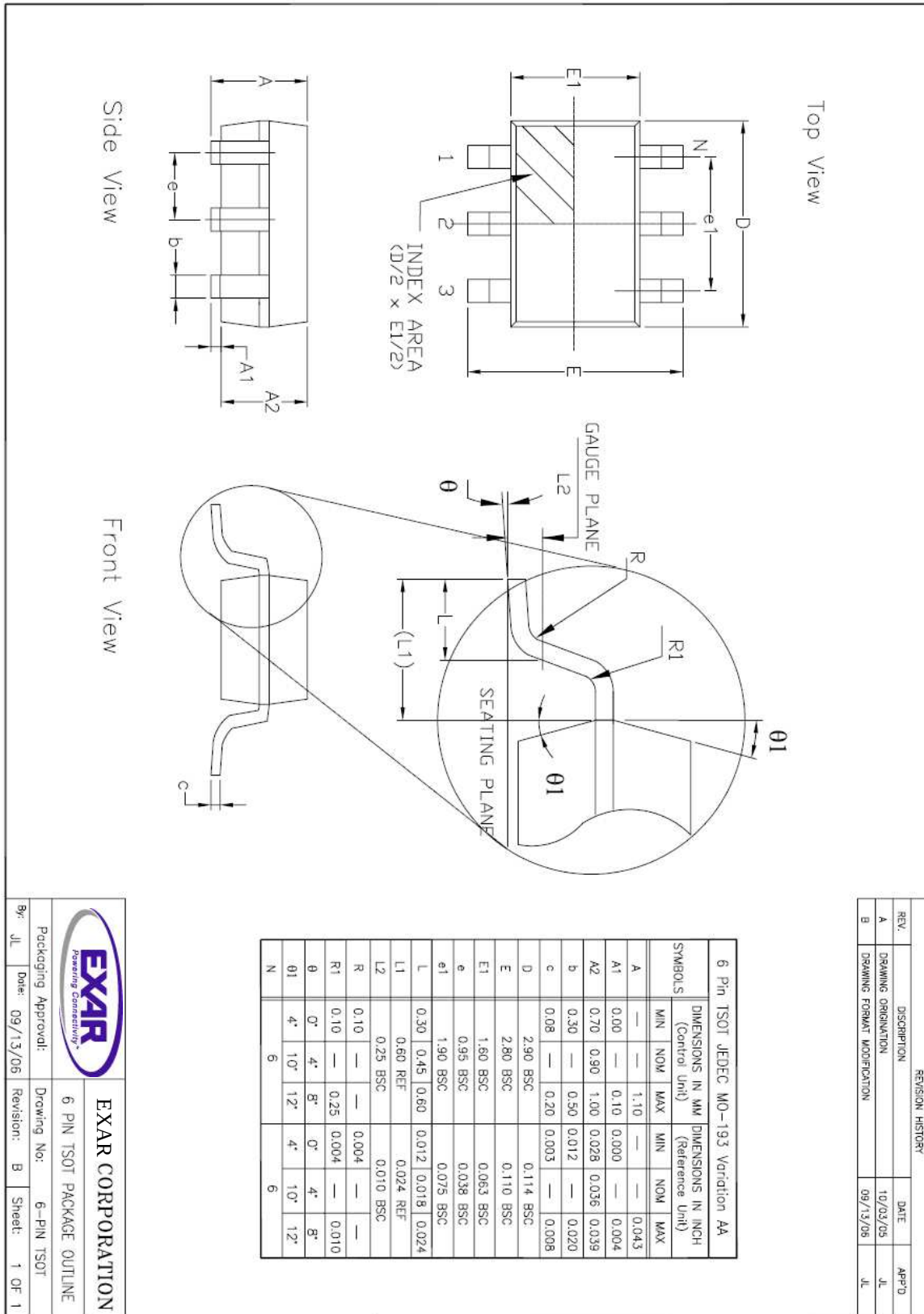
**Figure 13- Start up 2A,
ch1: VIN; ch2: VOUT; ch3: IOUT**



**Figure 14- Output ripple at 0A is 11mV,
ch1: VIN; ch2: VOUT; ch3: IOUT**



**Figure 15- Output ripple at 2A is 18mV,
ch1: VIN; ch2: VOUT; ch3: IOUT**





ORDERING INFORMATION

Part Number	Temperature Range	Package
SP6126EK1-L.....	-40°C to +125°C.....	(Lead Free) 6 Pin TSOT
SP6126EK1-L/TR.....	-40°C to +125°C.....	(Lead Free) 6 Pin TSOT

/TR = Tape and Reel

Pack Quantity for Tape and Reel is 2500

For further assistance:

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EXAR Technical Documentation: <http://www.exar.com/TechDoc/default.aspx?>



Exar Corporation
Headquarters and
Sales Office
48720 Kato Road
Fremont, CA 94538
main: 510-668-7000
fax: 510-668-7030

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