



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Input Voltage, V_{IN} to GND	–6.0 to 6.5 V
$\overline{V_{SD}}$ (See Detailed Description)	–0.3 V to V_{IN}
Output Current, I_{OUT}	Short Circuit Protected
Output Voltage, V_{OUT}	–0.3 V to $V_{IN} + 0.3$ V
Package Power Dissipation, $(P_d)^b$	440 mW

Package Thermal Resistance, $(\theta_{JA})^a$ 180°C/W

Maximum Junction Temperature, $T_{J(max)}$ 150°C

Storage Temperature, T_{STG} –65°C to 150°C

Notes

a. Device mounted with all leads soldered or welded to PC board.

b. Derate 5.5 mW/°C above $T_A = 70^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Input Voltage, V_{IN} 2 V to 6 V

Input Voltage, $\overline{V_{SD}}$ 0 V to V_{IN}

Operating Ambient Temperature, T_A –40°C to 85°C

$C_{IN} = C_{OUT} = 1 \mu\text{F}$ (ceramic), $C_{BP} = 0.01 \mu\text{F}$ (ceramic)

Maximum ESR of C_{OUT} : 0.4 Ω

SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Specified $T_A = 25^{\circ}\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$ $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$ $V_{SD} = 1.5\text{ V}$	Temp ^a	Limits –40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Start-Up BP Current	I_{OUT}	ON/OFF = High	Room		1		mA
Input Voltage Range	V_{IN}		Full	2		6	V
Output Voltage Accuracy	V_{OUT}	$1\text{ mA} \leq I_{OUT} \leq 150\text{ mA}$	Room	–1.5	1	1.5	%
			Full	–2.5	1	2.5	
Line Regulation ($V_{OUT} \leq 3\text{ V}$)	$\frac{\Delta V_{OUT} \times 100}{\Delta V_{IN} \times V_{OUT(nom)}}$	From $V_{IN} = V_{OUT(nom)} + 1\text{ V}$ to $V_{OUT(nom)} + 2\text{ V}$	Full	–0.06		0.18	% / V
Line Regulation ($3.0\text{ V} < V_{OUT} \leq 3.6\text{ V}$)			Full	0		0.3	
Line Regulation (5-V Version)			Full	0		0.4	
Dropout Voltage ^{d, g} ($V_{OUT(nom)} \geq 2.6\text{ V}$)	$V_{IN} - V_{OUT}$	$I_{OUT} = 1\text{ mA}$	Room		1		mV
		$I_{OUT} = 50\text{ mA}$	Room		45	80	
			Full		50	90	
		$I_{OUT} = 150\text{ mA}$	Room		130	180	
Full					220		
Dropout Voltage ^{d, g} ($V_{OUT(nom)} < 2.6\text{ V}$, $V_{IN} \geq 2\text{ V}$)		$I_{OUT} = 50\text{ mA}$	Room		65	100	
			Full			120	
		$I_{OUT} = 150\text{ mA}$	Room		190	250	
	Full				300		
Ground Pin Current ^{e, g} ($V_{OUT(nom)} \leq 3\text{ V}$)	I_{GND}	$I_{OUT} = 0\text{ mA}$	Room		100	150	μA
			Full			180	
		$I_{OUT} = 150\text{ mA}$	Room		110	200	
			Full			230	
Ground Pin Current ^e ($V_{OUT(nom)} > 3\text{ V}$)		$I_{OUT} = 0\text{ mA}$	Room		110	170	
			Full			200	
		$I_{OUT} = 150\text{ mA}$	Room		120	200	
			Full			230	
Peak Output current	$I_{O(peak)}$	$V_{OUT} \geq 0.95 \times V_{OUT(nom)}$, $t_{PW} = 2\text{ ms}$	Full	300			mA



SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Specified $T_A = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$ $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$ $V_{SD} = 1.5\text{ V}$	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Output Noise Voltage	e_N	$V_{NOM} = 2.6\text{ V}$, BW = 10 Hz to 100 kHz, $0\text{ mA} < I_{OUT} < 150\text{ mA}$, $C_{NOISE} = 0.01\text{ }\mu\text{F}$	Room		30		$\mu\text{V(rms)}$
Ripple Rejection	$\Delta V_{OUT}/\Delta V_{IN}$	$I_{OUT} = 150\text{ mA}$	$f = 1\text{ kHz}$	Room	60		dB
			$f = 10\text{ kHz}$	Room	40		
			$f = 100\text{ kHz}$	Room	30		
Dynamic Line Regulation	$\Delta V_{O(line)}$	$V_{IN} : V_{OUT(nom)} + 1\text{ V}$ to $V_{OUT(nom)} + 2\text{ V}$ $t_r/t_f = 2\text{ }\mu\text{s}$, $I_{OUT} = 150\text{ mA}$	Room		20		mV
Dynamic Load Regulation	$\Delta V_{O(load)}$	$I_{OUT} : 1\text{ mA}$ to 150 mA , $t_r/t_f = 2\text{ }\mu\text{s}$	Room		20		
Thermal Shutdown Junction Temperature	$T_{J(S/D)}$		Room		150		°C
Thermal Hysteresis	T_{HYST}		Room		20		
Reverse current	I_R	$V_{IN} = -6.0\text{ V}$	Room		1		μA
Short Circuit Current	I_{SC}	$V_{OUT} = 0\text{ V}$	Room		700		mA
Shutdown							
Shutdown Supply Current	$I_{CC(off)}$	$V_{SD} = 0\text{ V}$	Room		0.1	1	μA
$\overline{\text{SD}}$ Pin Input Voltage	V_{SD}	High = Regulator ON (Rising)	Full	1.5		V_{IN}	V
		Low = Regulator OFF (Falling)	Full			0.4	
Auto Discharge Resistance	R_{DIS}	Si91841 Only	Room		100		Ω
$\overline{\text{SD}}$ Pin Input Current ^f	$I_{IN(\overline{\text{SD}})}$	$V_{SD} = 1.5\text{ V}$, $V_{IN} = 6\text{ V}$	Room		0.7		μA
$\overline{\text{SD}}$ Hysteresis	$V_{HYST(\overline{\text{SD}})}$		Full		150		mV
V_{OUT} Turn-On Time	t_{ON}	V_{SD} (See Figure 1), $I_{LOAD} = 100\text{ nA}$			50		μs

Notes

- Room = 25°C, Full = -40 to 85°C.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing. Typical values for dropout voltage at $V_{OUT} \geq 2\text{ V}$ are measured at $V_{OUT} = 3.3\text{ V}$, while typical values for dropout voltage at $V_{OUT} < 2\text{ V}$ are measured at $V_{OUT} = 1.8\text{ V}$.
- Dropout voltage is defined as the input to output differential voltage at which the output voltage drops 2% below the output voltage measured with a 1-V differential, provided that V_{IN} does not drop below 2.0 V.
- Ground current is specified for normal operation as well as “drop-out” operation.
- The device’s shutdown pin includes a typical 2-M Ω internal pull-down resistor connected to ground.
- $V_{OUT(nom)}$ is V_{OUT} when measured with a 1-V differential to V_{IN} .

TIMING WAVEFORMS

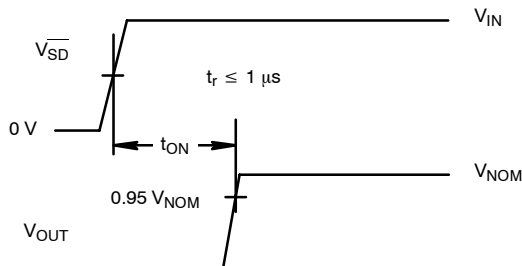
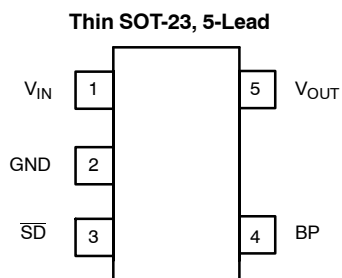


FIGURE 1. Timing Diagram for Power-Up

PIN CONFIGURATION



PIN DESCRIPTION

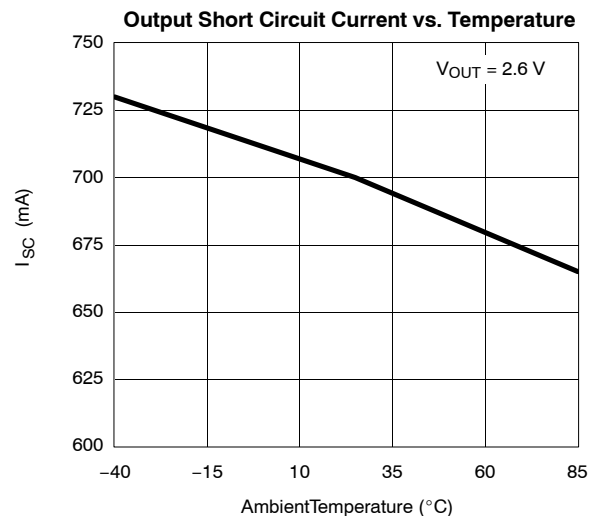
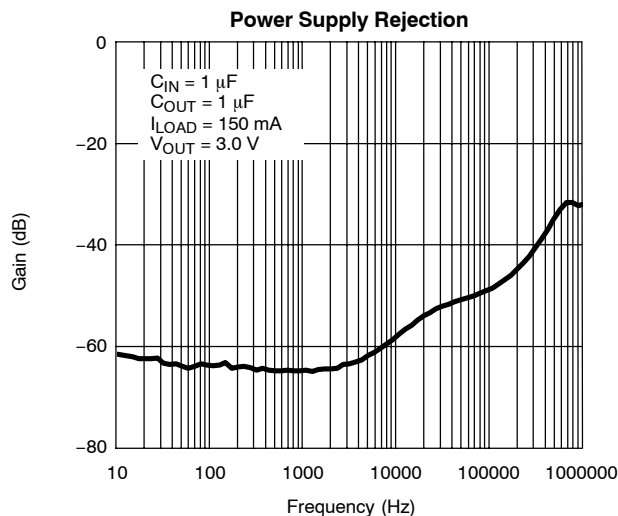
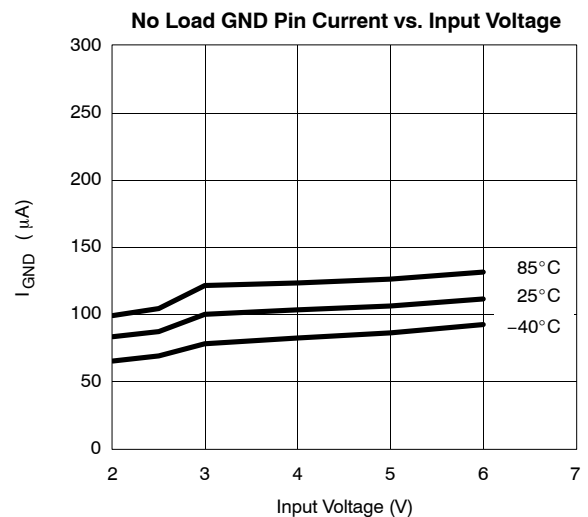
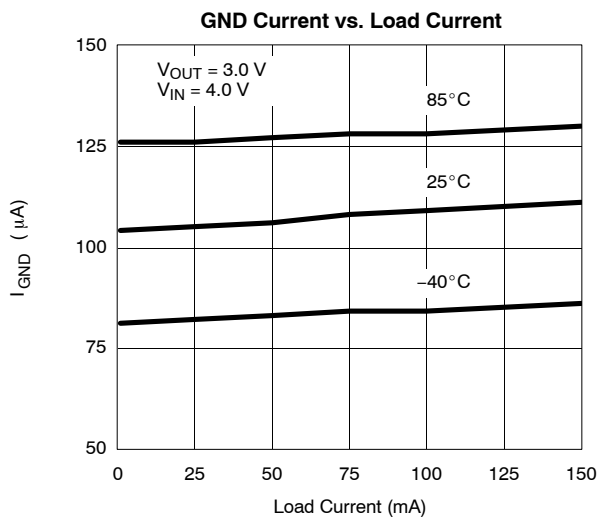
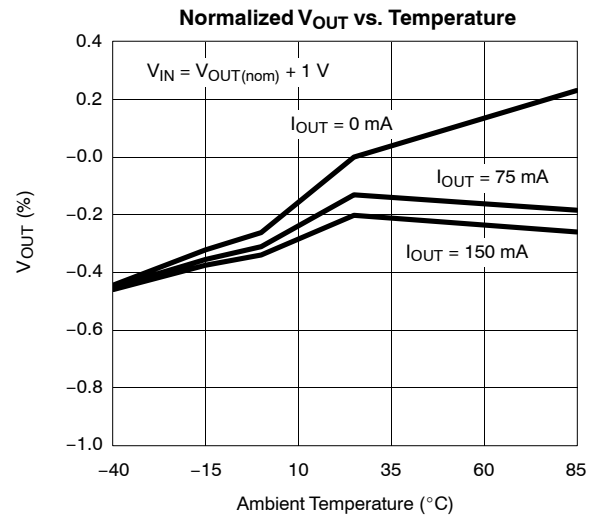
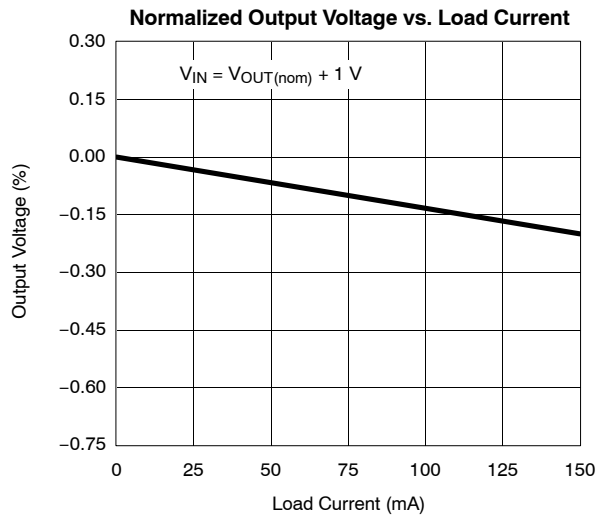
Pin No.	Name	Function
1	V _{IN}	Input supply pin. Bypass this pin with a 1-μF ceramic or tantalum capacitor to ground
2	GND	Ground pin. For better thermal capability, directly connected to large ground plane
3	SD	By applying less than 0.4 V to this pin, the device will be turned off. Connect this pin to V _{IN} if unused
4	BP	Noise bypass pin. For low noise applications, a 0.01 μF ceramic capacitor should be connected from this pin to ground.
5	V _{OUT}	Output voltage. Connect C _{OUT} between this pin and ground.

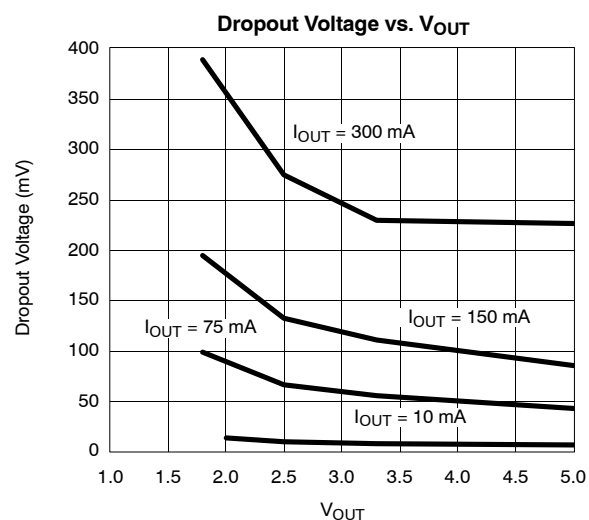
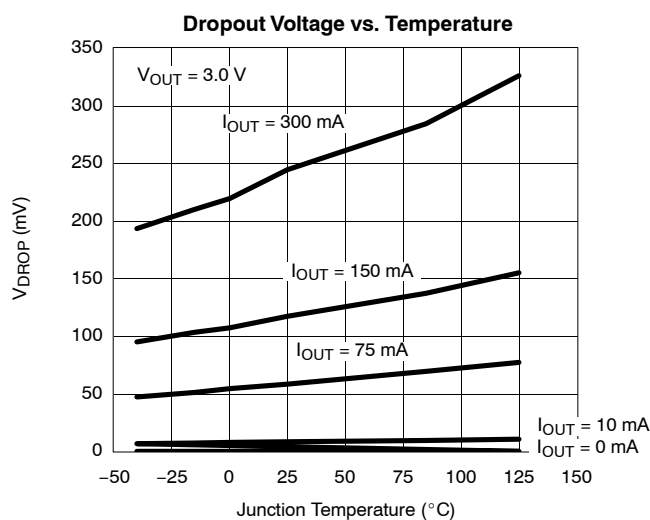
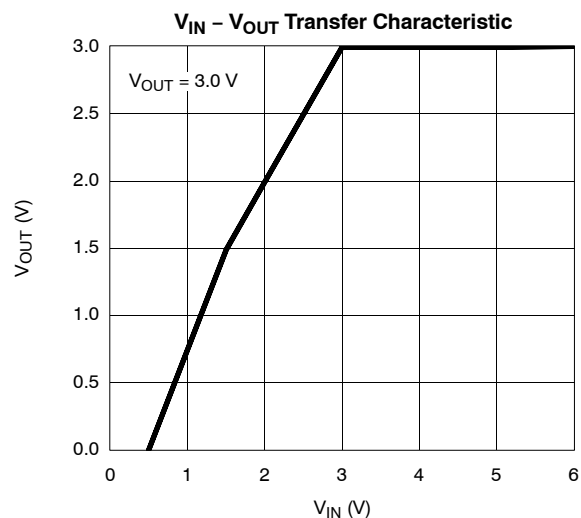
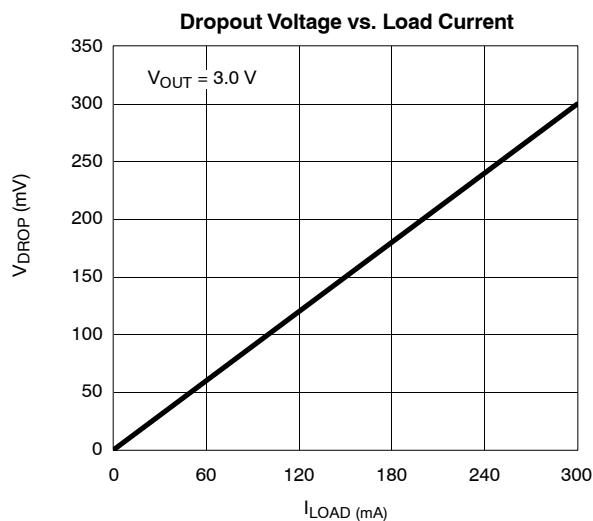
ORDERING INFORMATION—Si91841

Part Number	Lead (Pb)-Free Part Number	Marking	Voltage	Temperature Range	Package
Si91841DT-18-T1	Si91841DT-18-T1—E3	B4LL	1.8	–40 to 85°C	Thin SOT23-5
Si91841DT-25-T1	Si91841DT-25-T1—E3	B7LL	2.5		
Si91841DT-26-T1	Si91841DT-26-T1—E3	B8LL	2.6		
Si91841DT-28-T1	Si91841DT-28-T1—E3	B0LL	2.8		
Si91841DT-285-T1	Si91841DT-285—E3	C1LL	2.85		
Si91841DT-29-T1	Si91841DT-29-T1—E3	C2LL	2.9		
Si91841DT-30-T1	Si91841DT-30-T1—E3	C3LL	3.0		
Si91841DT-33-T1	Si91841DT-33-T1—E3	C4LL	3.3		
Si91841DT-50-T1	Si91841DT-50-T1—E3	C7LL	5.0		

Note: LL = Lot Code

TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)

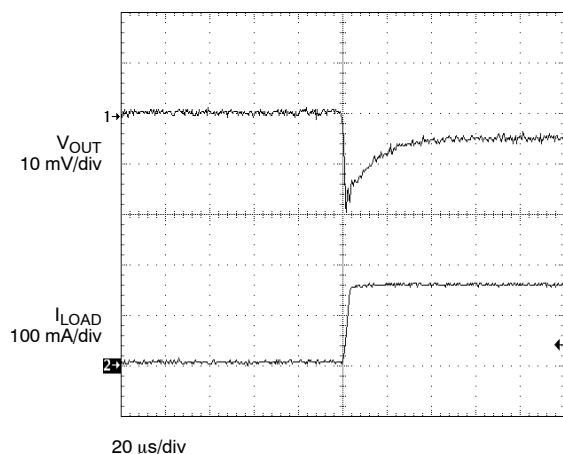


TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)




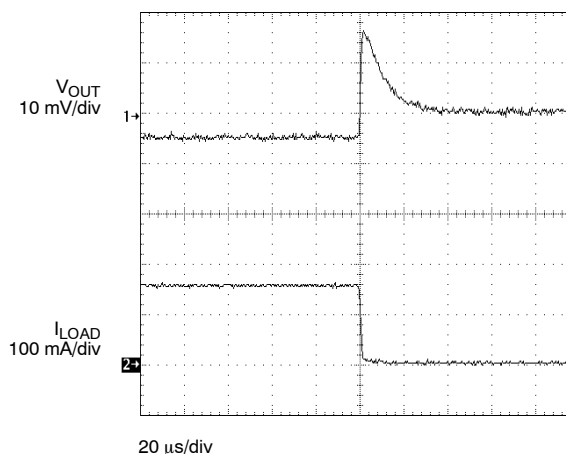
TYPICAL WAVEFORMS

Load Transient Response-1



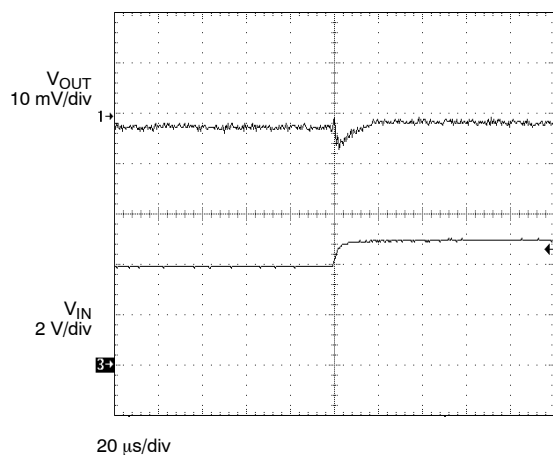
$V_{OUT} = 3.0$ V
 $C_{OUT} = 1$ μ F
 $I_{LOAD} = 1$ to 150 mA
 $t_{rise} = 2$ μ sec

Load Transient Response-2



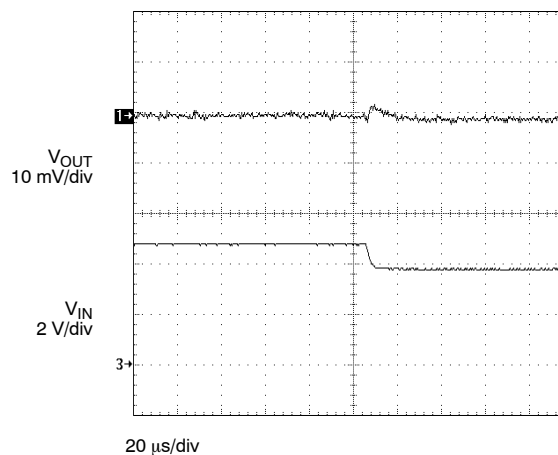
$V_{OUT} = 3.0$ V
 $C_{OUT} = 1$ μ F
 $I_{LOAD} = 150$ to 1 mA
 $t_{fall} = 2$ μ sec

Line Transient Response-1



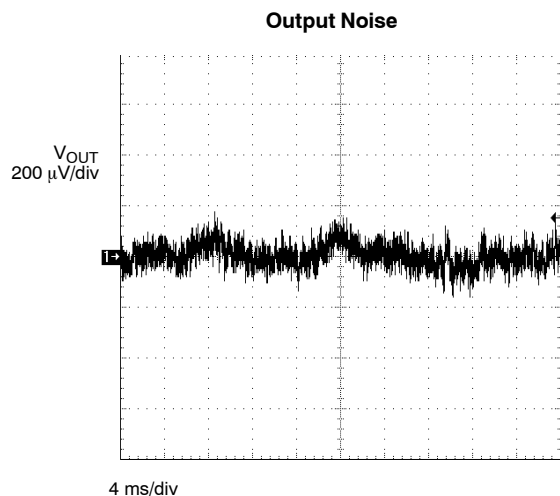
$V_{INSTEP} = 4$ to 5 V
 $V_{OUT} = 3$ V
 $C_{OUT} = 1$ μ F
 $C_{IN} = 1$ μ F
 $I_{LOAD} = 150$ mA
 $t_{rise} = 5$ μ sec

Line Transient Response-2

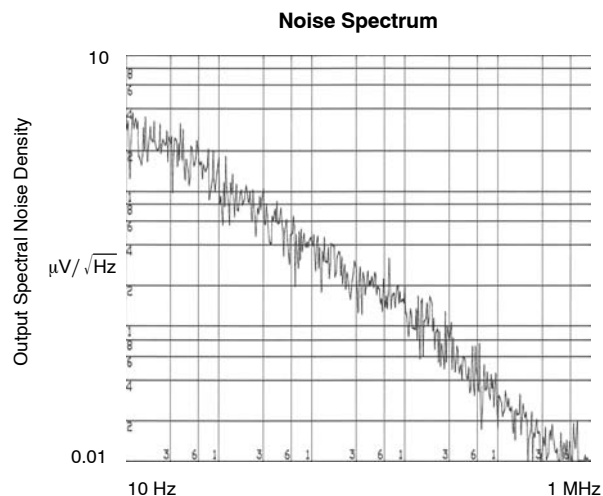


$V_{INSTEP} = 5$ to 4 V
 $V_{OUT} = 3$ V
 $C_{OUT} = 1$ μ F
 $C_{IN} = 1$ μ F
 $I_{LOAD} = 150$ mA
 $t_{fall} = 5$ μ sec

TYPICAL WAVEFORMS

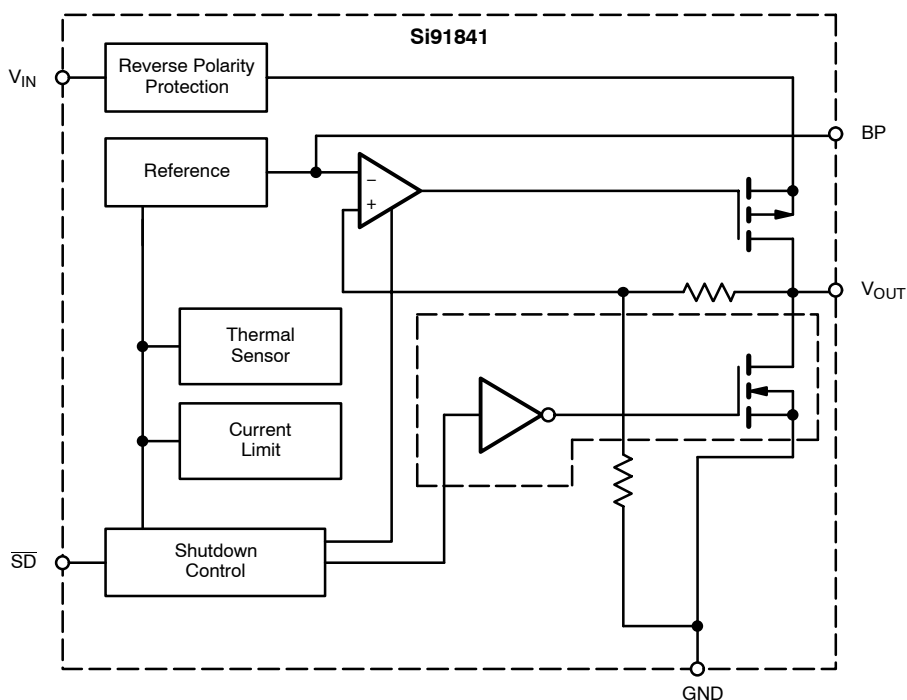


$V_{IN} = 4\text{ V}$
 $V_{OUT} = 3\text{ V}$
 $I_{OUT} = 150\text{ mA}$
 $C_{NOISE} = 0.01\text{ }\mu\text{F}$
 $BW = 10\text{ Hz to }100\text{ kHz}$



$V_{IN} = 4\text{ V}$
 $V_{OUT} = 3\text{ V}$
 $I_{LOAD} = 150\text{ mA}$
 $C_{NOISE} = 0.01\text{ }\mu\text{F}$

BLOCK DIAGRAM





DETAILED DESCRIPTION

The Si91841 is a low-noise, low drop-out and low quiescent current linear voltage regulator, packaged in a small footprint Thin SOT23-5 package. The Si91841 can supply loads up to 150 mA. As shown in the block diagram, the circuit consists of a bandgap reference error, amplifier, p-channel pass transistor and feedback resistor string. An external bypass capacitor connected to the BP pin reduces noise at the output. Additional blocks, not shown in the block diagram, include a precise current limiter, reverse battery and current protection and thermal sensor.

Thermal Overload Protection

The thermal overload protection limits the total power dissipation and protects the device from being damaged. When the junction temperature exceeds 150°, the device turns the p-channel pass transistor off.

Reverse Battery Protection

The Si91841 has a battery reverse protection circuitry that disconnects the internal circuitry when V_{IN} drops below the GND voltage. There is no current drawn in such an event. When the $\overline{SD}$ pin is hardwired to V_{IN} , the user must connect the $\overline{SD}$ pin to V_{IN} via a 100-k Ω resistor if reverse battery

protection is desired. Hardwiring the $\overline{SD}$ pin directly to the V_{IN} pin is allowed when reverse battery protection is not desired.

Noise Reduction

An external 10-nF bypass capacitor at BP is used to create a low pass filter for noise reduction. The start-up time is fast, since a power-on circuit pre-charges the bypass capacitor. After the power-up sequence the pre-charge circuit is switched to standby mode in order to save current. It is therefore not recommended to use larger bypass capacitor values than 50 nF. When the circuit is used without a capacitor, stable operation is guaranteed.

Auto-Discharge/No-Discharge

For Si91841 only, V_{OUT} has an internal 100- Ω (typ.) discharge path to ground when the $\overline{SD}$ pin is low.

Stability

The circuit is stable with only a small output capacitor equal to 6 nF/mA (= 1 μ F @ 150 mA). Since the bandwidth of the error amplifier is around 1–3 MHz and the dominant pole is at the output node, the capacitor should be capacitive in this range, i.e., for 150-mA load current, an ESR <0.4 Ω is necessary. Parasitic inductance of about 10 nH can be tolerated.

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