

- Programmable Wake-up Event Interface
- General Purpose Input/Output Pins (60 total)
- System Management Interrupt (SMI)
- GLUE Logic
 - 4 Buffered PCI Reset Outputs
 - Power OK Signal Generation
 - Power Sequencing
 - Power Supply Turn On Circuitry
 - Resume Reset Signal Generation
 - Speaker output
 - Intrusion Detection
- 2.88MB Super I/O Floppy Disk Controller
 - Licensed CMOS 765B Floppy Disk Controller
 - Software and Register Compatible with Microchip's Proprietary 82077AA Compatible Core
 - Configurable Open Drain/Push-Pull Output Drivers
 - Supports Vertical Recording Format
 - 16-Byte Data FIFO
 - 100% IBM® Compatibility
 - Detects All Overrun and Underrun Conditions
 - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
 - DMA Enable Logic
 - Data Rate and Drive Control Registers
 - 480 Address, Up to Eight IRQ and Four DMA Options
- Enhanced Digital Data Separator
 - 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
 - Programmable Precompensation Modes
- Keyboard Controller
 - 8042 Software Compatible
 - 8 Bit Microcomputer
 - 2k Bytes of Program ROM
 - 256 Bytes of Data RAM
 - Four Open Drain Outputs Dedicated for Keyboard/Mouse Interface
 - Asynchronous Access to Two Data Registers and One Status Register
 - Supports Interrupt and Polling Access
 - 8 Bit Counter Timer
 - Port 92 Support
 - Fast Gate A20 and KRESET Outputs
- Serial Ports
 - Two Full Function Serial Ports
 - High Speed NS16C550A Compatible UARTs with Send/Receive 16-Byte FIFOs
 - Programmable Baud Rate Generator
 - Modem Control Circuitry
 - Any LPC Address Configurable. 15 IRQ Options
- Multi-Mode™ Parallel Port with ChiProtect™
 - Standard Mode IBM PC/XT®, PC/AT®, and PS/2™ Compatible Bi-directional Parallel Port
 - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
 - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
 - ChiProtect Circuitry for Protection
 - 960 Addresses, Up to 15 IRQ and Four DMA Options

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General Description

The SCH5627 is a 3.3V PC 2001 compliant Super I/O controller with an LPC interface. All legacy drivers used for Super I/O components are supported making this interface transparent to the supporting software. The LPC bus also supports power management, such as wake-up and sleep modes.

The SCH5627 provides temperature monitoring with auto fan control. The temperature monitor is capable of monitoring up to three external diodes, one internal ambient temperature sensor or retrieving temperatures from external processors that implement the PECI Interface. This device offers programmable automatic fan control support based on one or more of these measured temperatures. There are four pulse width modulation (PWM) outputs with high frequency support as well as four fan tachometer inputs. In addition, there is support for a bi-directional PROCHOT# pin that may be used to generate an interrupt, adjust the programmed temperature limits in the auto fan control logic, or force the PWM outputs on full. The RRCC feature provides a linear relationship of temperature to fan speed.

The Glue Logic includes various power management logic; including generation of RSMRST# and Power OK signal generation. There are also two LEDs to indicate power status. The part also provides a low battery warning circuit.

The SCH5627 provides 60 General Purpose I/O control pins, which offer flexibility to the system designer.

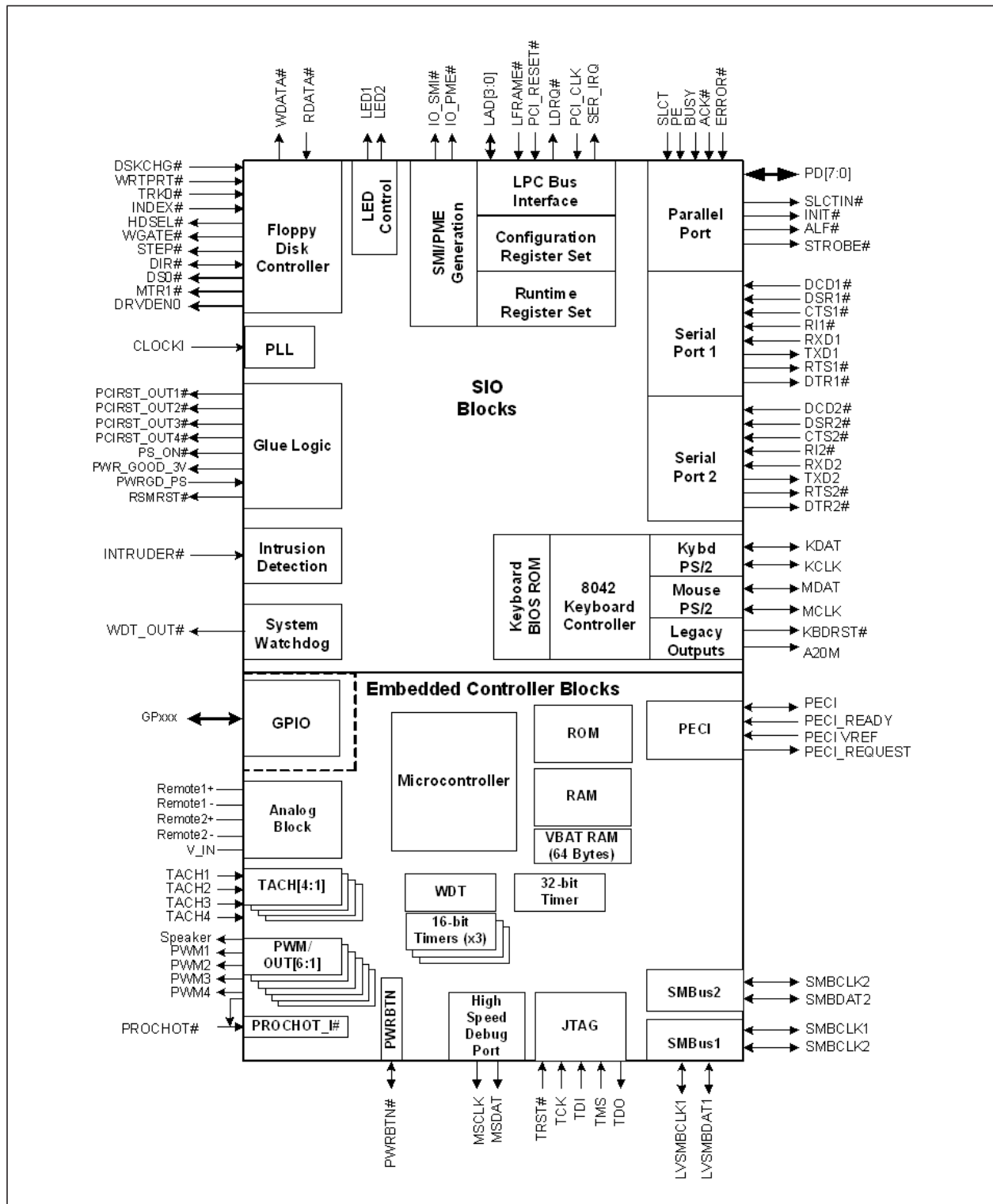
The SCH5627 incorporates the following Super I/O components: a parallel port that is compatible with IBM PC/AT architecture, as well as the IEEE 1284 EPP and ECP; two serial ports that are 16C550A UART compatible; a keyboard/mouse controller that uses an 8042 micro controller; and a floppy disk controller.

The SCH5627 is ACPI 1.0b/2.0 compatible and supports multiple low power-down modes. It incorporates sophisticated power control circuitry (PCC), which includes keyboard and mouse wake-up events.

The SCH5627 incorporates a high-performance embedded microcontroller. The SCH5627 communicates with the system host using the Intel® Low Pin Count bus.

The SCH5627 is directly powered by two separate suspend supply planes (VBAT and VTR) and senses a third runtime power plane (VCC) to provide “instant on” and system power management functions. The SCH5627 also contains an integrated VTR Reset Generator and a system power management interface that supports low-power states and can drive state changes as a result of hardware wake events as defined by the SCH5627 wake interface.

Block Diagram



APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001731A (05-01-14)	REV A replaces previous SMSC version Rev. 0.30 (01-25-1)	

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PART NO. ⁽¹⁾ - XXX ⁽²⁾ - [X] ⁽³⁾ Device Package Tape and Reel Option	Example: SCH5627-NS = 128-pin QFP Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21. Note 2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit http://www.microchip.com/pagehandler/en-us/aboutus/ehs.html. Note 3: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
Device: SCH5627 ⁽¹⁾ Package: NS = 128 pin QFP ⁽²⁾ Tape and Reel Blank = Tray packaging Option: TR = Tape and Reel ⁽³⁾	

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